Operational Stability of Organic Field-Effect Transistors

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Organic field-effect transistors (OFETs) are considered in technological applications for which low cost or mechanical flexibility are crucial factors. The environmental stability of the organic semiconductors used in OFETs has improved to a level that is now sufficient for commercialization. However, serious problems remain with the stability of OFETs under operation. The causes for this have remained elusive for many years. Surface potentiometry together with theoretical modeling provide new insights into the mechanisms limiting the operational stability. These indicate that redox reactions involving water are involved in an exchange of mobile charges in the semiconductor with protons in the gate dielectric. This mechanism elucidates the established key role of water and leads in a natural way to a universal "stress function", describing the stretched exponential-like time dependence ubiquitously observed. Further study is needed to determine the generality of the mechanism and the role of other mechanisms.

1. Introduction

Organic field-effect transistors (OFETs) are emerging as electronic switching elements in low-cost contactless identification transponders, electronic barcodes, and pixel engines of flexible active-matrix displays.[1–3] Long-term stability of these transistors is essential for commercial applications. Much progress has been made during the last decade in the development of environmentally stable p-type organic semiconductors with charge-carrier mobilities reaching up to 10 cm^2/Vs,[4–9] while more recently stable high-mobility n-type organic semiconductors have become available.[10–17]

However, high intrinsic stability of the semiconductor is not the only requirement for stable OFETs. Also the role of the gate dielectric needs to be considered. An important development has been the finding that the choice of the gate dielectric can lead to charge-carrier mobilities in the conducting channel of the organic semiconductor that differ by an order of magnitude or more.[7,18,19] It has been found that with the commonly used gate dielectric silicon-dioxide (SiO_2) electron trapping occurs at the interface between semiconductor and dielectric.[18] This was suggested to be caused by an electrochemical reaction in which silanols (Si-O-H, i.e., a hydroxyl, O-H, group bound to a Si atom) together with electrons in the semiconductor are transformed into $Si\text{-}O^-$ groups and H_2. By using a hydroxyl-free gate dielectric this electron trapping could be avoided and the resulting OFETs showed good n-channel conduction in most of the conjugated polymers studied.[18]

With the above problems being solved there remains one important problem that hinders widespread commercial introduction of OFETs: when OFETs are being operated their electrical characteristics change with time.[1–3,7,20] A very undesired consequence of this is that an OFET that is used to switch on a current, for example to drive a pixel in a display, will switch off in the course of time. The problem is due to the fact that the threshold gate voltage at which the transistor switches on gradually shifts to the gate bias voltage that is applied. This phenomenon is called the "bias-stress effect". Because the applied gate voltage determines the total amount of charges in the OFET accumulated close to the interface between the semiconductor and the dielectric, this means that somehow the mobile charges in the semiconductor channel are turned into immobile charges. Where precisely these immobile charges are located and what their character is has remained elusive for a long time,[20] mainly due to the experimental difficulty in detecting the processes that occur close to the semiconductor-dielectric interface in a working OFET.

A powerful technique that has become available in the last two decades is noncontact potentiometry of the potential in OFET structures by scanning Kelvin probe microscopy (SKPM).[21,22] With this technique the potential profile above a surface can be mapped out without making physical contact to the surface. The technique has been used to estimate the contact resistance at the source and drain contacts of a working OFET from the potential drop at these contacts[22] and to verify predictions coming from charge transport theories for the potential profiles in unipolar and bipolar transistors.[23,24] Important in the present context is that the technique can be used to study how potential profiles in a working OFET change as a function of time.[25] Studies of the spatio-temporal potential profile above the dielectric surface of an OFET structure without depositing the semiconductor[26] or after removing the semiconductor of a

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working OFET[27] have also been performed. Such studies provide a wealth of information on the time-dependent processes involving mobile and immobile charges that occur at the dielectric surface. We will see in this report that this information provides crucial clues for unraveling processes responsible for the operational instability of OFETs.

This Progress Report is built up as follows. In Section 2, we review the established facts that have been shown to be related to the operational instability of OFETs, with a focus on p-type OFETS with SiO_2 as gate dielectric. We discuss the similarities and differences with the operational instability of amorphous-silicon field-effect transistors (*a*-Si FETs), the reversibility of the threshold-voltage shift, and the role of the ambient conditions and the type of semiconductor. We also discuss the situation in which an OFET is stressed with a non-constant gate voltage, which leads to a non-monotonic time dependence of the transistor current, related to a memory effect. In Section 3 we discuss the results of SKPM potentiometry of the surface of the SiO_2 dielectric in an OFET structure, but without a deposited semiconductor. With a voltage applied to the drain contact the potential profile shows a time-dependence on a time scale that is independent of the polarity. From a comparison with work performed in the nineteen-sixties on the surface conductivity of SiO_2 the conclusion is drawn that the time evolution of the potential profile is caused by the motion of protons. Based upon this experiment and the other established facts, a mechanism is proposed for the operational instability in Section 4. The mechanism involves reversible redox reactions taking place at the interface between the semiconductor and the dielectric involving water, holes, oxygen, and protons, and a reversible migration of protons into the gate dielectric. We introduce a universal "stress function" that plays a central role in the mechanism. In Section 5 it is shown that the mechanism can explain the main established facts of the operational instability. The prediction that trapped charges are not located in the semiconductor but in the dielectric is corroborated by experiments where the semiconductor of an OFET that has been exposed to gate bias stress is removed, after which SKPM potentiometry on the transistor structure clearly shows the presence of charge. Also, the influence of the oxidation potential of the semiconductor on the characteristic time of the operational instability as predicted by the mechanism is verified. In Section 6 we discuss other proposed mechanisms for operational instabilities and several open issues, such as the explanation for the operational instability in n-type OFETs. A summary and conclusion are given in Section 7.

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2. The Operational Instability of OFETs: Established Facts

A common way to study the operational instability in OFETs is the following. The transistor is electrically stressed by applying a constant voltage to the gate electrode for a prolonged period of time. In order to study the change in the transistor characteristics by the stress, this situation is at short time intervals interrupted by a sweep of the gate voltage, during which the current is measured for a small applied source-drain voltage, yielding the transfer curve of the transistor. In this Progress Report we will often show measurements on a typical p-type bottom-contact and bottom-gate OFET grown on a heavily p-doped silicon wafer acting as the gate electrode. The transistor consists of a 200 nm thick thermally grown SiO_2 gate dielectric, on top of which an 80 nm thick layer of the conjugated polymer polytriarylamine (PTAA) is spin-coated. PTAA is a well-established

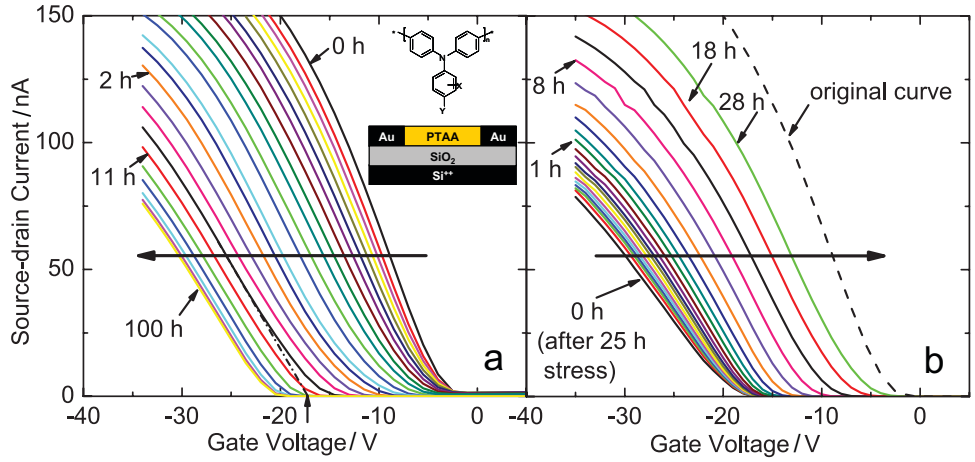

Figure 1. (a) Measured transfer curves after stressing an OFET with a gate bias voltage of –20 V for the indicated times. The source-drain voltage during the measurement of the transfer curve was –3 V. The dash-dotted line shows how the threshold voltage (arrow at horizontal axis) is determined. The inset shows the OFET structure and the chemical structure of PTAA, where X and Y are short alkyl chains. The measurements were performed at ambient conditions and a temperature of 30 °C. (b) Transfer curves measured at the indicated times after stressing the OFET for 25 hours and then grounding the gate electrode. The original transfer curve is indicated with the dashed line. Panel (a) is adapted and reprinted with permission from [50]. Copyright 2009, American Institute of Physics.

air-stable p-type amorphous semiconductor that exhibits charge-carrier mobilities of 10^{-3}–10^{-2} cm^2/Vs.[19] Before spin-coating, the surface of the SiO_2 is treated with hydrophobic hexamethyldisilazane (HMDS), which decreases the amount of water adsorbed onto the otherwise hydrophilic SiO_2 surface. The gold source and drain electrodes define a channel in the semiconductor with a width W of 2500 µm and a length L of 10 µm. The transfer curves of this transistor for different stress times with a gate voltage of –20 V are shown in **Figure 1**a. The main effect of the applied gate bias is a shift of the transfer curves to more negative gate voltages. **Figure 2** quantifies this effect by showing the shift in the threshold voltage as a function of time. The threshold voltage is defined here as the extrapolation of the linear part of the transfer curve to the gate-voltage axis; see the dash-dotted line and the arrow at the horizontal axis in Figure 1a. The transfer curves in Figure 1a show that the shift of the threshold voltage stops when it has reached a value that is about equal to the applied gate voltage during stress.

Following the analysis of the threshold-voltage shift in *a*-Si FETs[28] it has become customary[29,30] to fit the threshold-voltage shift in OFETs to a stretched-exponential function of the form

$$\Delta V_{th}(t) = V_0 \left(1 - \exp\left[-(t/\tau)^{\beta}\right]\right) \quad (1)$$

The data in Figure 1a can be very well fitted with this function (dashed line in Figure 2) using the fit parameters $V_0 = 19$ V for the prefactor, $\tau = 10^4$ s for the relaxation time, and $\beta = 0.43$ for the exponent. In the case of *a*-Si FETs different explanations for stretched-exponential behavior in trapping have been given, of which we mention: i) a defect relaxation model that is controlled by dispersive diffusion of hydrogen governed by a power-law time dependence[31] and ii) a local two-state defect model with an exponential distribution of barriers between the two states.[32] Since defects of the type present in *a*-Si do not exist in OFETs the explanation for the stretched-exponential dependence should be a different one.

The following features of the bias-stress effect in p-type OFETs with SiO_2 gate dielectric have been established:

1. The key role of water has been established in different ways. Gomes et al. have demonstrated that water on the surface of SiO_2 plays an important role in the bias-stress effect.[33]

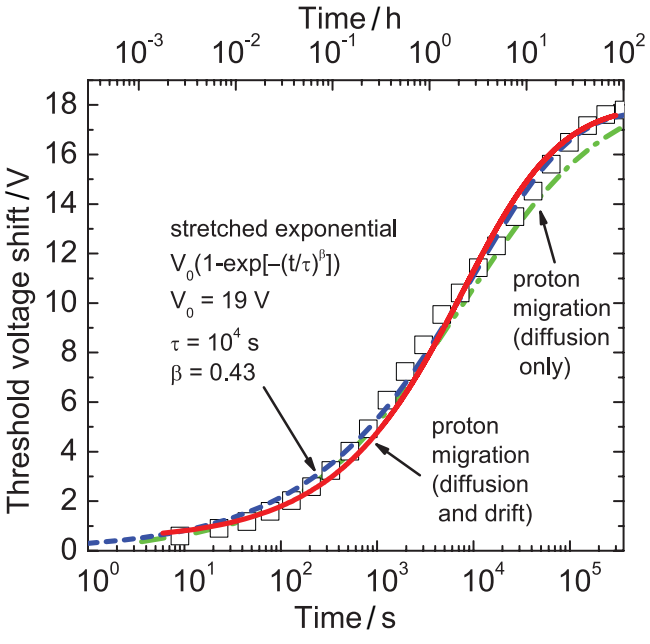

Figure 2. Threshold-voltage shift as a function of time for the transfer curves in Figure 1a (symbols) and a fit to a stretched-exponential function (dashed line). The other lines indicate the results for the proton migration mechanism with only diffusion (dash-dotted line) and diffusion and drift (solid line) of protons in the gate dielectric (see Section 5). Adapted and reprinted with permission from [50]. Copyright 2009, American Institute of Physics.

When investigating the effect as a function of temperature they found that, independent of the organic semiconductor and the deposition techniques, the bias-stress effect is only present above 200 K. This temperature corresponds to a known phase transition of supercooled water. Confined water does not freeze at 273 K but forms a metastable liquid, which finally solidifies at 200 K. It was therefore concluded that the effect only occurs in the presence of liquid water.[33] It was also shown that under vacuum conditions, with practically no water present on the SiO_2 interface, the bias-stress effect is significantly slowed down.[29,30,34,35] This is evident from the relaxation time of $\tau = 2 \times 10^6$ s, obtained from bias-stress measurements on a similar PTAA transistor as in Figure 1, but in vacuum.[30] This value is two orders of magnitude larger than the above value of $\tau = 10^4$ s in ambient conditions. Furthermore, pretreatment of the SiO_2 with HMDS[26] or octadecyltrichlorosilane (OTS)[36] is known to decelerate the effect. Use of a hydrophobic organic gate dielectric practically eliminates the effect[37] and the same holds for coverage of the SiO_2 with a layer that is impenetrable to water.[38]

2. The shift in the threshold voltage is reversible in a process called "recovery". Although recovery is often mentioned in studies of the operational instability of OFETs, thorough studies of the effect are rare. In recovery, the gate voltage of a transistor that has undergone stress is set to zero. The transfer curve then shifts back to the original curve. This is shown in Figure 1b, where the transfer curves of the investigated transistor are plotted after grounding the gate electrode following a 25 hours period of stress. The backward shift of the threshold voltage can also be fitted with a stretched-exponential function, with a relaxation time that is roughly the same as for stress.[30] This is unlike *a*-Si FETs, where the relaxation time for recovery is about two orders of magnitude larger than that for stress.[28]
3. The dynamics of the threshold-voltage shift during stress does not depend on whether or not a current flows through the transistor. The transfer curves measured for the case that a constant source-drain voltage is applied are the same as those for which during stress the source-drain bias is set to zero.[30]
4. The dynamics does not depend on the value of the gate voltage during stress. The only parameter that changes is the prefactor V_0 in the fit to the stretched-exponential function. The value of V_0 is always close to the absolute value of the applied gate voltage.[30]
5. The dynamics is thermally activated, i.e., $\tau = \tau_0 \exp(E_a/k_B T)$, with $k_B T$ the thermal energy. The activation energy E_a is about 0.6 eV and depends only weakly on the organic semiconductor. The relaxation time τ itself, however, depends strongly on the type of semiconductor and the ambient.[30]

In a transistor under real operating conditions the applied gate voltage is non-constant. One may therefore wonder what happens if instead of a constant, a non-constant voltage is applied to the gate.[39] In **Figure 3** we display the source-drain current for the case that the transistor is first stressed with a gate voltage of –20 V and then, after 900 s (15 minutes), with a voltage of –10 V. After the start of the stress the current, as expected, gradually decreases. Remarkably, however, after the switch from –20 V to –10 V the current first increases, reaches a maximum, and then continues to decrease. This is remarkable, since after 900 s the threshold voltage has not yet reached –10 V (see Figure 2), so that the transistor is still under stress conditions when the gate voltage is stepped to –10 V. One would therefore expect a monotonic decrease of the current. Instead, the transistor shows an anomalous bias-stress effect with a memory, in which the stress history apparently determines the future electrical behavior. The memory effect is clear from considering the state of the transistor at the points b and d in Figure 3. At both points the current and the gate voltage, and hence the number of mobile charges, is the same. However, the electrical behavior after these points is different. A viable explanation for the bias-stress effect in OFETs should be able to explain this anomalous effect.

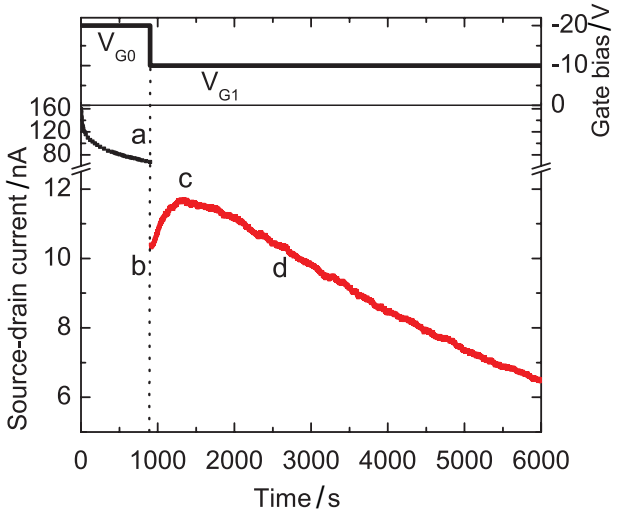

Figure 3. Source-drain current (bottom) of the OFET of Figure 1 as a function of time for the case that first a gate bias voltage of $V_{G0} = -20$ V is applied, which is switched to $V_{G1} = -10$ V after 900 s (top). The source-drain voltage during the measurement is –3 V. The meaning of the labels a-d is explained in Section 5. Adapted and reprinted with permission from [39]. Copyright 2010, American Institute of Physics.

We conclude this section by noting that, although n-type OFETs with SiO_2 gate dielectric suffer from electron trapping, as discussed in the previous section, it is still possible to fabricate such transistors. It is then found that n-type OFETs also show a bias-stress effect, as demonstrated for a perylene transistor in the supporting information of Ref. [27]. The question therefore comes up if there is a relation between the bias-stress effect in p-type and n-type OFETs. Although we give suggestions for such a relation in Section 6, we consider this as an open issue that requires more research.

3. Potentiometry at the SiO_2 Surface

The electrical potential measured above a surface gives information about the total charge present below that surface but not about the distribution of the charge. Potentiometry of an OFET

by SKPM is therefore not able to determine where the charges are located that cause the probed potential profile. The charges can be located in the semiconductor, at the interface between semiconductor and dielectric, or in the dielectric. In order to shed light on this issue, SKPM measurements of the surface potential were performed on a transistor structure as depicted in the inset of Figure 1a, but without deposition of a semiconductor.[26] **Figure 4** shows the time evolution of the potential profiles with grounded source and gate electrodes, after applying a potential to the drain electrode. Since SiO_2 is an insulator, one would expect to see a zero potential above the SiO_2 and only a non-zero potential above the drain electrode. However, Figure 4 makes clear that in the absence of a semiconductor charges can be present at the surface of the SiO_2 and that these charges can slowly move. Eventually, a linear potential profile from drain to source is established; see the last curve in Figure 4b.

The measurements were done after exposing the SiO_2 surface to a vapor of HMDS with different exposure times. This leads to different coverages of the surface with HMDS, as verified with low-energy ion scattering (LEIS).[26] The hydrophobicity of the surface was determined by measuring the contact angle of a water drop on the surface.[26] By comparing Figures 4a and b we come to the conclusion that the HMDS coverage has a strong influence on the charge dynamics, with a faster dynamics for the less hydrophobic surface. This suggests that the charge dynamics is correlated with the presence of water. This suggestion was verified by varying the ambient humidity: a reduced ambient humidity has the same effect as a higher HMDS coverage.[26]

Remarkably, the charge dynamics is insensitive to the polarity: the time scales for the charge motion are comparable for both polarities of the drain potential (compare the main panel and the inset of Figure 4a). Since it is extremely unlikely that charge carriers of different type have the same mobility, this points at two possibilities: i) charge carriers of opposite sign are bound to a third common species that determines the mobility of charges of both signs, or ii) the charge mobility is in both cases determined by a mobile charge carrier of one sign, moving with respect to a background of immobile carriers of the other sign, where the difference in concentration between mobile and immobile charges determines the net observed charge.

Surface-conductivity measurements on SiO_2 performed in the nineteen-sixties and repeated thirty years later have revealed an ionic nature of the conductivity.[40–42] It was shown that the surface conductivity increases with an increasing amount of water on the surface. The occurrence of electrolysis of water during the measurements was demonstrated explicitly by the replacement of water in the ambient by heavy water (D_2O) and the detection of deuterium gas (D_2) after performing the surface-conductivity measurements.[40] It was concluded that the charge carriers are protons (H^+), which move along the surface with a mobility that increases with the amount of adsorbed water.[42] Because of the presence of silanol groups the absorbed water layer is mildly acidic due to the reaction Si-O-H $\leftrightarrow$ Si-O^- + H^+.[43] Hence, there will be an abundance of protons in the absorbed water layer. At the electrodes, placed on the surface to measure the surface conductivity, the following redox reactions should then take place:

$$2H_2O \rightarrow 4H^+ + 4e^- + O_2\,(g)\,, \tag{2}$$

at the positive electrode, and

$$2H^+ + 2e^- \rightarrow H_2\,(g)\,, \tag{3}$$

at the negative electrode. The net result of the reactions (2) and (3) is the electrolysis of water under the production of oxyhydrogen (O_2 and H_2 in gas form). We note that due to the acidic conditions the reaction $2H_2O + 2e^- \rightarrow 2OH^- + H_2$(g) occurring at the negative electrode will be followed by the reaction $2OH^- + 2H^+ \rightarrow 2H_2O$, leading to the net reaction (3).

The above mechanism can explain the potentiometry measurements of Figure 4. The difference with the surface-conductivity measurements is the presence of a third electrode, the gate. After application of a positive voltage to the

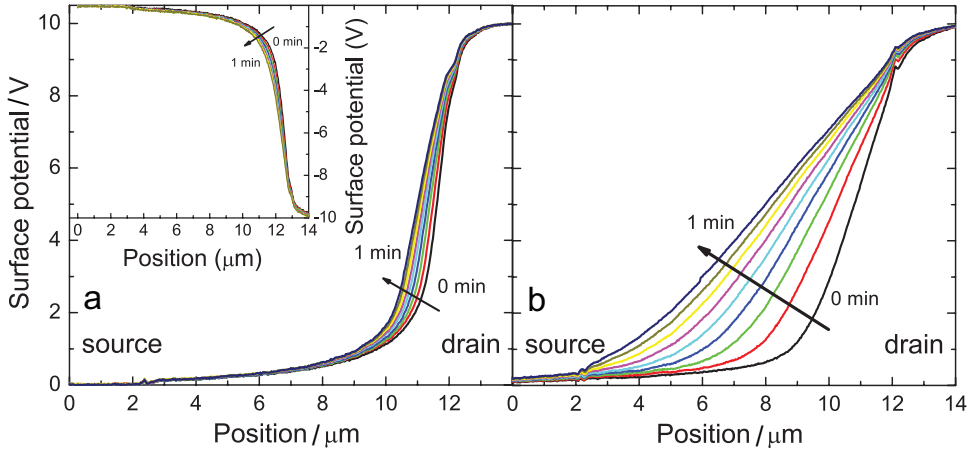

Figure 4. Surface potential measured by SKPM under ambient conditions of the transistor structure displayed in the inset of Figure 1a but without a semiconductor, for (a) a high and (b) a low HMDS coverage. A potential is applied to the drain contact, 10 V in the main panel of (a) and –10 V in the inset. The potential profile is measured at regular time intervals of 6 s. The source and gate contacts are kept at 0 V. Adapted and reproduced with permission from [28]. Copyright 2008, Wiley-VCH Verlag.

drain, the reaction (2) will take place at the drain contact, while no reaction will yet take place at the grounded source contact. The amount of protons close to the drain will increase, leading to a net positive charge (the proton charge minus the charge of the Si-O^- groups) that slowly spreads to the source electrode. Finally, a stationary situation is established where the potential decreases linearly from drain to source (see the last potential profile in Figure 4b). There is then a net current of protons from drain to source. When this situation is reached the reaction (3) will start to take place at the source contact, removing protons from the surface of the SiO_2. While a positive charge distribution emerges at the surface of the SiO_2, a compensating negative charge distribution, accounting for overall charge neutrality, emerges at the gate electrode.

On the other hand, when a negative voltage is applied to the drain, the reaction (3) will take place at the drain contact. The amount of protons close to the drain will decrease, leading to a net negative charge with more Si-O^- groups than protons. By motion of protons towards the drain the negative charge distribution spreads to the source electrode. When a stationary situation is established the reaction (2) will start at the source electrode. This scenario provides a natural explanation for the polarity independence of the potentiometry measurements, since for both polarities the time evolution of the potential profile is governed by the motion of protons. Hence, of the two possible explanations for the polarity independence of the time evolution of the potential profile we conjecture that the second is the appropriate one.

By integrating the amount of charge on the SiO_2 surface to obtain the total charge it is found that the total charge as a function of time can be fitted well with a stretched-exponential function.[26] Hence, on first thought it seems that an explanation can now also be given for the bias-stress effect for the case that a semiconductor is present: mobile charges in the semiconductor are slowly replaced by (almost) immobile charges at the SiO_2 surface. The role of water is clarified. Also, the reversibility can be explained: protons can be created in reaction (2) as well as removed in reaction (3), where the time scale is in both cases set by the motion of protons. The bias-stress effect for n-type OFETs can then be explained by a growing deficit of protons with respect to Si-O^- groups.

On second thought, however, the conclusion is that the above mechanism cannot be the full explanation for the bias-stress effect, for the following reasons: i) build-up of immobile charge only close to the source and drain contacts cannot lead to the observed uniform shift of the transfer curves with time; such a uniform shift can only be understood by build-up of immobile charge all along the transistor channel, ii) the mechanism cannot explain the memory effect shown in Figure 3. Clearly, an essential ingredient is still missing. This ingredient is introduced in the next section.

4. Proton Migration Mechanism

Aguirre et al.[44] have recently demonstrated that the charge transport in carbon-nanotube FETs (CFETs) with a SiO_2 gate dielectric in ambient is governed by the oxygen/water redox couple:

$$4H^+ + O_2 + 4e^- \leftrightarrow 2H_2O, \quad (4)$$

where the oxygen is solvated in the water layer adsorbed on the SiO_2 surface and where protons are present because of the slightly acidic nature of this layer (see the previous section). The redox reaction (4) suppresses electron transport in the carbon nanotube because of transfer of electrons from the nanotube to the water layer. In contrast to the reactions (2) and (3), where oxygen and hydrogen gas escape into the ambient, the redox reaction (4) is reversible, because of the solvated oxygen. Indeed it was shown, by sweeping the gate voltage back and forth while monitoring the current through the CFET, that the electrons can be reversibly transferred between the carbon nanotube and the SiO_2 surface.[44] SKPM measurements on a CFET have visualized the involved spatio-temporal charge-transfer process.[45] Since organic semiconductors are permeable to water,[36,46] water molecules can reach the SiO_2 surface in an OFET and form an adsorbed water layer as in the case of the above CFETs. The reaction (4) will therefore also occur at the interface between an organic semiconductor and the SiO_2 in an OFET, establishing an equilibrium between the charge in the accumulation layer of the semiconductor, in the form of either holes or electrons, and protons on the SiO_2 surface.

However, the establishment of such an equilibrium is expected to occur on a much shorter time scale than that of the bias-stress effect. Furthermore, it is not expected to lead to the memory effect shown in Figure 3. Another ingredient needs to be added that determines the time scale of the bias-stress effect and that is responsible for the memory effect. This additional ingredient is the reversible migration of protons into the bulk of the SiO_2. Reversible motion in SiO_2 is the basis of memory effects in $Si/SiO_2/Si$ devices, where protons shuttle through the SiO_2 layer from one Si layer to the other on a time scale of seconds to thousands of seconds,[47,48] i.e., on a similar time scale as the bias-stress effect in OFETs. DFT calculations predict an activation energy for proton diffusion in SiO_2 of E_d = 0.5 eV,[49] which is close to the $E_a \approx 0.6$ eV activation energy for the bias-stress effect measured in OFETs with different organic semiconductors.[30]

Based on these considerations, the following mechanism for the bias-stress effect in p-type OFETs is proposed:[50,51]

1. Holes in the organic semiconductor, indicated by "os^+", are in equilibrium with protons on the surface of the SiO_2 in the redox half reactions (4) and

$$os^+ + e^- \leftrightarrow os, \quad (5)$$

   where "os" refers to an electrically neutral site of the organic semiconductor.
2. Protons on the surface of SiO_2 are in equilibrium with protons in the SiO_2 close to the surface:

$$H^+ (\text{on } SiO_2) \leftrightarrow H^+ (\text{in } SiO_2)\,. \quad (6)$$

3. Protons in the SiO_2 close to the surface can reversibly migrate into the bulk of the SiO_2.

Since the migration of protons into the bulk of the SiO_2 is expected to be slow as compared to the reactions (4)-(6), the net

result of these reactions will be the establishment of an equilibrium between the surface concentration [os$^+$] of holes in the accumulation layer and the volume concentration [H$^+$] of protons in the SiO_2 close to the surface:

$$\left[H^+\right] = \alpha \left[os^+\right], \tag{7}$$

where the proportionality constant α, which has the dimension of an inverse length, is determined by the reaction constants of the reactions (4)–(6).

It is now a relatively straightforward matter to solve the drift-diffusion problem of the proton migration in the SiO_2 with the boundary condition Equation (7) for a fixed gate voltage V_{G0} and a zero or small source-drain voltage. The problem becomes particularly simple for the case that only diffusion of protons is taken into account and the penetration depth of the protons into the SiO_2 is small with respect to the thickness of the SiO_2 dielectric layer.[50,51] The solution of the diffusion problem is then conveniently given in terms of a universal dimensionless "stress function" $S(x)$ that is the solution of the equation[51]

$$S(x) = \frac{1}{2}\int_0^x \frac{S(x') - S(x)}{(x - x')^{3/2}}\, dx' + \frac{1 - S(x)}{x^{1/2}} \tag{8}$$

The surface concentration $h_0(t) = [os^+]$ of holes in the accumulation layer of the semiconductor is related to this dimensionless function by

$$h_0(t) = c_0\, S(t/t_0) \tag{9}$$

where the surface concentration constant c_0 and the characteristic time t_0 are given by

$$c_0 \equiv \frac{C\,|V_{G0}|}{e} \tag{10}$$

$$t_0 \equiv \frac{1}{\pi \alpha^2 D} \tag{11}$$

with C the capacitance of the SiO_2 dielectric per unit area, e the unit charge, and D the diffusion coefficient of protons in the SiO_2. The solution for the threshold-voltage shift as a function of time becomes[51]

$$\Delta V_{th}(t) = |V_{G0}|\left(1 - S(t/t_0)\right) \tag{12}$$

The only unknown parameter in this expression is the characteristic time t_0.

An extremely accurate approximation to the stress function $S(x)$ is

$$S(x) \approx \exp\left[-\frac{2}{\pi}\left(\frac{x}{1 + 0.35x^{0.64}}\right)^{1/2}\right] \tag{13}$$

which in the limit $x \to 0$ approaches the correct analytical result $S(x) = \exp\left[-2\sqrt{x}/\pi\right]$, obtained from Equation (8) in this limit. By comparing Equation (12) and Equation (13) with Equation (1) one observes that in the limit of short stress periods the exponent β is equal to 0.5, whereas for long stress periods β becomes $(1 - 0.64)/2 = 0.18$. The fitted result $\beta = 0.43$ in Section 2 can be regarded as a good comprise for describing the threshold-voltage shift as a function of time with a stretched-exponential function over a broad time interval. At $x \approx 4.8$ the argument of the exponent in Equation (13) is equal to –1, so that the relaxation time τ in Equation (1) can be linked to the characteristic time t_0 in Equation (12) by $\tau \approx 4.8 t_0$.

5. Application of the Proton Migration Mechanism

The dash-dotted line in Figure 2 provides a fit of the threshold-voltage shift to Equation (12) with $t_0 = 4.2 \times 10^3$ s.[50] The fit is good up to about 10^4 s. The reason why the fit becomes worse after this time is the neglect of the drift contribution to the proton motion, which is driven by the electric field in the gate dielectric. Because of the very steep gradients in the proton distribution at the start of stress, diffusion initially dominates over drift, but after about 10^4 s the situation reverses and the drift contribution becomes dominant. If this contribution is also taken into account, using a proton mobility μ as following from Einstein's relation, $D/\mu = k_B T/e$,[50] the full line in Figure 2 is obtained. This provides an excellent fit to the measured threshold-voltage shift. It is now possible to extract the parameters α and D separately, instead of only the product $\alpha^2 D$ appearing in the definition Equation (11) of t_0, with the result $\alpha = 2.2$ nm^{-1} and $D = 1.6 \times 10^{-19}$ cm^2/s. Furthermore, it is now possible to obtain an estimate of the penetration depth of the protons into the SiO_2. A penetration depth of about 30 nm is obtained at the end of the stress in Figure 1 for $t \approx 4 \times 10^5$ s, which is indeed much smaller than the thickness of 200 nm of the SiO_2 gate dielectric.[50,51] We are not aware of any measurements of the proton diffusion coefficient in the used gate dielectric of dry amorphous thermally grown SiO_2. However, the value we find is very close to a reported diffusion coefficient of 10^{-19} cm^2/s of protons in Si_3N_4.[52]

The anomalous bias-stress effect in Figure 3 can be explained in the way sketched in **Figure 5**.[39] The initially large gate voltage of $V_{G0} = -20$ V leads via the equilibrium Equation (7) between holes in the semiconductor and protons in the dielectric at the interface with the semiconductor to a high proton concentration in the dielectric. When the gate voltage is switched at $t_{switch} = 900$ s to the smaller value $V_{G1} = -10$ V, there has to be a proton flux back to the semiconductor in order to maintain the equilibrium. As a result, the number of holes in the accumulation layer temporarily increases and so does the source-drain current. At a time t_{max} a maximum in the number of holes and the current is reached, after which the number of holes and the current continue to decrease. The memory effect is now easily explained: despite the fact that the gate voltages and the currents at the points b and d in Figure 3 are the same, the future development of the currents is different, since the proton distribution in the dielectric is different; compare Figures 5b and d.

Since the anomalous bias-stress effect occurs at relatively short times, the drift contribution to the proton motion can be neglected. Because the problem then becomes linear, instead of Equation (9) the following result is obtained for the hole

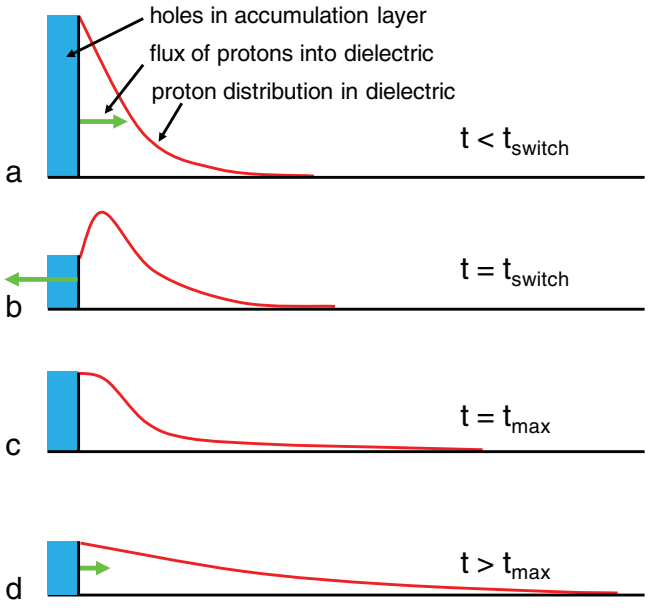

Figure 5. Explanation for the anomalous bias-stress effect. There is an equilibrium between holes in the accumulation layer of the semiconductor and protons in the dielectric at the interface with the semiconductor, indicated by the matching of the bar with the line. The figures (a)-(d) correspond to the points a-d indicated in Figure 3. (a) With the initially large gate voltage V_{G0} a high proton concentration is established in the dielectric just before the switching time t_{switch}; the proton flux is directed towards the dielectric and the transistor current is decreasing. (b) When the gate voltage is switched to a smaller value V_{G1} the proton flux is directed towards the semiconductor and the transistor current increases. (c) At some time t_{max} the proton flux becomes zero and the current reaches a maximum. (d) After t_{max} the proton flux is again directed towards the dielectric and the transistor current continues to decrease.

concentration $h(t)$ in the accumulation layer in terms of the stress function $S(x)$:[51]

$$h(t) = c_0 S(t/t_0) - (c_0 - c_1) S((t - t_{switch})/t_0)\theta(t - t_{switch}) \quad (14)$$

with $\theta(t)$ the Heaviside step function and $c_1 \equiv C|V_{G1}|/e$. The function $h(t)$ has the shape of the anomalous current transient in Figure 3. **Figure 6** shows a comparison of measured and predicted current transients, using the same value $t_0 = 4.2 \times 10^3$ s as obtained from the fit in Figure 2. The time-dependent hole concentration $h(t)$ can be translated to a time-dependent source-drain current with the help of the measured transfer curve before stress, displayed in Figure 1a. Apart from a current offset, which cannot be accurately determined,[39] the agreement between measured and predicted current transients for different gate voltages V_{G1} after switching and for different switching times t_{switch} is excellent. In particular, the time t_{max} of the current maximum is excellently predicted.

The proton-diffusion problem for a stress-recovery cycle can be solved by calculating the proton concentration profile in the dielectric after the stress and then putting the proton concentration at the interface with the semiconductor equal to zero, which corresponds to a grounded gate with no holes in the semiconductor.[51] During the recovery, the protons will move out of the dielectric towards the semiconductor and react with the solvated oxygen to form holes in the semiconductor and water in the reactions (4) and (5). This process leads to a backward shift of the threshold voltage. The dynamics of this backward shift depends on the proton concentration profile before recovery and thus on the duration of the stress. Hence, in contrast to the dynamics for stress, the dynamics for recovery is not universal. The dynamics of the backward shift of the threshold-voltage during recovery can also be fitted well with stretched-exponential functions, but the relaxation time τ and the exponent β now depend on the duration of the stress. In particular, the relaxation time τ for recovery becomes longer with a longer duration of the stress.[51] We can see this in Figure 1b, which shows that after 25 hours of stress the transfer curve has not yet returned to the original curve after an equally long period of recovery. Hence, a longer exposure of a transistor to stress makes it relatively more difficult to return the transistor to its initial state by recovery. This has important practical consequences for using recovery as a technique to "refresh" transistors that have undergone stress.

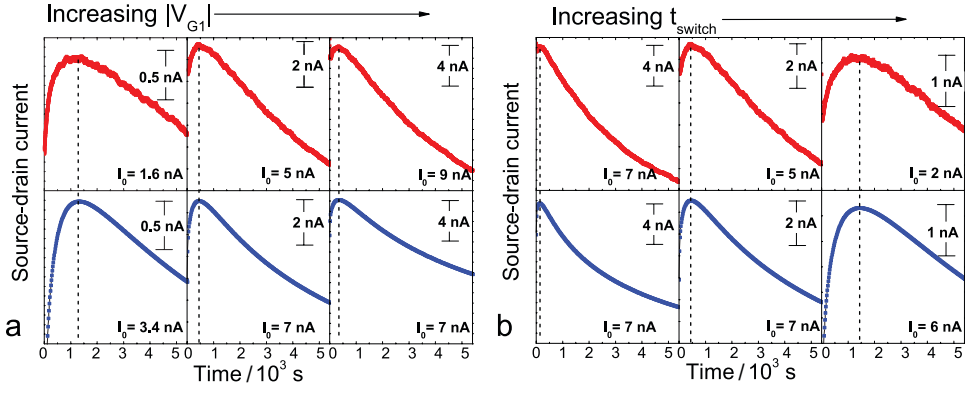

Figure 6. Experimental (upper curves) and theoretical (lower curves) anomalous current transients as a function of the time for the OFET of Figure 1 after switching from a gate voltage $V_{G0} = -20$ V to a lower gate voltage V_{G1} at t_{switch}. The source-drain voltage is −3 V. (a) Constant $t_{switch} = 900$ s and, from left to right, $V_{G1} = -7$, −10, and −12 V. (b) Constant $V_{G1} = -10$ V and, from left to right, $t_{switch} = 300$, 900, and 1800 s. The bars indicate the current scale. A subtracted current offset I_0 is indicated in each graph. The dotted lines indicate the times at which the maximum in the currents is reached. Adapted and reprinted with permission from [39]. Copyright 2010, American Institute of Physics.

Close inspection of the time evolution of the transfer curve in Figure 1a shows that during stress the slope of this curve in its linear region slightly decreases, pointing at a decreased charge-carrier mobility. This is not due to a degradation of the semiconductor, because the slope increases again during recovery; see Figure 1b. The lower charge-carrier mobility after stress should be attributed to scattering of mobile carriers in the accumulation layer of the transistor by the random Coulomb potential of the protons in the gate dielectric. The effect has recently been investigated for the case of a field-effect transistor consisting of a monolayer of a semiconducting molecule that is self-assembled on top of the SiO_2 (SAMFET).[53] For this case the effect of Coulomb scattering can be relatively easily investigated, because the carriers in the semiconductor are necessarily confined to a thin layer. By modeling the transfer curves, taking into account Coulomb scattering by a random distribution of protons in the gate dielectric, and comparing the modeled to the measured transfer curves it was concluded that after 15 days (1.3×10^6 s) of stress with a gate voltage of −30 V in ambient atmosphere the protons have penetrated into the gate dielectric to a distance of about 30 nm,[53] which is consistent with the distance obtained from the drift-diffusion modeling of the proton migration mechanism for the bias-stress effect discussed above.

Explicit proof that the immobilized charge responsible for the bias stress is not trapped in the semiconductor but at the dielectric surface or in the dielectric comes from SKPM potentiometry studies of OFETs that have undergone stress, performed after removing the semiconductor layer.[27] **Figure 7**a displays transfer curves of a sequence of identically prepared PTAA OFETs that have been exposed during different periods to gate bias stress with a gate voltage of −60 V. A logarithmic instead of a linear current scale is used, so that the low-voltage region can be seen more clearly. We define the "pinch-off voltage" as the onset of the current, as indicated in the figure. The saturation of the current at about 10^{-8} A is due to a parasitic leakage current.

Figure 7b displays the corresponding potential profiles measured by SKPM after exfoliation of the PTAA and grounding of all the electrodes. Easy exfoliation by peeling with a piece of adhesive tape is possible due to the treatment of the SiO_2 with HMDS, which lowers the interfacial energy.[27] Figure 7b shows that immediate exfoliation leads to a negative surface charge, probably due to Si-O^- groups.[18] The presence of a negative surface charge agrees with the positive pinch-off voltage found in Figure 7a for the unstressed OFET. For the OFETs that have undergone stress for a period longer than 15 minutes a positive surface charge appears in Figure 7b, in agreement with the negative pinch-off voltage in Figure 7a. The inset in Figure 7a gives the surface potential in the middle of the channel as a function of the pinch-off voltage for the different curves in the main panel of Figure 7a, showing a clear linear relation between the two quantities. After the exfoliation a fresh semiconductor can be adhered again to the stressed transistor structure, after which again a negative pinch-off voltage is measured.[27] This demonstrates unequivocally that the bias-stress effect is not related to charges trapped in the semiconductor, in agreement with the proton migration mechanism. We can, however, not conclude that the charges are trapped within the SiO_2, because SKPM

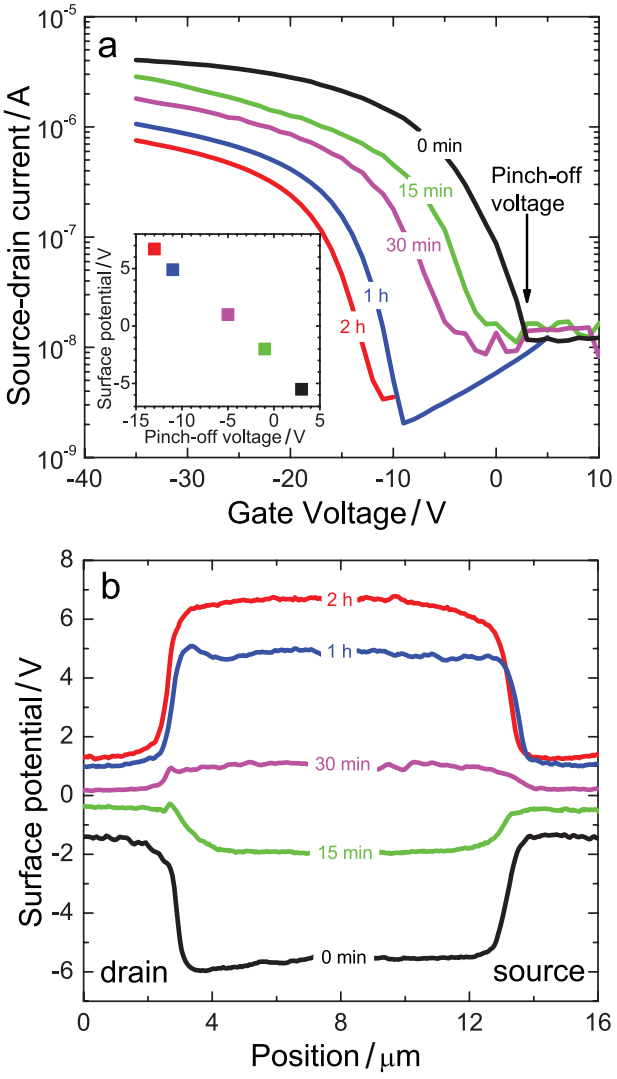

Figure 7. (a) Transfer curves of PTAA OFETs that have been exposed under ambient conditions to bias stress with a gate bias voltage of −60 V during the indicated periods. The source-drain voltage is −5 V. (b) Surface potential of these OFETS as measured by SKPM after exfoliation of the PTAA and grounding of all the electrodes. The inset in (a) gives the surface potential from (b) in the middle of the channel as a function of the pinch-off voltage for the different curves in (a). Adapted with permission from [27]. Copyright 2010, Wiley-VCH Verlag.

potentiometry cannot distinguish between charges trapped on the SiO_2 surface or in the bulk of the SiO_2.

The SKPM potentiometry after exfoliation has been performed for several p-type as well as n-type OFETs.[27] The results for an n-type perylene OFET with SiO_2 gate dielectric show that the bias-stress effect is in that case accompanied by a build-up of negative charge at the SiO_2 surface (see the supporting information of Ref. [27]).

We now come to the study of the dependence of the time scale of the bias-stress effect on the organic semiconductor.[54] The characteristic time t_0 of the proton migration mechanism is given by Equation (11). Since the diffusion coefficient D in this equation is related to diffusion of protons in the SiO_2 it does

not depend on the specific semiconductor used in the OFET. The parameter α depends on the rate constants of the reactions (4)–(6). The reactions (4) and (6) do not directly involve the semiconductor and the corresponding rate constants are therefore not expected to depend strongly on the semiconductor. However, the rate constant of reaction (5) will depend strongly on the oxidation potential of the semiconductor, which is directly related to the semiconductor's highest occupied molecular orbital, E_{HOMO}. One can derive the following expression for α:[54]

$$\alpha \propto \frac{[H_2O]^{1/2}}{[O_2]^{1/4}} \exp\left[\frac{E_{HOMO} - 4.97eV}{4k_B T}\right] \quad (15)$$

where it has been used that the electrode potential of the reaction (4) with respect to the standard calomel electrode (SCE) is 0.57 V, assuming a pH of 7, and the electrode potential of the reaction (5) with respect to the SCE is $E_{HOMO}/e - 4.4$ V.[55] Together with the activated behavior of proton diffusion in SiO_2, $D = D_0 \exp(-E_d/k_B T)$, this then leads to the following result for the relaxation time τ of the bias-stress effect:

$$\tau \propto t_0 \propto \frac{1}{\alpha^2 D} \propto \frac{[O_2]^{1/2}}{[H_2O]} \exp\left[-\frac{E_{HOMO} - 4.97eV}{2k_B T}\right] \exp\left(\frac{E_d}{k_B T}\right) \quad (16)$$

This relation is tested in **Figure 8**, which displays the measured room-temperature relaxation time τ of OFETs of different semiconductors as a function of E_{HOMO}. The line with slope $-1/2k_B T$ is a rough fit to Equation (16). The proportionality constant found in this fit cannot be verified due to experimental uncertainties in the amount of water adsorbed onto the SiO_2, the partial oxygen pressure, and other factors. Another uncertainty is that even with identical ambient conditions the water and oxygen uptake of different semiconductors will be different. Also, the electrode potentials of a confined layer of water will be different from those of bulk water, as used above. Despite these uncertainties the predicted trend in Figure 8 seems to be generally followed by the experimental data.

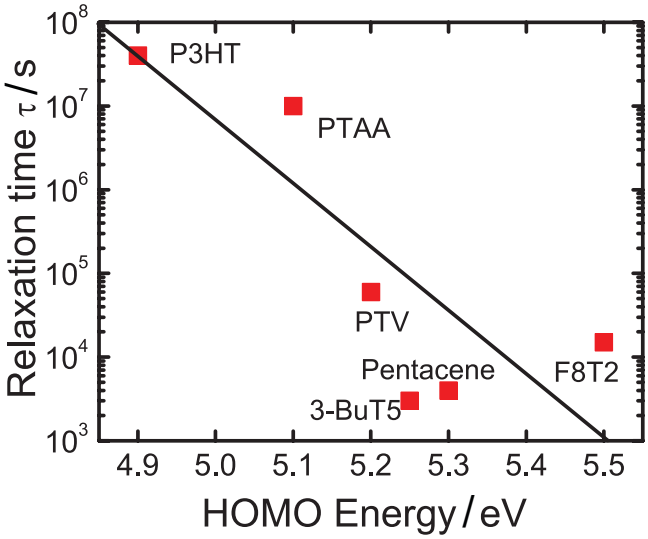

Figure 8. Symbols: room-temperature (25°C) relaxation time τ of the bias-stress effect of OFETs of different semiconductors as a function of the semiconductor HOMO energy. The line with slope $-1/2\ k_B T$ is a fit to Equation (16). The semiconductors are poly(3-hexylthiophene) (P3HT), polytriarylamine (PTAA), polythienylene-vinylene (PTV), 3-butyl-quinquethiophene (3-BuT5), pentacene, and poly(9,9'-dioctyl-fluorene-co-bithiophene) (F8T2). Adapted and reprinted with permission from [54]. Copyright 2011 American Institute of Physics.

It follows from Equation (16) that the activation energy E_a for the bias stress-effect is not precisely equal to the activation energy E_d for diffusion of protons in SiO_2, but corrected by the term $(E_{HOMO} - 4.97\ eV)/2$. For $E_{HOMO} \approx 5eV$ this correction is small. A further quantitative analysis is prohibited by the uncertainties in the determined activation energies.[30] We should note here that because of the expected slight acidity of the water layer adsorbed onto the SiO_2, the electrode potential of reaction (4) is probably somewhat larger than 0.57 V,[44] correcting the above 4.97 eV (= (4.4 + 0.57) eV) to a higher value.

Equation (16) shows that in order to reduce the operational instability, an organic semiconductor with an as low as possible HOMO energy should be used, preferably well below 5 eV. However, with such a low HOMO energy the semiconductor becomes unstable towards oxidation. The only route towards stable organic transistors is thus the elimination of water.

6. Other Proposed Mechanisms and Open Issues

We will now discuss other mechanisms that have been proposed to explain operational instabilities of OFETs. The most commonly proposed mechanisms are based on slow trapping of mobile charges. The location of these traps could be at grain boundaries in the semiconductor,[56,57] at the semiconductor-dielectric interface,[58] or in the bulk of the semiconductor.[59] In order to yield a stretched-exponential dependence of the time dependence of the threshold-voltage shift, a wide distribution of trapping times has to be present. Such a wide distribution can be obtained by a distribution of energy barriers or distances between the mobile charges and the traps. Since in studies of the bias-stress effect the threshold voltage is observed to shift all the way to the applied bias voltage, no matter how large this bias voltage is, the number of traps should be extremely large, which seems a problematic feature of trapping mechanisms. Furthermore, if recovery is supposed to occur by slow detrapping it is not clear how these mechanisms can explain why in an equilibrium situation between trapping and detrapping the threshold voltage should be close to the applied bias voltage. Finally, it is not clear how trapping mechanisms can explain the specific memory effect observed in the anomalous bias-stress effect discussed in Section 2.

Nevertheless, there is compelling evidence that trapping mechanisms do play a role in OFETs of polycrystalline pentacene.[60] Use of a gate dielectric consisting of SiO_2 with a Cytop (a highly hydrophobic fluoropolymer) layer on top eliminates the bias-stress effect in single-crystal pentacene OFETs, demonstrating that with this dielectric there is no migration of

protons into the SiO_2. However, the polycrystalline pentacene OFETs with this dielectric do show a bias-stress effect, which was attributed to trapping of charges in the grain boundaries between the crystallites.[60] Indications for charge trapping in disordered grain boundaries also come from SKPM measurements of OFETs of the high-mobility polymer poly[2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene] (pBTTT): the potential above a stressed OFET shows structures on a 100 nm length scale that are correlated with the topography of the polymer.[57] These results appear to show that under certain circumstances charge trapping in the semiconductor can lead to an operational instability. It would be interesting to further investigate the properties of the instability in these circumstances, like the reversibility and the memory effect.

The bias-stress effect has also been explained with a bipolaron mechanism.[61] The idea of this mechanism is that two charges of the same sign can form an immobile doubly charged state, a bipolaron, where the carriers are bound by a shared lattice deformation. Because of the Coulomb repulsion of the charges at large distance, there is an energy barrier between the two separated charges and the bipolaron state, and this could explain the long time scale of the bias-stress effect. The ratio of the time scales of the bias-stress effect and the recovery is in this mechanism determined by the stability of the bipolaron with respect to the charge-separated state. Because of the bimolecular reaction involved in the formation of a bipolaron from two charges, the bipolaron mechanism predicts a time derivative of the decrease of the number of mobile carriers that is initially proportional to the square of the number of mobile carriers. For very short times such a behavior was indeed found for p-type OFETs of poly(9-9'-dioctyl-fluorene-co-bithiophene) (F8T2) and a regioregular polythiophene.[61] The bipolaron mechanism can also explain illumination-induced recovery in the F8T2 OFETs. The idea here is that the absorbed light creates free electron-hole pairs in the F8T2. The bipolaron state has a double positive charge to which an electron is strongly attracted. The electron recombines with one of the holes and a mobile hole is released.[61]

Although the bipolaron mechanism can explain some aspects of the operational instability, there are experimental observations that cannot be explained by the mechanism: i) for longer time scales, when the threshold-voltage shift is more than 50% of the total final shift, the rate at which the threshold-voltage shift occurs was found to be proportional to the fourth power of the gate voltage;[62] this would suggest a process involving four charges, which seems unlikely, ii) illumination-induced recovery is observed in some OFETs, like in the above F8T2 OFET, but it is not a generally observed phenomenon, iii) the bipolaron binding energy is expected be different for different organic semiconductors, whereas the activation energy of the bias-stress effect is observed to vary only weakly with the semiconductor.[30]

Contact degradation has also been suggested to cause an operational instability.[63] It was found that the relative arrangement of the charge injecting source/drain contacts with respect to the charge accumulation layer at the interface influences the device degradation upon application of a gate bias. Using SKPM potentiometry, a real-time measurement of the potential drop near the source and drain contacts was performed. Two types of device architectures were investigated: a coplanar and a staggered architecture. In the coplanar device configuration the source and drain contacts are patterned on the gate dielectric before deposition of the semiconductor. In the staggered configuration the source and drain contacts are put on top of the organic semiconductor. Based on their measurements, the authors suggested that in coplanar device configurations an increase in source contact resistance during current flow is primarily responsible for a rapid device degradation.[63] On the other hand, in staggered device configurations the current reduction is significantly lower and this was attributed to charge trapping in the channel. In the staggered device configurations the contacts do not exhibit a significant degradation when exposed to bias stress.[63] The authors did not suggest a mechanism for the increase in contact resistance on application of a gate bias and the reversibility of the degradation was not addressed. We note that in the studies presented in this report contact degradation was never found to play an important role, so that the generality of this cause for operational instability might be limited.

Recently, the bias-stress effect was investigated in p-type OFETs of single-crystalline organic semiconductors with a parylene gate dielectric.[64] A model was proposed in which holes in the semiconductor move into the localized electronic states in the disordered parylene. Dispersive transport of these holes in the parylene dielectric then leads to a stretched-exponential time dependence of the threshold-voltage shift in the case of diffusion-dominated hole transport and a to stretched-hyperbola time dependence in the case of drift-dominated transport. It was experimentally observed that a larger HOMO energy of the crystalline semiconductor leads to an increased rate of the bias-stress effect, which was attributed to a better overlap with the density of states of localized states in the parylene.[64] We note that the explanation for the bias-stress effect put forward in this report also predicts an increased rate with increasing HOMO energy; see Figure 8. We do not exclude the possibility that in the measurements of Ref. [64] also proton production at the interface between the crystalline semiconductor and the parylene takes place, with subsequent migration of these protons into the parylene. In this context we recall that it has been established that single-crystalline pentacene is permeable to water.[46] It was not discussed in Ref. [64] how the proposed mechanism explains recovery, whereas this is naturally explained by the proton-migration mechanism.

The proton-migration mechanism discussed in this report has been specifically investigated for p-type organic field-effect transistors with SiO_2 as gate dielectric. However, the redox reactions (4) and (5) on which the mechanism is based are not specific for SiO_2, but only rely on the presence of water. The migration of protons into the gate dielectric should also not be specific for SiO_2. In fact, the bias-stress effect also occurs in OFETs with other gate dielectrics,[65] including the above mentioned parylene.[64] Interestingly, the effect also occurs in field-effect transistors of amorphous oxide semiconductors with SiO_2 gate dielectric.[66] The acceleration of the effect upon exposure to water vapor[66] suggests that also in this case the proton migration mechanism could be responsible for the effect. This would mean that the proton migration mechanism is a phenomenon that occurs not exclusively in organic transistors.

Although not discussed in detail in this Progress Report, the bias-stress effect also occurs in n-type OFETs with SiO_2 gate dielectric[67] (see also the supporting information of Ref. [27]). The dynamics of the threshold-voltage shift for n-type OFETs can also be fitted with a stretched-exponential function.[67] In the light of the proton-migration mechanism this may seem a puzzle. However, we suggest that an explanation may be found in an equilibrium that should exist between negatively charged Si-O^- groups on the SiO_2 surface and protons in the SiO_2 even before application of a gate bias (see also the discussion of Figure 4 in Section 3). Application of a positive bias in the case of n-type OFETs should then result in a motion of the protons already present in the SiO_2 towards the semiconductor, resulting in a removal of electrons from the semiconductor in the redox reaction (4) and, instead of reaction (5), the redox reaction

$$os + e^- \leftrightarrow os^-, \tag{17}$$

where os^- now stands for a negatively charged unit of the organic semiconductor. This would then lead to a shift in the threshold voltage to more positive voltages. Hence, the idea would be that threshold-voltage shifts are polarity-independent, similarly to the polarity-independent charging of the SiO_2 surface found in Section 3. This suggestion should of course be further investigated.

We conclude this section by noting that the evidence for the involvement of protons in the bias-stress effect is at this moment still indirect. The modeling of the bias-stress effect presented in this Progress Report only requires the existence of positively charged species that can diffuse into the gate dielectric. Motion of holes in SiO_2 has also been reported in the past, with an activation energy close to that of proton motion: 0.6 eV.[68] However, in that work the holes originated from electron-hole pairs that could only be created at very high electric fields and with ionizing radiation of 18 eV. Moreover, the hole mobility determined in that work (about 10^{-9} cm^2/Vs at room temperature) is much too large to explain the observed time scale in the bias-stress effect. Together with the widely reported influence of water and the known electrochemistry involving protons and water at the SiO_2 surface, this leaves protons as the logical candidate for the involved charged species. Explicit detection of an excess of protons in the gate dielectric after bias stress would provide final proof for the proton mechanism, but because of the very small concentrations involved such detection will be extremely difficult. A possibility to provide such proof is perhaps the exposure of the OFET to (partly) tritiated water (T_2O or HTO) and the radiometric detection of tritium in the dielectric after bias stress.

7. Summary and Conclusion

In this Progress Report we have reviewed the various aspects of the operational instability in organic field-effect transistors (OFETs). The instability occurs when an OFET undergoes an electrical stress by applying a bias voltage to the gate electrode during a long period. The threshold voltage at which the transistor switches on then gradually shifts in the direction of the gate voltage applied during stress. The effect is caused by a transformation of mobile into immobile charge, but the character of the involved immobile charge and the location of this charge have remained elusive for many years. We have discussed in detail a recently proposed mechanism for this charge immobilization. The mechanism is based on redox reactions involving holes in the semiconductor, water, oxygen, and protons. The produced protons can slowly migrate into the gate dielectric and form the immobilized charge responsible for the shift in the threshold voltage.

We have focused the discussion on p-type OFETs of an air-stable polymeric semiconductor with a silicon-dioxide (SiO_2) gate dielectric. Studies of the potential profile by non-contact potentiometry of a transistor structure without a deposited semiconductor revealed slowly moving charges at the SiO_2 surface when a potential is applied to the drain contact. On the basis of previous studies of charge conduction on the SiO_2 surface, protons present in an adsorbed water layer were identified as the moving charged species. In an operating OFET protons will also be present in an adsorbed water layer on the SiO_2 surface in an equilibrium with mobile charges in the accumulation layer. Proton migration into the SiO_2 then leads to the final immobilization of charge and determines the time scale of the bias-stress effect. Potentiometry after semiconductor exfoliation of OFETs exposed to gate bias stress shows that the immobilized charges are not located in the semiconductor, providing evidence for the exchange of charge between semiconductor and dielectric.

The main conclusion of this Progress Report is thus that water is the main culprit behind the operational instability of OFETs. The route towards stable OFETs therefore lies in the elimination of water. As mentioned in the previous section, single-crystalline pentacene OFETs using a SiO_2 dielectric with a hydrophobic layer of Cytop on top, repelling water from the semiconductor-dielectric interface, have been shown to be immune to bias stress.[60] This is a very encouraging result.

Finally, we want to remark that calculations within the framework of density-functional theory have shown that water at the Si-SiO_2 interface can undergo oxidation to produce protons in the presence of holes.[69] This is comparable to what is in this Progress Report proposed to happen at the interface between an organic semiconductor and SiO_2. In a similar way as in OFETs these protons may move into the SiO_2. It might therefore be useful to investigate if the proton-migration mechanism discussed in this Progress Report can provide an alternative to the existing explanations for the bias-stress effect occurring in *a*-Si field-effect transistors.

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