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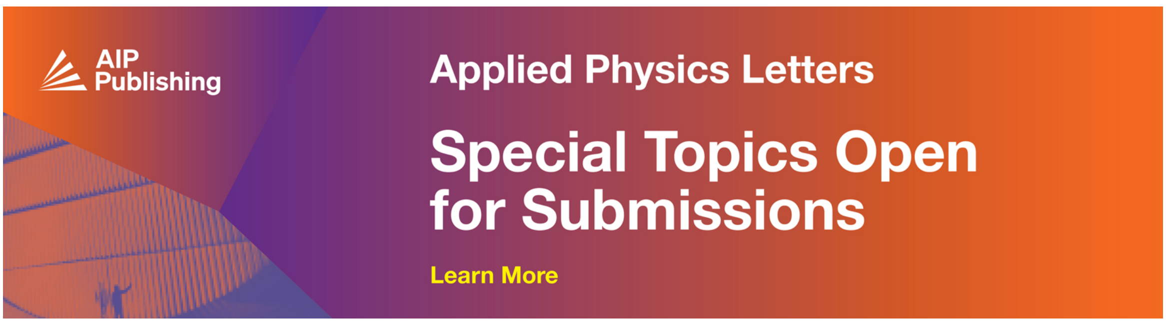

Anomalous current transients in organic field-effect transistors

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Here we study the origin of the gate bias-stress effect in organic *p*-type transistors. Based on water-mediated exchange between holes in the semiconductor and protons in the gate dielectric, we predict anomalous current transients for a non-constant gate bias, while ensuring accumulation. When applying a strongly negative gate bias followed by a less negative bias a back-transfer of protons to holes and an increase of the current is expected. We verify this counterintuitive behavior experimentally and can quantitatively model the transients with the same parameters as used to describe the threshold voltage shift. © *2010 American Institute of Physics*. [doi:10.1063/1.3339879]

Organic field-effect transistors are the basic building blocks of ultralow cost contactless identification transponders, or electronic barcodes, and pixel engines of flexible active matrix displays.[1,2] The bottleneck for commercial introduction is their operational stability. The electrical instability under the application of a prolonged constant gate bias is manifested as a shift of the threshold voltage the gate bias voltage at which the transistors switches on with time. This shift in threshold voltage leads to a monotonically decreasing source-drain current. The effect is usually referred to as the "bias-stress effect" and its origin is heavily debated.[3–6] It has been extensively studied in *p*-type organic transistors with silicon-oxide (SiO_2) as gate dielectric. Recently, we proposed a mechanism for the effect in these transistors based on the production of protons in the accumulation layer of the transistor from holes and water and subsequent migration of these protons into the gate dielectric.[7] We showed that the resulting model quantitatively explains the observed stretched-exponential dependence of the threshold-voltage shift with time. The model also explains various other aspects of the bias-stress effect, such as the activation energy of about 0.6 eV, independent of the semiconductor,[8] and the influence of water.[9–15] The amount of water needed is extremely small: Only an adlayer of water, which is present even for a device that has been kept in vacuum for several days, is sufficient.

In practical applications, however, transistors are not biased statically but dynamically, i.e., the applied biases are a function of time. Little or no attention has been paid to this case. In the present letter, we explore the case of a time-varying gate bias and study the predictions of the above model. We first show that the model predicts anomalous non-monotonic current transients for this case. We then show the results of measurements that clearly display these anomalous current transients, using the same OFET as in our study of the bias-stress effect.[7] Finally, we demonstrate that we can model these current transients quantitatively, using exactly the same parameters as used in our modeling of the bias-stress effect. We note that in this modeling the diffusive component of the proton flux was found to dominate over the drift component during the time period relevant for the present discussion.[7] Therefore, we will only take into account proton diffusion.

For completeness, we mention the main ingredients of the model.[7] (1) In the accumulation layer there is a thermodynamic equilibrium between holes and protons, where in the presence of water holes are converted into protons and oxygen, while protons are back-converted into holes and hydrogen. The net effect of these reactions is the production of oxyhydrogen (H_2 and O_2). (2) There is thermodynamic equilibrium between protons in the accumulation layer and protons in the SiO_2 close to the interface with the semiconductor. (3) Protons move in the SiO_2 by diffusion and drift and this motion is the rate-limiting process. The combination of (1) and (2) leads to an equilibrium between the surface density $[h^+]$ of holes in the accumulation layer and the volume density $[H^+]$ of protons in the SiO_2 at the interface with the semiconductor, which can be expressed as,

$$[H^+] = \alpha[h^+], \quad (1)$$

where the parameter α is determined by the reaction constants and the amount of water present at the semiconductor interface with the dielectric. The motion of protons in the SiO_2 is quantified by a diffusion constant D.

We will consider the situation that the transistor is prestressed with a strongly negative gate bias V_{G0}. During this prestressing period protons will diffuse from the interface into the bulk of the SiO_2, leading to a decrease of holes in the accumulation layer according to Eq. (1) and hence to a decreasing source-drain current. The density profile of protons during this period is sketched in Fig. 1(a). Then, at time $t = t_1$, the gate bias is stepped to a less negative voltage V_{G1}, which is still negative enough to ensure that the transistor is in accumulation mode. The hole density in the accumulation layer will suddenly decrease and so will the proton density in the SiO_2 at the interface with the semiconductor. The proton density profile immediately after this step is sketched in Fig. 1(b). After this step the proton flux will be directed toward the semiconductor. The excess protons will be converted back into holes, leading to an increase of the current. At a particular time t_{max}, a maximum in the current will be

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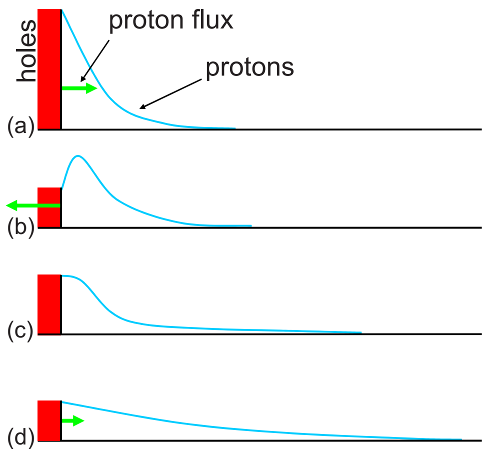

FIG. 1. (Color online) Sketch of the mechanism behind the anomalous current transients. Bars: hole density in the accumulation layer. Lines: proton density in the dielectric, scaled such that the lines connect continuously to the red bars at the interface. Arrows: proton flux from semiconductor into dielectric, or vice versa. (a) Applying a strongly negative gate bias V_{G0} creates a decaying proton concentration profile. There is a proton flux into the dielectric and the source-drain current decreases with time. (b) Immediately after switching to a less negative gate voltage V_{G1} at time t_1 the proton concentration at the interface decreases. Excess protons in the bulk of the dielectric diffuse back towards the semiconductor and convert back into holes, leading to an increasing current. (c) At a certain time t_{max}, the flux of protons is zero and the current reaches a maximum. (d) The proton flux is again directed into the dielectric. The source-drain current continues to decrease with time.

reached when the proton flux at the interface becomes zero; see Fig. 1(c). After that time, the proton flux at the interface reverses sign again and the usual bias-stress effect continues; see Fig. 1(d). Hence, the current transient resulting from this time-varying gate bias will be nonmonotonic, despite the fact that the transistor is all the time in accumulation and therefore under stressing conditions.

We checked the above prediction by applying such gate biasing scheme, shown in the upper panel of Fig. 2: A prestressing gate voltage $V_{G0}=-20$ V is followed by a step to a voltage $V_{G1}=-10$ V after a prestressing time $t_1=900$ s. The lower panel of Fig. 2 shows the resulting source-drain current, which exactly shows the predicted behavior. The indicated points a–d correspond in the same order to Figs. 1(a)–1(d). Importantly, we made sure that the transistor remains well into accumulation mode during the whole experiment. We remark that the occurrence of a nonmonotonic current transient is not predicted by other models for the bias-stress effect that we know of,[7] which would rather predict a current transient indicated by the dashed line in Fig. 2. The nonmonotonic nature of the transient shows that the OFET has a "memory" of its biasing history. This is clearly demonstrated by the fact that at the points b and d in Fig. 2 the source-drain current is the same, whereas the future development of the current is not. This memory effect is caused by the "storage" of protons in the gate dielectric, which is a unique feature of the present model.

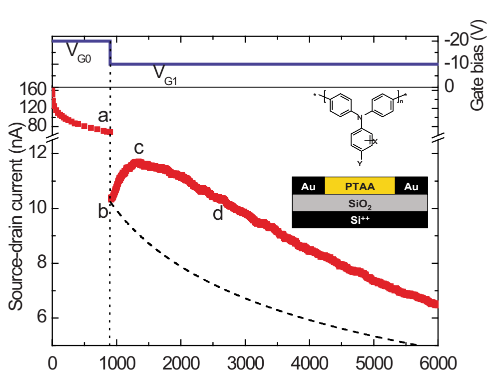

FIG. 2. (Color online) Upper panel: Dynamic switching scheme of the gate bias voltage V_G. Lower panel: Source-drain current I_{SD} vs time t for a source-drain voltage $V_{SD}=-3$ V. The dotted line indicates the switching time $t_1=900$ s. The dashed line indicates the expected transient. Inset: Transistor structure, with a polytriarylamine derivative as semiconductor. The transistor used is the same as in Ref. 7.

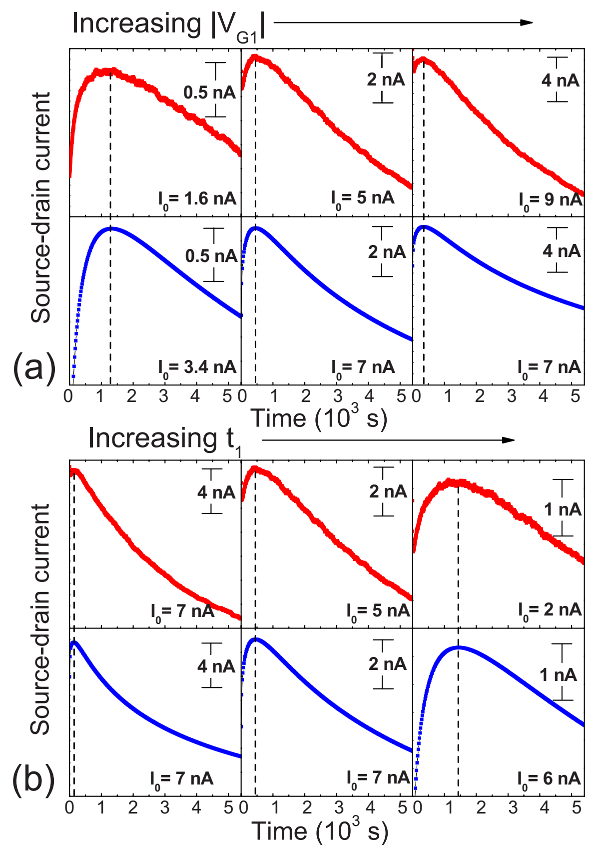

FIG. 3. (Color online) Upper curves: Measured source-drain current I_{SD} for $V_{SD}=-3$ V as a function of time $t-t_1$ after switching. The initial gate bias is $V_{G0}=-20$ V. Lower curves: Model predictions using $\alpha=2.2$ nm^{-1} and $D=1.6\times10^{-19}$ cm^2/s as obtained in Ref. 7. Vertical dashed lines: time t_{max} for which the model predicts maximal current. Bars: current scale. The transients are displayed with an offset current I_0 that is indicated in the figures. (a) Constant switching time $t_1=900$ s and varying gate bias V_{G1} after switching: −7, −10, and −12 V (left to right). (b) Constant $V_{G1}=-10$ V and varying t_1: 300, 900, and 1800 s. The experimental curves in the middle panels of (a) and (b) are the same as in Fig. 2 for $t>t_1$.

In order to make a quantitative comparison, we show in Fig. 3 the measured and predicted current transients for different values of the prestressing time t_1 and the gate voltage V_{G1} after the prestressing time. In the calculations we have used exactly the same values of α and D as obtained in our previous work from a fit of the theoretical to the measured time-dependence of the threshold-voltage shift:[7] $\alpha=2.2$ nm^{-1} and $D=1.6\times10^{-19}$ cm^2/s. We obtain the predicted current transients as follows. First, we find the hole concentration in the accumulation layer by solving a one-dimensional diffusion equation for the protons in the SiO_2 with the boundary condition Eq. (1), under the requirement that the total charge (holes+protons) is constant. Next, we translate the hole concentration into a time-dependent threshold-voltage shift and use the transfer curves from Ref. 7 to obtain the current transient. We note that in this procedure the lateral inhomogeneity of the hole density in the accumulation layer due to the finite source-drain voltage $V_{SD}=-3$ V is neglected.

In Fig. 3(a) a gate bias $V_{G0}=-20$ V is applied for a fixed prestressing time $t_1=900$ s, after which the gate bias is stepped to three different values of V_{G1}, while in Fig. 3(b) the initial gate bias $V_{G0}=-20$ V and the final gate bias $V_{G1}=-10$ V are kept fixed and three different values of the prestressing time t_1 are taken. The agreement between the experimental and predicted transients is striking. We show the experimental and theoretical transients with different offset currents I_0, which roughly compensates for the above mentioned neglect of inhomogeneity. We checked that the times t_{max} at which the peaks appear are highly insensitive to the particular value of V_{SD}. The agreement between the experimental values of t_{max} and the theoretical predictions is excellent. We note that this agreement is obtained without introducing any other parameter than the parameters α and D obtained in our work on the bias-stress effect.[7]

Summarizing, we predicted the occurrence of anomalous nonmonotonic current transients in *p*-type organic transistors for a time-varying gate bias, where after prestressing with a strongly negative gate bias the bias is stepped to a less negative voltage. During prestressing, protons produced in the semiconductor from holes and water diffuse into the gate dielectric. After the step in the bias, these protons diffuse back to the semiconductor, where they are reconverted into holes. This leads to a temporal increase in the number of holes and the transistor current. The occurrence of the resulting nonmonotonic current transients was verified experimentally. The measured current transients accurately follow the model predictions, obtained using parameters from the modeling of the bias-stress effect. We consider the quantitative prediction and the experimental verification of these quite unexpected results as an important step forward in the understanding of the operational instabilities occurring in organic transistors.

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