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Charge Trapping at the Dielectric of Organic Transistors Visualized in Real Time and Space**

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Recently the commercialization of the first reflective organic displays employing organic field-effect transistors (OFETs) used for on–off switching of pixels was announced. These new electrophoretic displays are bistable and have low power consumption. Future, emissive, organic light-emitting displays (OLEDs), however, will operate at high powers and then reliability and excellent long-term stability OFETs will be crucial for stable operation. Unfortunately, OFETs commonly suffer significantly from gate-bias stress under ambient conditions that, over time, causes a detrimental shift in the voltage that the device requires to switch. This threshold-voltage shift limits the exploitation of the full potential of organic semiconductors and OFETs in low-cost, large-area, flexible applications. As an example, using current technologies OLEDs would require up to four driving OFETs per pixel to compensate for the threshold voltage shift in the transistors.[1] This demonstrates the urgency for a proper understanding of the stressing mechanism.

In practice, OFETs are hybrid material devices that consist of metallic contacts, an inorganic gate dielectric, and an organic semiconductor. Silicon dioxide is commonly used as the gate dielectric. Although the top layer of SiO_2 is known to contain trap sites for charge carriers,[2] it is presently not clear if these traps are related to the bias-stress effect, and, if so, how this is affected by environmental conditions such as humidity.[3–9]

In this Communication, the dynamics of trapping and detrapping of charges on bare SiO_2 are visualized in real time and space using scanning Kelvin probe microscopy (SKPM) and compared to the bias-stressing dynamics of an organic field-effect transistor using a SiO_2 dielectric. The results clearly show that the generally observed gate-bias stress effect in OFETs is due to water-related charge trapping at the SiO_2 surface, rather than to trapping in the organic semiconductor itself. This insight rationalizes previous results[3–9] and gives credence to the argument that the surface of the inorganic gate dielectric determines the reliability of organic transistors. We further explain why passivating the SiO_2 surface or decreasing the ambient humidity results in a significant reduction in the bias stress.

For our studies, we used a polytriarylamine (PTAA) (Merck, UK) that yields reproducible transistors with a hole mobility of 10^{-3}–10^{-2} cm^2 V^{-1} s^{-1}.[10] The chemical structure of PTAA together with a schematic picture of the cross-section of a transistor is depicted in the inset of Figure 1a. Transistors were fabricated using heavily doped p-type silicon wafers as the common gate electrode with a 200 nm thermally oxidized SiO_2 layer as the gate dielectric. Gold source and drain electrodes were defined by photolithography with a channel width and length of 2500 and 10 μm, respectively. Before depositing gold, a 10 nm titanium adhesion layer was evaporated. The substrates were exposed to a UV-ozone treatment for 10 min., followed by passivation of the SiO_2 layer with hexamethyldisilazane (HMDS). Subsequently, PTAA films with a layer thickness of 80 nm were deposited by spin coating from toluene.

In order to test the reliability of the prepared organic field-effect transistors, the influence of a prolonged gate bias on the drain current was investigated in ambient conditions by applying a gate bias of –20 V for 27 h. The gate bias was interrupted 22 times for several seconds to record the transfer characteristics of the transistor (Fig. 1a) at a drain bias of –9 V by sweeping the gate bias from +20 V to –35 V, while the source electrode was grounded. Figure 1a shows that the transfer curves shift with stress time, t, in the direction of the applied gate bias but that the shape of the transfer curves is more or less constant, in correspondence with shifts observed earlier.[8] Hence, the main effect of gate-bias stress is a shift of the threshold voltage, V_{th}, which is empirically defined as the intercept of the extrapolated transfer curve with the voltage axis. The threshold voltage shift as a function of time is presented in Figure 1b.

The threshold voltage shift, ΔV_{th}, can be attributed to trapped charges. At a trap surface density of N_{tr}, the thresh-

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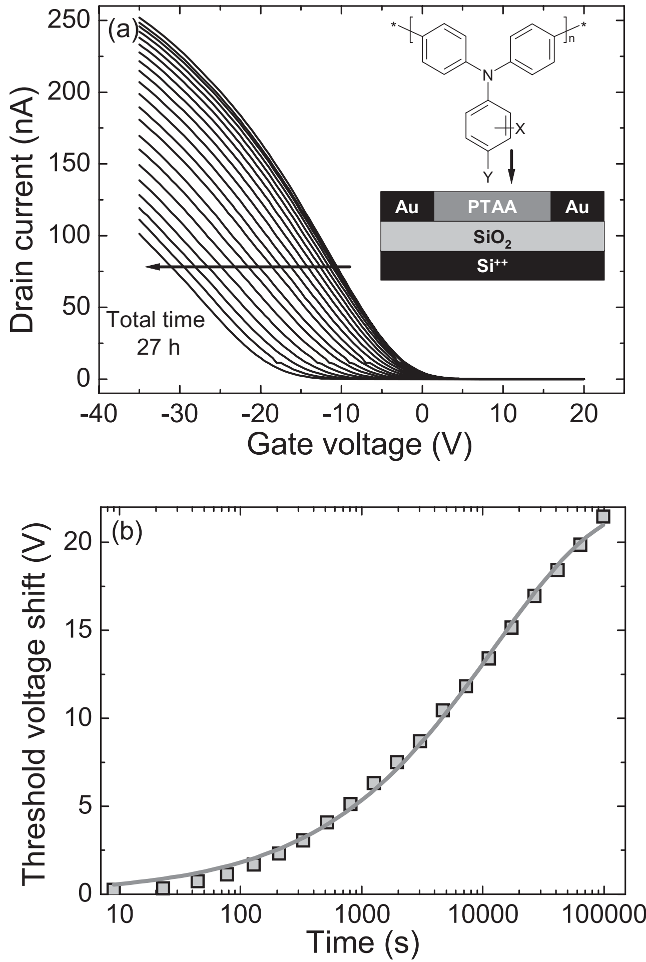

Figure 1. a) Drain current as a function of the applied gate bias for increasing stress time. The gate bias during stress was –20 V and the temperature 20 °C. The inset shows the schematic cross-section of the transistor and the chemical structure of polytriarylamine, where *X* and *Y* are short alkyl side chains. b) The threshold voltages obtained from (a) presented as a function of time on a logarithmic scale. The fully drawn curve is a fit with a stretched-exponential time dependence.

old-voltage shift is given by $\Delta V_{th} = eN_{tr}/C_{ox}$ where C_{ox} is the capacitance of the gate dielectric and e is the elementary charge. The rate at which the charges are trapped depends on the free-carrier density N_f and is usually modeled with a time-dependent diffusion constant, $D(t) = D_0(\omega t)^{-a}$, in which ω is an attempt-to-escape frequency and a a dispersion parameter.[11] The change of the carrier density from equilibrium is then described by

$$dN_f/dt = -AD(t)N_f \quad (1)$$

where A is a prefactor that is proportional to a capture cross-section for the charge carriers.[11] Solving Equation 1 using the definition for threshold voltage shift results in a stretched-exponential time dependence[11]

$$\Delta V_{th}(t)/V_0 = 1 - N_f(t)/N_f(0) = 1 - \exp(-(t/\tau)^{\beta}) \quad (2)$$

where t is a characteristic time constant, the dispersion parameter $\beta = 1 - \alpha = T/T_0$. T is the absolute temperature and $k_B T_0$ is the characteristic width of the distribution of trap sites (k_B is Boltzmann's constant). The prefactor V_0 is equivalent to $V_{th}(t = \infty) - V_{th}(t = 0)$, in which $V_{th}(t = \infty)$ is equal to the applied gate bias. When we fit the threshold-voltage shift as a function of time with the stretched exponential in Figure 1b, a good agreement is found with $\tau = 10^4$ s and $\beta = 0.5$. Recently, we have shown that for these bottom-gate organic transistors with a SiO_2 dielectric, τ is thermally activated with an activation energy of 0.6 eV that is virtually independent of the semiconductor used.[8] Although the stretched-exponential formalism gives a proper way to compare different OFETs, a satisfying explanation for the mechanism that causes the – material independent – threshold voltage shift is lacking. It has been suggested that water[3,5,7–9] or hydroxyl groups at the surface[2,4] are the origin of the threshold-voltage shift that is induced by the gate-bias stress.

To resolve this issue, SKPM was performed on the same OFET devices, but without using the organic semiconductor layer. The device layout is depicted in the inset of Figure 2a. Because this device does not have an active layer, usual transport measurements cannot be performed but SKPM allows vs to study the potential profile at the SiO_2 gate dielectric while biases are applied to the electrodes.[12,13] In the actual experiment, first a height profile was recorded with tapping-mode atomic force microscopy (AFM), followed by a second pass during which the potential profile was measured at a lift height of 50 nm above the surface. The absolute values for the measured potentials depend on the capacitive coupling between the AFM probe and the entire investigated device that leads to a small offset between the reference source and drain contacts. A simple scaling was performed to correct for the deviation in the observed surface-potential difference between the source and drain electrodes from the applied bias.[14]

Figure 2b shows the potential profile that was obtained when a +10 V bias was applied to the drain electrode while the source and gate electrodes were grounded. As expected, SKPM reveals a surface potential of 0 V above the source electrode (left) and the SiO_2 dielectric (middle), and on the drain electrode the surface potential is approximately +10 V. However, as a function of time, the potential profile becomes less square, indicating that charges enter the area between the electrodes, that is, the SiO_2 gate dielectric. This effect is present for charges of both polarities on similar timescales, as indicated by the inset of Figure 2b. Here the potential profiles as a function of time are shown when the source and gate are grounded and the potential of the drain is –10 V. The polarity-independent effect is remarkable, because hole and electron trapping on SiO_2 are expected to be quite different from each other. SiO_2 is known to trap electrons rather than holes.[2] The similar timescales might indicate that 1) both charge carriers are trapped at a transporter (i.e., an ion or water itself) of which the movement across the surface is the time-limiting factor, or 2) only one type of carrier, presumably the hole, is

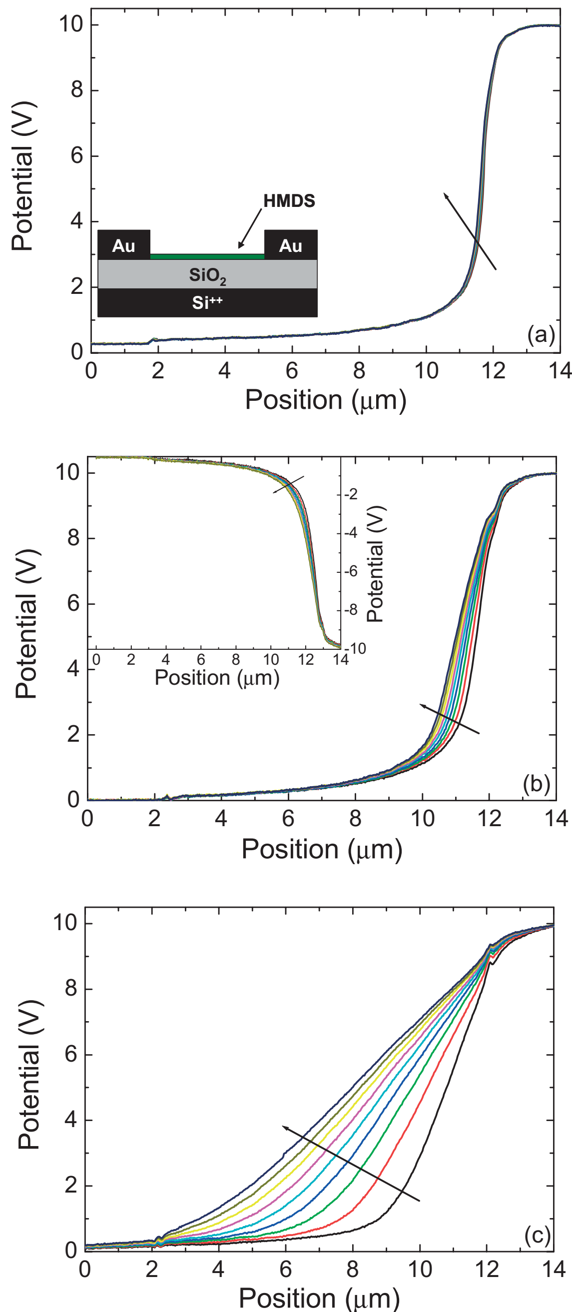

Figure 2. Potential profiles as a function of time for substrates with different HMDS coverage. The applied bias on the drain (right) electrode is 10 V, the source and gate electrodes are grounded. The time step between each curve is 6 s. The contact angle of the surface with respect to water of a), b), and c) is 70°, 60°, and 40°, respectively. The inset of (a) shows the cross-section of the device layout used, the inset of (b) shows the potential profiles when –10 V is applied to the drain electrode and 0 V to source and gate electrode.

trapped reversibly and at zero drain voltage its charge density is compensated by an equal charge density of the other, irreversibly trapped, type of carrier, presumably the electrons. In the latter case, we probe the movement of a carrier with one specific polarity. This might explain the similar timescales observed.

To verify if the charges are at, rather than below, the SiO_2 surface, the surface of the SiO_2 was covered with different surface concentrations of HMDS. HMDS binds to the OH groups present at the SiO_2 surface and reduces the concentration of OH groups at that surface. The coverage, or degree of silylation, can be controlled by the time of the HMDS vapor exposure. With increasing silylation, the surface becomes more hydrophobic, as evidenced by a large water contact angle.[15,16] The surface potential profiles of three substrates with water contact angles of 70°, 60°, and 40° are shown in Figure 2a–c, respectively. These contact angles represent HMDS coverage of approximately 53, 42, and 14 % as measured with high-sensitivity low-energy ion scattering.[17] With decreasing contact angle, there is an increase in the rate at which the potential profile changes is observed. This indicates that charges are indeed present on the surface of SiO_2 and that their mobility can be reduced by passivating the surface. Silylation lowers the density of available sites, thereby reducing the ability of the charges to move along the SiO_2 surface, which is in agreement with surface conductivity measurements on surface-modified SiO_2.[18] It is worthwhile to note that functionalization of the SiO_2 also changes the local surface work function as measured with SKPM. With increasing HMDS coverage, an increase of the surface potential was observed before applying a bias. This is observed as an increasing step with increasing HMDS coverage at 2 μm in Figure 2a–c.

To study the time dependence of the charge movement, the relaxation process of the trapped charges was measured by stressing the devices with +10 V on the drain for 1 min and then grounding all contacts. The resulting potential profiles are presented in Figure 3a–c, again for the substrates with contact angles of 70°, 60°, and 40°, respectively. Comparison of the potential profiles reveals that immediately after stressing most charges are present in the device with the lowest HMDS coverage, as inferred from the higher and broader distribution of the surface potential. After the contacts were grounded, a decrease of the surface potential as a function of time is observed in agreement with experiments on CdSe.[19] Again, we observe that lower HMDS coverage results in a faster relaxation process.

The total number of trapped charges is, in first order, proportional to the integral of the measured potential.[20] In Figure 4, the number of trapped charges, that is, the integral of the curves of Figure 3a–c, is plotted as a function of time. The time dependence of the decrease in the number of trapped charges can be described with the stretched-exponential time relation of Equation 2. A perfect fit is obtained for all three HMDS coverages. The typical time constant τ increases with the coverage of HMDS, in agreement with the observation of a slower relaxation process. With β we observe an increase with decreasing HMDS coverage. Remarkably, the values of β are comparable to the ones found in the gate-bias stress of the OFET in Figure 1 that was made on using a similar

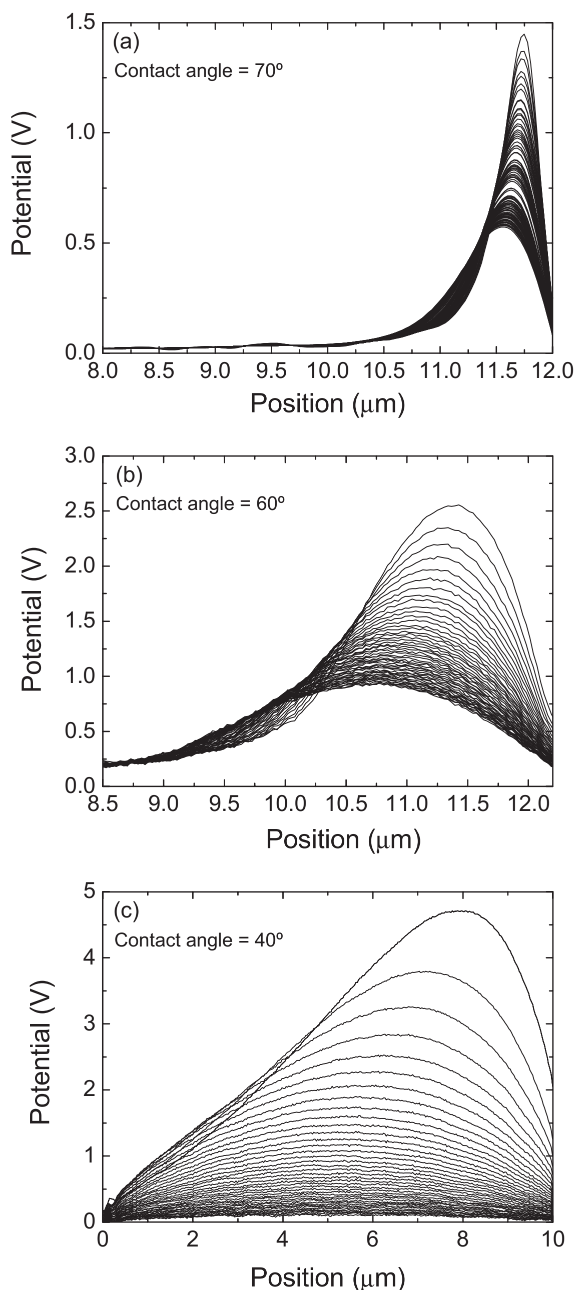

Figure 3. Potential profiles as a function of time for substrates with different HMDS coverage after 10 V was applied to the drain electrode for 1 min. During this measurement all electrodes were grounded. The time step between each curve is 6 s. The contact angle of the surface with respect to water of a), b), and c) is again 70°, 60°, and 40°, respectively.

substrate. This strongly suggests a common origin of both phenomena.

The decreasing amount of injected charges during stress upon increasing the silylation of the surface suggests that the generally observed bias-stress effect in OFETs is due to charge trapping at the SiO_2 surface. To verify if water has a role in the charge trapping, we decreased the water content of the ambient atmosphere by purging with dry N_2 gas. Under

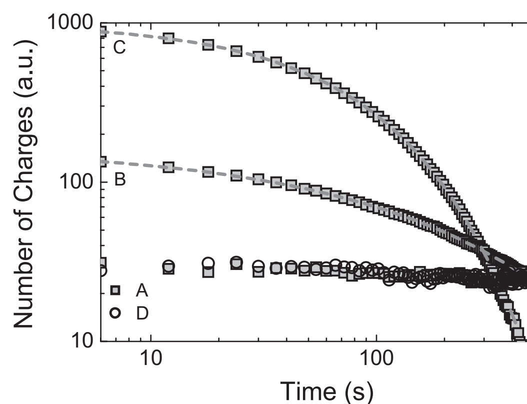

Figure 4. Squares: the total number of trapped charges, i.e., the integral of the curves of Figure 3a–c, as a function of time measured at a humidity of 40 % (indicated by A, B, and C, respectively). Dashed lines: fits with a stretched-exponential time dependence. The values for t and β, respectively, are 70 s and 0.8 for B, and 131 s and 0.5 for C. The fit of A is not unique because of the limited variation of the total number of charges as a function of time. Open circles (D): measurements of the sample with a contact angle of 40°, but measured at a lower humidity (13 %).

these conditions, the number of trapped charges is dramatically reduced and their kinetics are slowed down significantly, as shown by the open circles in Figure 4. Interestingly, we can exactly reproduce the behavior of the 40°-contact-angle sample with the 70°-contact-angle sample by only decreasing the relative humidity from approximately 40 % (ambient) to 13 %. It seems therefore that silylation and humidity act, with opposite effects, on the same trap. Hence, both the silylation and humidity dependence are in qualitative agreement with the stress measurements on OFETs in air and in vacuum, where the values for β are 0.5 and 0.3, respectively.[8] Although the actual microscopic mechanism for this change in β is not clear, this might suggest that the width of the trap distribution changes or that we probe a smaller section of the same distribution. The dependence of the gate-bias-stress-induced threshold-voltage shift on the humidity was also reported by Gomes et al.[7]

So far, we have argued that the bias stress in actual OFETs is likely to be caused by traps on the SiO_2 surface, whose filling with charges is imaged by SKPM. Indeed, the dispersion parameter β, reflecting the width of the involved trap distribution, is very similar in the two experiments. However, the time scales of the experiments, represented by the parameter τ, are different. This should not come as a surprise since in the SKPM experiment the carriers are injected from a metal contact, whereas in the OFET the accumulation layer is believed to act as the charge reservoir.

To explain the threshold-voltage shift in amorphous silicon field-effect transistors, Crandall has proposed a two-level rate-equation model for defect relaxation.[21] Crandall showed that when the two levels are exponentially distributed in energy, the time dependence of the transition from the mobile state to the trapped state follows a stretched-exponential time relation. Therefore this model provides a rationalization of

the observed threshold-voltage shift when we assume that in the OFET the charge carriers can be in a mobile state in the polymer or in a water-induced trap state at the SiO_2 surface. The two-level model for the OFETs is supported by previous temperature dependent measurements that show that these levels are separated by an average energy barrier of 0.6 eV.[8]

In conclusion, our experiments reveal that the gate-bias-induced threshold-voltage shift of an OFET under ambient conditions follows a similar stretched exponential time dependence as the trapping of charges at the dielectric layer of a FET device *without* the organic semiconductor. The charge trapping occurring in the SiO_2 top layer sheds new light on previously reported results. First, it explains that the activation energy of the threshold-voltage shift does not depend on the particular semiconducting polymer that is used.[8] Second, the influence of water on the gate-bias stress[5,7,9] can now also be explained as an increase in trap site density on the SiO_2 surface. Our conclusion that the gate-bias-induced threshold-voltage shift is due to traps at the SiO_2 substrate surface is further supported by the fact that this effect is reduced when a layer of poly(α-methylstyrene) is placed between the SiO_2 and the active layer.[4] In this case, the presence of a spatial barrier between the mobile charge carriers and the traps results in a much longer time scale for the threshold voltage shift dynamics. In combination with the SKPM measurements presented in this paper, all observations above clearly demonstrate that the generally observed bias-stress effect in OFETs is related to water-related charge trapping at the SiO_2 surface.

Experimental

Field-effect transistors were fabricated using heavily doped p-type Si wafers as the common gate electrode with a 200 nm thermally oxidized SiO_2 layer as the gate dielectric. Using conventional photolithography, gold source and drain electrodes were defined in a bottom-contact device configuration with channel width and length of 2500 and 10 μm, respectively. A 10 nm layer of titanium was used as an adhesion layer for the gold on SiO_2. The SiO_2 layer was treated with the primer hexamethyldisilazane (HMDS) prior to semiconductor deposition in order to passivate its surface. Polytriarylamine (PTAA) films were spun from a 1 % toluene solution at 2000 rpm. for 20 s resulting in a film thickness of approximately 80 nm. A different coverage of HMDS was obtained by exposing a SiO_2 substrate to a HMDS vapor for different lengths of time.

SKPM measurements were performed with a Veeco Dimension 3100 AFM operated in ambient and in a nitrogen environment. First, the height profile was recorded in tapping mode. Then the potential profiles were measured in non-contact lift mode at a distance of 25 nm from the surface. The internal voltage sources of the AFM were used to apply the biases to the electrodes.

The results presented in this paper were obtained using three different samples, containing four transistors each, on which repeated measurements were performed. The transistors on each substrate, containing an equal HMDS coverage, showed, under equal humidity conditions, identical characteristics.

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