Scalable general high voltage MOSFET model including quasi-saturation and self-heating effects

Yogesh Singh Chauhan [a,*], Costin Anghel [a], Francois Krummenacher [a], Christian Maier [b], Renaud Gillon [c], Benoit Bakeroot [d], Bart Desoete [c], Steven Frere [c], Andre Baguenier Desormeaux [e], Abhinav Sharma [a], Michel Declercq [a], Adrian Mihai Ionescu [a]

[a] *Electronics Laboratory (LEG), Institute of Microelectronics and Microsystems (IMM), Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015, Lausanne, Switzerland*
[b] *Robert Bosch, Reutlingen, Germany*
[c] *AMI Semiconductor (AMIS), Oudenaarde, Belgium*
[d] *University of Gent, Gent, Belgium*
[e] *Cadence Design Systems, Paris, France*

1. Introduction

The interest in the high voltage devices has dramatically increased as these devices were integrated with the low power modules in MOS technology. The accurate compact modeling of high voltage (HV) MOS transistors has always been a great challenge in the device modeling community. This is due to the fact that the charges and field associated with the drift region and intrinsic MOS have very complex dependence on the external terminal biases owing to the asymmetric device architecture. Though many groups around the world have attempted to model the different architectures of HV MOS transistors using different approaches, most of these are sub-circuit models. To the best of our knowledge, in the literature, there is no available compact *general* HV MOS model (i.e. a single model

* Corresponding author. Tel.: +41 21 693 4604; fax: +41 21 693 3640.
E-mail addresses: yogeshsingh.chauhan@epfl.ch (Y.S. Chauhan), christian.maier@de.bosch.com (C. Maier), renaud.gillon@amis.com (R. Gillon), benoit.bakeroot@elis.ugent.be (B. Bakeroot), andreb@cadence.com (A.B. Desormeaux), adrian.ionescu@epfl.ch (A.M. Ionescu).

for any HV MOS device e.g. LDMOS and VDMOS) capable of combining the accuracy, speed, scalability for both DC and AC domains.

Acceptable simulation accuracy is obtained by the use of adopted macro-models based on conventional low voltage modules [1,2], but these macro-models are not physical and do not take into account the special phenomena of HV devices. Some compact models have also been reported in the literature with better accuracy [3–10]. Halleweyen et al. [3] and Aarts et al. [8] reported surface potential based LDMOS models but only for DC operations. Previously Aarts et al. [7] reported a physical LDMOS model for both DC and AC operations, however scalability of the model has not been shown. Other models reported in the literature show reasonable accuracy in DC operation [4–6, 9,10], but do not show model validity for AC operation under different biasing conditions and model scalability especially with temperature, drift length and number of fingers.

A modeling strategy for HV MOS transistors based on the scalable drift resistance [11,12] and the use of EKV2.6 MOSFET model [13] as a core for the intrinsic MOS channel is presented. The strategy is optimized according to the fast convergence and good accuracy criteria. The model is stable and robust in the entire bias range useful for circuit design purpose. An important aspect of this *general* model is the scalability of the model with physical and electrical parameters along with the correct modeling of quasi-saturation and self-heating effect. Most of the transistor characteristics and scalability is validated on VDMOS device [14]. The model is also validated on LDMOS device [15] especially for the scalability with width and voltage handling capability (i.e. scalability for drift length).

2. General drift resistance model

Fig. 1(a) and (b) show the schematics of high voltage VDMOS and LDMOS devices respectively. Even though here we are showing simple device architectures in Fig. 1, the model can be used, as described earlier for any HV device which uses extended drift region to handle the high voltage applied at the drain node e.g. LDMOS with thin or thick oxide etc.

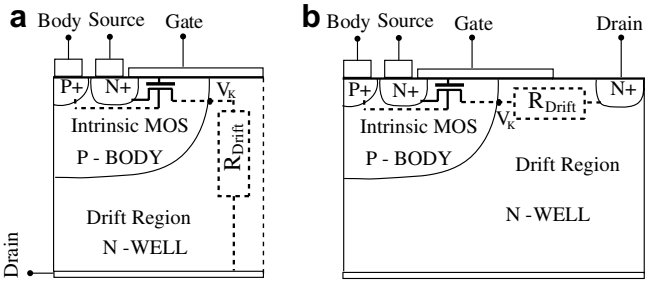

Fig. 1. Schematic representation of high voltage (a) Vertical DMOS (VDMOS) and (b) Lateral DMOS (LDMOS) device Architecture.

It has been shown in the literature that the intrinsic drain voltage (V_K) always remains at low values for entire bias domain [16]. Based on this concept, we consider our device divided into an intrinsic MOSFET region and a drift region, where the intrinsic transistor part is modeled by using low voltage EKV model [13] described in the next section while modeling of drift region is carried out by using bias dependent resistance explained below.

As mentioned earlier, the motivation to use a resistance to model the drift region is to get the fast convergence along with excellent accuracy. The simplest resistance expression could be a constant resistance. Fig. 2 shows the transfer characteristics (I_D–V_G) using constant resistance (dash lines) as drift resistance. It can be seen that the constant resistance accurately models the low drain and low to medium gate bias behavior, as at low drain bias, the intrinsic transistor drives the current while the drift region behaves like a constant resistor. Another interesting remark is that the fixed resistance cannot model the behavior of the device at low V_D, when high gate voltage is applied. The explanation for this deviation comes from the accumulation charge sheet, which extends into the drift region with the increase of the gate voltage and lowers the resistance of the drift part. In order to simulate the above described effect, a slight reduction of the drift resistance with the gate voltage is introduced in the model:

$$R_{\mathrm{Drift}} = \frac{R}{1 + \theta_{\mathrm{Acc}} \cdot \mid V_G \mid} \tag{1}$$

where R is the constant resistance, θ_{Acc} is the gate bias modulation parameter (effect of accumulation charge sheet on R_{Drift}) and V_G is the applied gate voltage. The value of R can be obtained by extracting the silicon resistivity and then calculating the global resistance function of the geo-

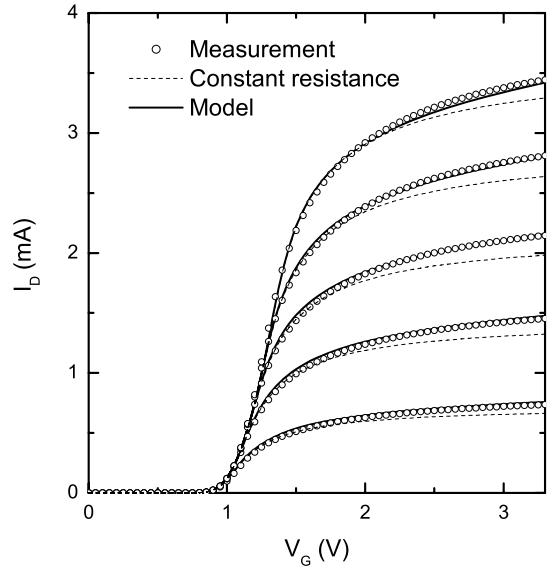

Fig. 2. I_D vs. V_G for $V_D = 0.1$–0.5 V for 50 V VDMOS transistor. The constant resistance along with the accumulation charge sheet effect provides excellent accuracy at low drain bias.

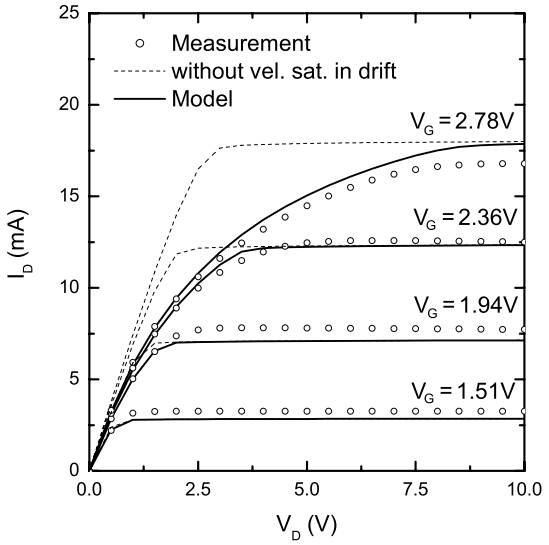

Fig. 3. I_D vs. V_D for 50 V VDMOS transistor. The modeling of velocity saturation effect on drift resistance provides good behavior in the linear region.

metrical dimensions, if the doping concentration of the drift zone is known. The model behavior using (1) is shown in Fig. 2 by solid lines. It can be observed that the matching between the simulation and measured data is excellent. Thus, it can be concluded that (1) correctly reproduces the physics inside the device. Moreover, this expression proves to be highly efficient in terms of implementation as it uses the simplest representation and the minimum number of parameters for the description of the physical phenomenon at low gate and drain bias. Fig. 3 shows the I_D–V_D characteristics using drift resistance derived above by dash lines. It is easily observable that even though above derived expression showed excellent characteristics at low V_D, it is not working well at higher V_D. It is also important to mention that once the current saturates in the intrinsic MOS transistor, the drift part has no influence on the current. Consequently, the drift part only affects the linear regime of the output characteristics. Although, this influence seems to be limited, the transition from linear to saturation is very sensitive to the drift resistance variation. The delayed transition between linear and saturation regime at high gate voltages occurs due to the carrier velocity saturation in the drift and is equivalent to an increase in the resistance of the drift region. In literature, the carrier velocity saturation effect on the current is modeled using hyperbolic dependence of the electric field across the region. It means that this dependence would be linear for the resistance. Thus, in order to simulate the carrier velocity saturation dependence using the drift resistance expression, a direct dependence on the field applied in the drift region is introduced as:

$$R_{\mathrm{Drift}} = R \cdot \left[\frac{1 + \left(\frac{V_D - V_K}{\mathrm{VSAT}}\right)^{\alpha_{\mathrm{vsat}}}}{1 + \theta_{\mathrm{Acc}} \cdot |V_G|}\right] \tag{2}$$

where VSAT and α_{vsat} are the velocity saturation parameters. The mobility is considered constant all over the current path and the electric field uniformly distributed along the length of the drift region. Solid lines in Fig. 3 show the drain current using (2), which proves that this expression takes into account major physical phenomena in the drift region.

The final expression for drift resistance including geometry and temperature effects can be written as [11,12]:

$$\begin{aligned} R_{\mathrm{Drift}} = R_{\mathrm{Drift0}} \cdot & \left[\frac{1 + \left(\frac{V_D - V_K}{\mathrm{VSAT}}\right)^{\alpha_{\mathrm{vsat}}}}{1 + \theta_{\mathrm{Acc}} \cdot |V_G|}\right] \\ & \cdot \left[1 \pm (k_{rd} - 1) \cdot \left(\frac{N_F - 1}{N_F + N_{\mathrm{CRIT}}}\right)\right] \\ & \cdot (1 + \alpha_T \cdot \Delta T), \end{aligned} \tag{3}$$

where R_{Drift0} is the value of the drift resistance at low bias voltage defined as

$$R_{\mathrm{Drift0}} = \rho_{\mathrm{Drift}} \cdot \left[\frac{L_{\mathrm{DR}}}{(W + \Delta W) \cdot N_F}\right]. \tag{4}$$

Where ρ_{Drift} is the resistivity per unit length at room temperature ($T = 300$ K). L_{DR}, W, ΔW and N_F represent the drift length, width, width offset and number of fingers respectively. N_{CRIT} and k_{rd} are the parameters for drift scaling with number of fingers. The "+" sign is used for drain-on-side devices while "−" sign is used for drain-all-around devices. α_T is the temperature coefficient of the drift region and ΔT is the difference in ambient temperature with normal room temperature ($T = 300$ K). The effect of temperature variation due to self-heating effect is not taken into account in the drift resistance as self-heating generally occurs at high V_D. Another reason for this is to remove any problem of ill-convergence as self-heating effect adds iterations in the simulation.

3. Charge evaluation based on EKV model and current backtracking

The main reason behind using EKV MOSFET model [13] for intrinsic channel is that EKV model has physical expression for current and charges, which are continuous from weak to moderate to strong inversion. Another important characteristic of EKV model is that compared with other existing MOS models (e.g. BSIM), it uses less number of parameters which are all physical. The drain-to-source current (V_K to V_S in our model) in EKV model is given as

$$I_{KS} = I_S(i_f - i_r) \tag{5}$$

where I_S is the specific current [13] defined as

$$\begin{aligned} & I_S = 2 \cdot n \cdot \beta \cdot U_T^2, \quad n = \frac{1}{1 - \frac{\gamma}{2 \cdot \sqrt{V_G - V_T + \left(\frac{\gamma}{2} + \sqrt{\psi_0}\right)^2}}}, \\ & \psi_0 = 2\phi_F + \text{several } U_T, \quad \beta = \mu \cdot C_{ox} \cdot \frac{W}{L} \end{aligned} \tag{6}$$

where $U_T = \frac{kT}{q}$ is the thermal voltage, n is the slope factor, V_T is the threshold voltage, γ is the body effect parameter and, C_{ox} is the oxide capacitance per unit area. The normalized forward current i_f and normalized reverse current i_r are defined as

$$i_f = \left[\ln\left(1 + e^{\frac{v_p - v_s}{2}}\right)\right]^2, \tag{7}$$

and

$$i_r = \left[\ln\left(1 + e^{\frac{v_p - v_k}{2}}\right)\right]^2, \tag{8}$$

where $v_p = \frac{V_P}{U_T}, v_s = \frac{V_S}{U_T}, v_k = \frac{V_K}{U_T}$ are the normalized pinch-off ($V_P = \frac{V_G - V_T}{n}$), source and intrinsic drain voltage respectively [13].

The total gate charge is the sum of the charges related to intrinsic-drain (V_K), source, body and drift. The charges associated with the intrinsic MOS are directly obtained from EKV model [13].

The R_{Drift} expression (3) used above for current modeling does not provide the correct behavior for intrinsic drain voltage (V_K) at low-gate/high-drain biases, as this resistance in actual case should rise to Giga-ohm at low-gate/high-drain biases. The preceding statement is verified by the fact that at low gate bias, the drift region is in depletion and the current is very small. But this resistance provides accurate current prediction because at low-gate/high-drain bias (intrinsic MOS in saturation), the current is well modeled by the intrinsic MOS part. The impact of the intrinsic drain potential (V_K) on AC characteristics was shown by Hefyene et al. [17,18]. The correct V_K behavior is not only important for the peaks of capacitances which are very specific to high voltage devices, it is also extremely important for the position of the peaks with gate and drain bias. Thus it is extremely important to first obtain the correct V_K behavior with gate and drain bias. In literature, this is obtained using interpolation between V_K in the linear region and V_{Ksat} in the saturation region to limit the value of V_K to V_{Ksat} [3]. In this work, the accurate V_K value, which is used in the calculation of accumulation charge, can be obtained by backtracking of K-node charge as given below. The motivation for this strategy is to get the impact of current saturation on charge and then on V_K.

The V_K behavior which has great impact on capacitance of high voltage devices [17,18], is obtained by backtracking of K-node charge or current backtracking [19]. The normalized potential v_k is expressed as a function of v_p and q_k (normalized inversion charge density at V_K) as [19]

$$v_k = v_p - (2 \cdot q_k + \ln q_k) \tag{9}$$

where q_k is expressed as [19]

$$q_k = \sqrt{i_r + 0.25} - 0.5. \tag{10}$$

Thus V_K can be easily expressed as

$$V_K = U_T \cdot \left[v_p - \left\{2 \cdot \left(\sqrt{i_r + 0.25} - 0.5\right) + \ln\left(\sqrt{i_r + 0.25} - 0.5\right)\right\}\right] \tag{11}$$

The intrinsic drain potential (V_K) behavior obtained by this method shows excellent agreement with literature [20] (see Figs. 4 and 5). The unique behavior of V_K can be explained by considering the variation of the channel and drift resistance with bias. Initially as V_G increases, most of the drain voltage drop occurs across intrinsic MOS channel as channel resistance is very high compared to drift resistance. With increasing V_G, channel resistance drops

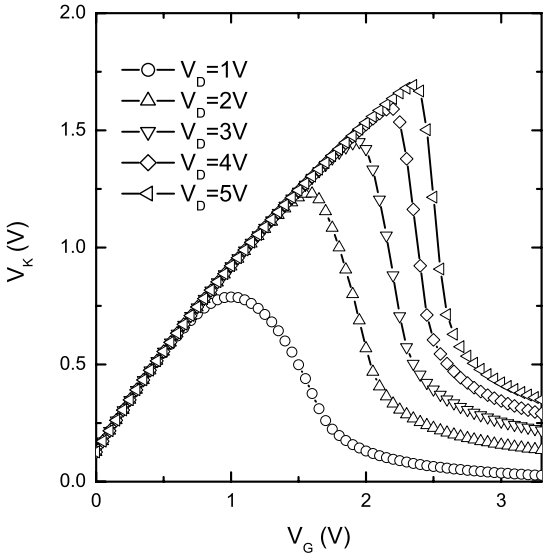

Fig. 4. Intrinsic-drain potential V_K vs. V_G for $V_D = 1$–5 V in steps of 1 V for VDMOS transistor. The decrease in V_K is caused by drift region.

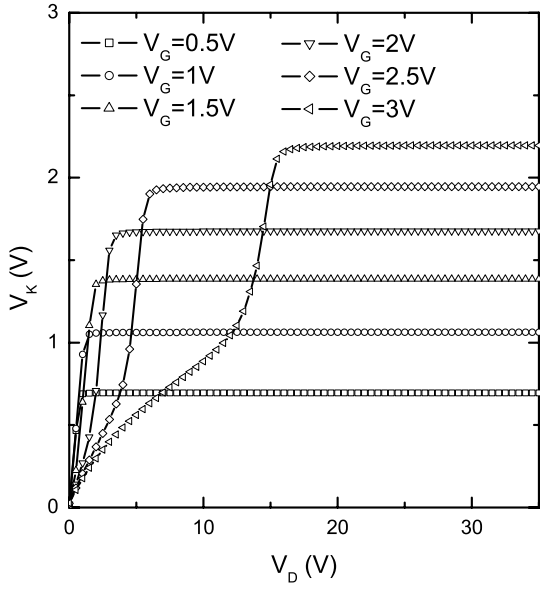

Fig. 5. Intrinsic-drain potential V_K vs. V_D for $V_G = 0.5$–3 V in steps of 0.5 V for VDMOS transistor.

sharply compared with drift resistance and at some bias condition, channel resistance becomes equal to drift resistance. This is the point where peak of V_K occurs on V_K–V_G characteristics (see Fig. 4). If V_G keeps on increasing after this point, V_K keeps on decreasing as drift resistance now dominates compared to channel resistance. This same explanation can be easily associated with V_K–V_D characteristics also (see Fig. 5). Please note that the effect of drift resistance is observed in the linear region only (see Fig. 5). Once current saturates, V_K gets saturated to V_{KSat} and after that, any increase in the drain voltage, drops across the drift region. This has also been verified from numerical device simulation.

The normalized drift accumulation charge density can be written as

$$q_{drift} = v_g - v_{fb\_drift} - \psi_{s\_drift}. \tag{12}$$

where v_{fb_drift} is the normalized flat-band voltage of drift region and ψ_{s_drift} is the normalized surface potential in the drift region. The total drift accumulation charge is obtained by integrating the drift charge density over the gate overlap length, assuming ψ_{s_drift} varies linearly in the drift region also validated from numerical device simulation.

Thus total gate charge can be written as,

$$Q_G = Q_S + Q_K + Q_B + Q_{Drift}, \tag{13}$$

where Q_S, Q_K and Q_B are the charges related to source, intrinsic drain and body node respectively, obtained from EKV MOS model [13].

The capacitances are defined using standard method as:

$$C_{ij} = \begin{cases} -\dfrac{\delta Q_i}{\delta V_j} & i \neq j \\ +\dfrac{\delta Q_i}{\delta V_j} & i = j \end{cases}$$

4. Quasi-saturation and self-heating effect in high voltage devices

The high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact-ionization effects. In fact some of these effects (self-heating and impact-ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased. Here we will discuss origin and modeling of these effects.

4.1. Quasi-saturation effect

The quasi-saturation effect is one of the unique effect observed in HV devices. To explain the quasi-saturation effect, we will discuss the saturation mechanisms in HV devices [16] using measured characteristics of Fig. 3. The current saturation on I_D–V_D characteristics can occur due to following three mechanisms. (a) Pinch-off in the channel: This is generally observed at low V_G (see $V_G = 1.51$ V curve in Fig. 3). (b) Velocity saturation in the channel: This is generally observed at medium to high V_G (see I_D–V_D curves for $V_G = 1.94$ V, 2.36 V, 2.78 V at $V_D = 10$ V in Fig. 3). A simple way to see this effect is that when intrinsic MOS is velocity saturated, the output characteristics become equidistant for equal increase in V_G. (c) Another saturation mechanism can be given by velocity saturation in the drift while intrinsic MOS is still not saturated. Actually this cannot be called saturation as current does not get saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_G does not increase current level significantly and gate bias has small effect (see $V_G = 2.78$ V in Fig. 3). This effect is called quasi-saturation, which is generally observed at high V_G. Please note that all or any two of the three effects described above may superimpose with each other as seen in Fig. 3 and therefore they cannot be separated from each other. As our drift resistance already includes the velocity saturation in the drift, the quasi-saturation effect is easily modeled by this model.

4.2. Self-heating effect

The self-heating effect (SHE) represents the heating of the device due to its internal power dissipation. This effect appears when high levels of power are attained in the device. The dissipated heat leads to an increase in the internal temperature of the device. The internal temperature increase influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE are distributed or non-distributed models. As expected, better accuracy was obtained from distributed models, which offer a larger flexibility for the current simulation.

Still, the clear advantage of the non-distributed models over the distributed ones is the parameter extraction procedure, as non-distributed approach offers a simple and efficient representation of the problem. Fig. 6 shows the equivalent sub-circuit used for the self-heating representation. This classical representation can be used for the DC, AC or transient simulation of the device in some critical regimes (other than analog operation).

In our model, the SHE is modeled using standard circuit shown in Fig. 6, where the thermal resistance (R_{TH}) and

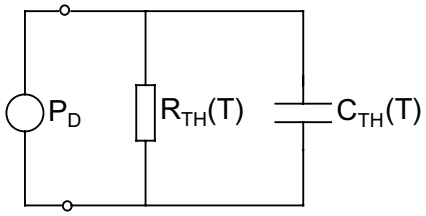

Fig. 6. Representation of the electro-thermal circuit for self-heating effect simulation (Power dissipation $P_D = I_D(V_D - V_S)$, thermal resistance $R_{TH}(T) = R_{THNOM}(1 + \alpha\Delta T)$ and thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$) [22,23].

thermal capacitance (C_{TH}) varies dynamically with the device temperature [22,23]. The extraction procedure for R_{TH} and C_{TH} has been discussed in [22,23]. The expressions for thermal resistance and capacitance from [22,23] are re-written here to complete this discussion.

The thermal resistance is expressed as [22,23]

$$R_{TH} = R_{THNOM}(T_e) \cdot [1 + \alpha \cdot (T_i - T_e)] \quad (14)$$

where T_e and T_i are the ambient and internal device temperatures, respectively and R_{THNOM} is also considered a linear function of the ambient temperature: $R_{THNOM}(T_e) = R_{THNOM}(300\ K) \cdot [1 + \alpha \cdot (T_e - 300\ K)]$. One should note that in (14), the temperature increase, $\Delta T = T_i - T_e$, at known ambient temperature is essentially given by SHE (related to the injected electrical power P_D), and consequently, R_{THNOM} could be considered as the nominal thermal resistance at zero injected power (at given ambient temperature T_e). The thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$ and temperature coefficient of thermal resistance α are extracted from I_D vs. V_D characteristics for different pulse widths τ_w [22,23].

4.3. Impact-ionization effect

When the drain bias across the device increases, the electric field in the drift region also increases as a function drain bias. In this high field zone, the longitudinal electric field varies linearly and reaches its peak value at the drain junction. The impact-ionization current (or avalanche current) can be expressed as

$$I_{avl} = (M - 1) \cdot I_D \quad (15)$$

where M is called as multiplication factor. Rossel et al. [24] developed the following approximate expression for M from impact ionization integral assuming low multiplication level.

$$M - 1 \simeq 1 - \frac{1}{M} = (2.8 \times 10^{-73}) \cdot N_{eff}^3 \cdot V_D^4 \quad (16)$$

In the model implementation, we combined the constant (2.8×10^{-73}) with N_{eff} and used a single parameter N_{EFF}. Thus multiplication factor M can be rewritten as:

$$M - 1 = N_{EFF}^3 \cdot V_D^4 \quad (17)$$

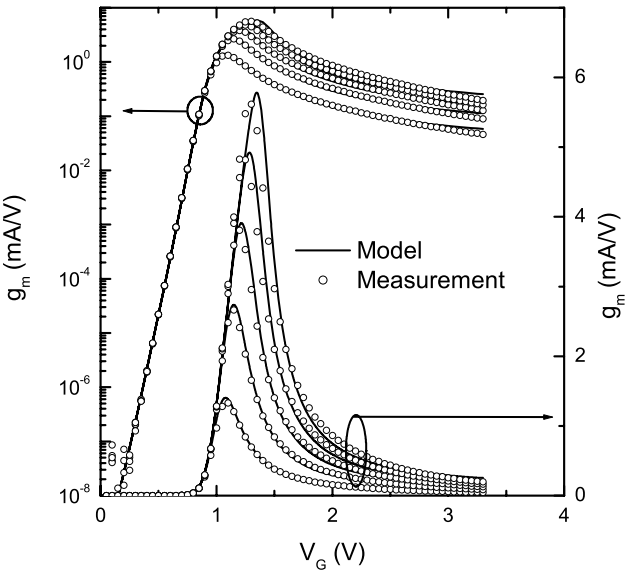

Fig. 8. Transfer characteristics at low drain bias for $W = 40\ \mu m$, $L = 0.6\ \mu m$ and $N_F = 2$ at $T = 30\ ^\circ C$: g_m–V_G for $V_D = 0.1$–$0.5\ V$ for VDMOS transistor. The sharp decrease in transconductance at higher gate bias can be explained by the dominance of drift resistance over channel resistance.

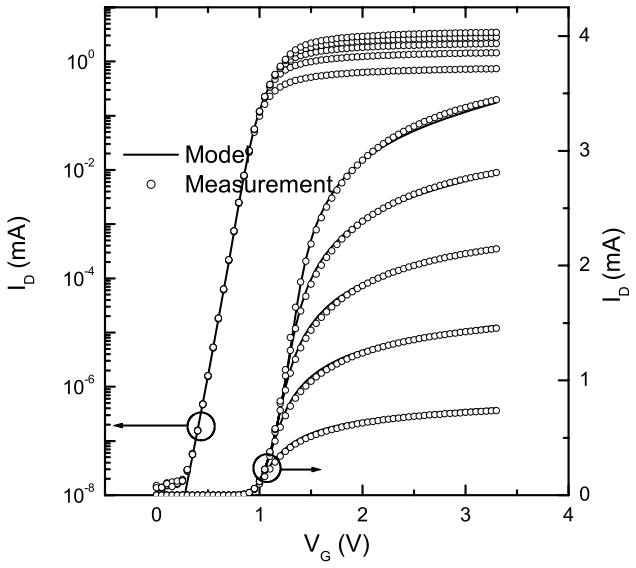

Fig. 7. Transfer characteristics at low drain bias for $W = 40\ \mu m$, $L = 0.6\ \mu m$ and $N_F = 2$ at $T = 30\ ^\circ C$: I_D–V_G for $V_D = 0.1$–$0.5\ V$ for VDMOS transistor. The current at higher V_G is heavily affected by drift region.

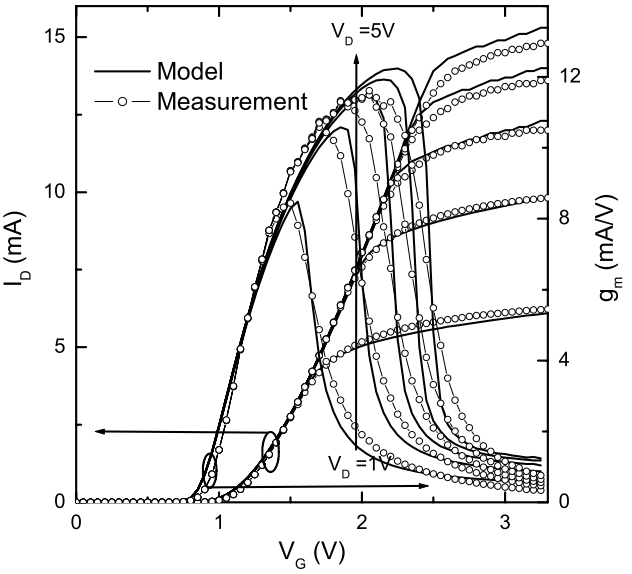

Fig. 9. Transfer characteristics at medium drain bias for $W = 40\ \mu m$, $L = 0.6\ \mu m$ and $N_F = 2$ at $T = 30\ ^\circ C$: I_D–V_G for $V_D = 1$–$5\ V$ in steps of 1 V for VDMOS transistor.

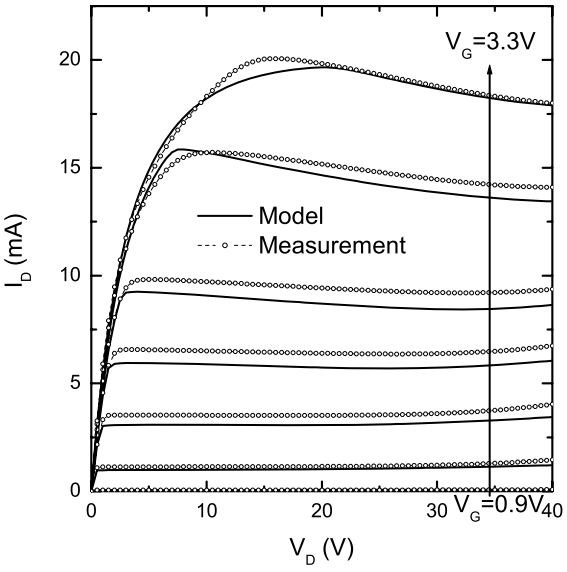

Fig. 10. Output characteristics (I_D vs. V_D) for $W = 40$ μm, $L = 0.6$ μm and $N_F = 2$ at $T = 30$ °C for VDMOS transistor. Note self-heating effect is correctly simulated. The discrepancy in the curves can be explained by the simultaneous optimization of drift resistance, self-heating effect, impact-ionization effect and velocity saturation in MOSFET at high V_D.

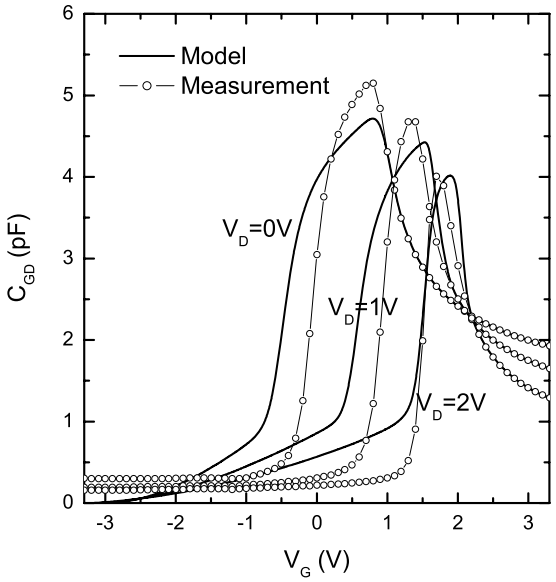

Fig. 12. Gate-to-drain capacitance C_{GD} vs. V_G for $V_D = 0$, 1 V, and 2 V for VDMOS transistor. Here C_{GD} includes the drift overlap capacitance. The sharp decrease in C_{gd} at higher V_G is heavily affected by drift region. The discrepancy in the curves is due to assumption of constant doping in the channel and simplified drift charge evaluation. The accuracy on capacitances can be improved by modeling the lateral non-uniform doping present in the intrinsic MOS channel [25].

5. Model validation and results

This model is calibrated on the measured characteristics of a 50 V VDMOS and 40 V LDMOS devices provided by AMIS and BOSCH [14,15]. The source and body are tied to avoid parasitic bipolar transistor for all measurements.

5.1. Case study 1: vertical DMOS device

The schematic representation of the VDMOS device under study is shown in Fig. 1(a). Only half of the device is considered as it is symmetric along vertical axis. Fig. 7 shows the transfer characteristics for low drain bias, which demonstrates that the model provides accurate simulation of current and subthreshold slope. From Fig. 8, it can be observed that the model not only gives accurate values of peak of transconductance and its slope in the subthreshold

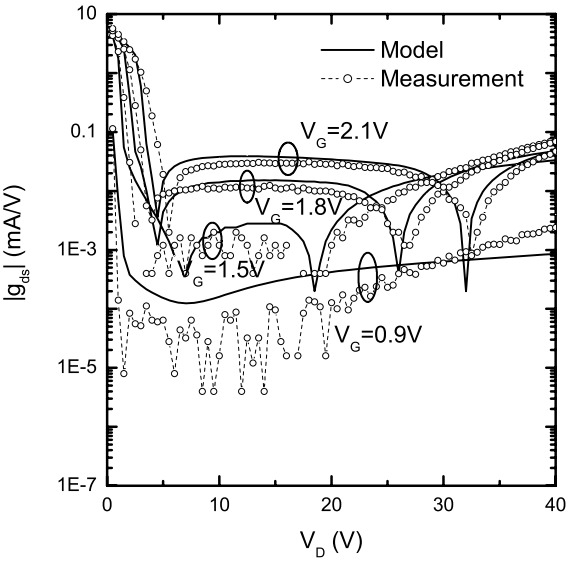

Fig. 11. Output characteristics ($|g_{ds}|$ vs. V_D) for $W = 40$ μm, $L = 0.6$ μm and $N_F = 2$ at $T = 30$ °C for VDMOS transistor. Note peaks of output-conductances are correctly matched. The first dip in $|g_{ds}|$ originates from self-heating effect while second dip is caused by impact-ionization effect.

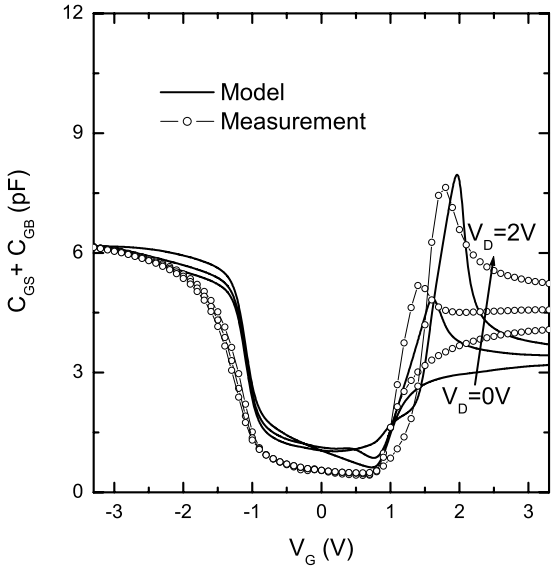

Fig. 13. Gate-to-source and gate-to-body capacitance $C_{GS} + C_{GB}$ vs. V_G for $V_D = 0$, 1 V, and 2 V for VDMOS transistor. The discrepancy in the curves is due to assumption of constant doping in the channel and simplified drift charge evaluation. The accuracy on capacitances can be improved by modeling the lateral non-uniform doping present in the intrinsic MOS channel [25].

regime but also predicts the correct behavior after the peak, which is very important in circuit design. Fig. 9 shows the transfer characteristics for medium drain bias (V_D = 1–5 V). Figs. 10 and 11 show the output characteristics and output-conductance for different gate bias respectively, which show that not only the transition from linear to saturation regime is well predicted by the model validating correct drift model, it also correctly simulates the self-heating effect in the output characteristics. The peaks of output-conductance are also well predicted by the model. Capacitances C_{GD} and $C_{GS} + C_{GB}$ obtained using this model, are shown in Figs. 12 and 13 respectively. The special behavior of the high voltage capacitances, i.e. the peaks [7,18] in C_{gd} and C_{gs} are well modeled. It can be seen that all the capacitances show good trend for the entire gate and drain bias range. It should be noted that in literature very few models have been successful in modeling the correct behavior of capacitances of HV MOS devices [1,2,7,11,12]. Furthermore the accuracy on capacitances can be improved by

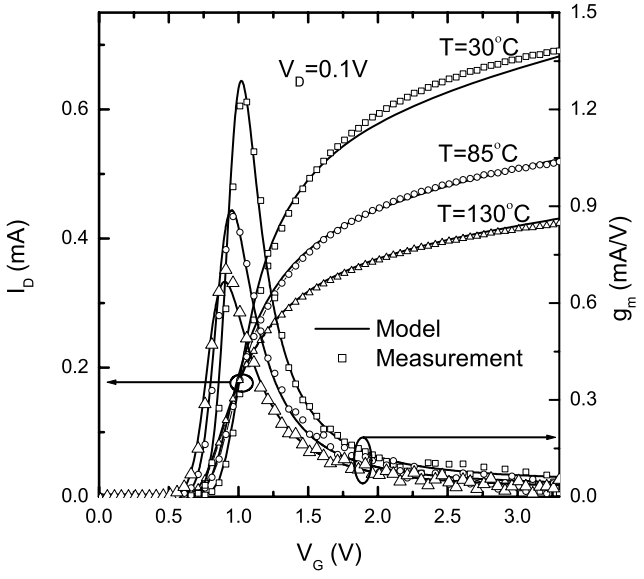

Fig. 14. Temperature scaling: I_D–V_G and g_m–V_G for $W = 40\ \mu m$, $L = 0.6\ \mu m$ and $N_F = 2$ for VDMOS transistor at $T = 30\ °C$, 85 °C and, 130 °C. Note change in threshold voltage with temperature and peak of transconductance is correctly modeled. The ZTC-point is also well simulated.

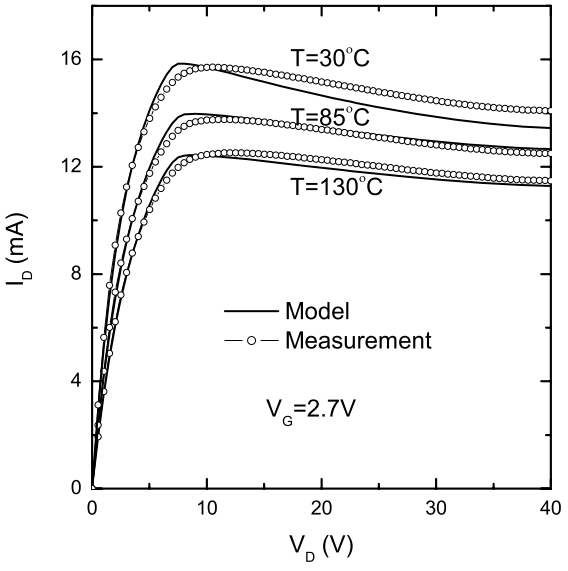

Fig. 15. Temperature scaling: I_D–V_D for $W = 40\ \mu m$, $L = 0.6\ \mu m$ and $N_F = 2$ for VDMOS transistor at $T = 30\ °C$, 85 °C and, 130 °C. Note self-heating effect is very well modeled for different temperatures. The decrease in slope in the linear region is caused by increase in drift resistance with temperature.

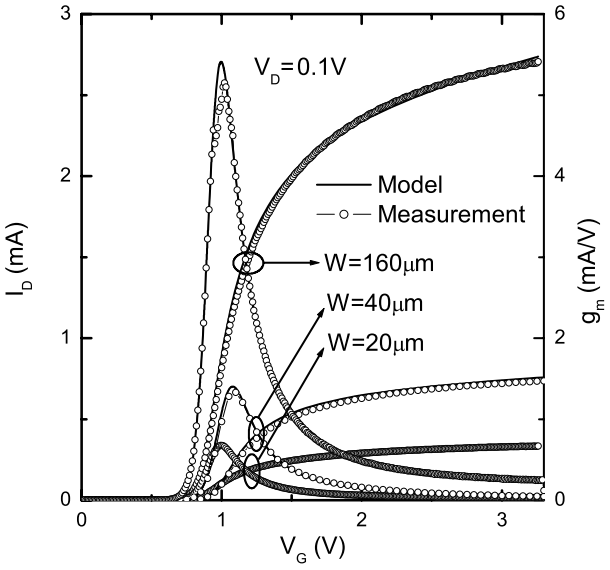

Fig. 16. Width scaling: I_D–V_G and g_m–V_G for $W = 20\ \mu m$, 40 μm, 160 μm, $L = 0.6\ \mu m$ and $N_F = 2$ at $T = 30\ °C$ and $V_D = 0.1\ V$ for VDMOS transistor.

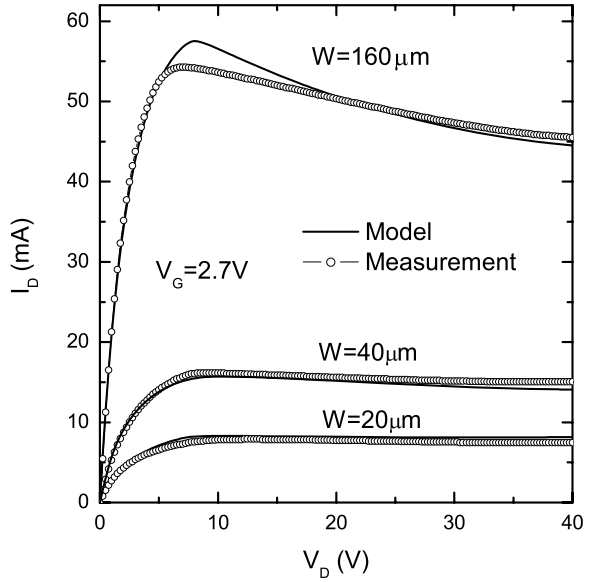

Fig. 17. Width scaling: I_D–V_D for different widths for $L = 0.6\ \mu m$ and $N_F = 2$ at $T = 30\ °C$ for VDMOS transistor. The self-heating effect is more prominent for higher widths due to increased power dissipation.

modeling the lateral non-uniform doping in the intrinsic MOS channel of high voltage devices [25].

Model scalability: An important characteristic of any model is the scalability with physical and electrical parameters. Fig. 14 shows the transfer characteristics for different temperatures. It can be seen that the model correctly simulates the variation of drain current, transconductance and most importantly the threshold voltage shift with temperature. An important observation is that ZTC (zero-temperature-coefficient) point is also well modeled in Fig. 14.

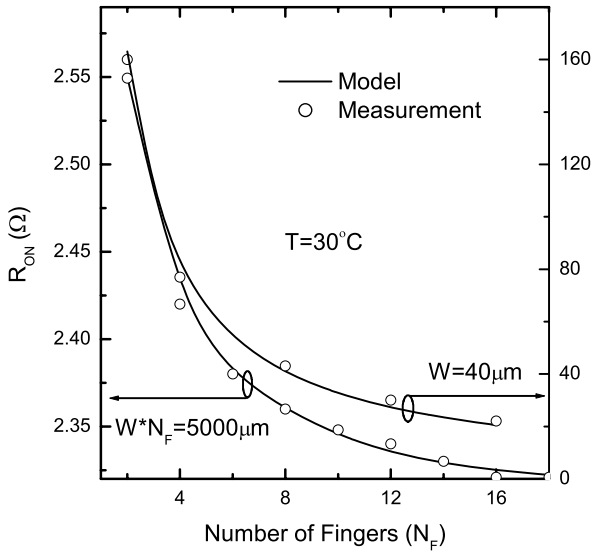

Fig. 18. ON-resistance R_{ON} with number of fingers (N_F) for $W = 40$ μm and $W \cdot N_F = 5000$ μm at $V_G = 3.3$ V and $V_D = 0.5$ V for drain-all-around VDMOS transistor at $T = 30$ °C. The decrease of R_{ON} with number of fingers for drain-all-around device is caused by current spreading at the finger edges.

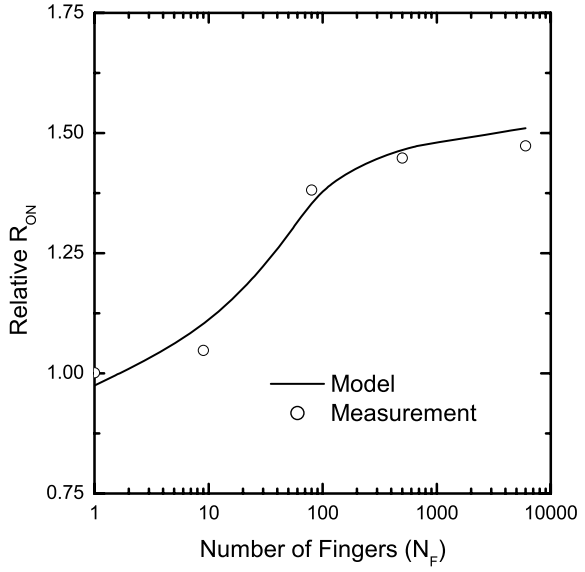

Fig. 19. Relative On-resistance $\frac{R_{ON}}{R_{ON}|_{N_F=1}}$ with Number of fingers (N_F) for drain-on-side VDMOS transistor. The increase in R_{ON} with number of fingers for drain-on-side device is caused by the interaction of depletion regions of the neighborhood fingers.

Fig. 15 shows the I_D–V_D curves for different temperatures, which demonstrates that the SHE is correctly modeled for entire temperature range. The scaling of the model is also tested for different device geometries. The transfer and output characteristics shown in Figs. 16 and 17 respectively, demonstrate that the model scales excellently with different transistor widths. The variation of ON resistance (R_{ON}) with number of fingers (N_F) is modeled using k_{rd} and N_{CRIT} parameters in (3). Fig. 18 shows that the R_{ON} scaling with N_F is well modeled for different widths for drain-all-around device. The decrease of R_{ON} with number of fingers for drain-all-around device is caused by current spreading at the finger edges. Fig. 19 shows the R_{ON} scaling

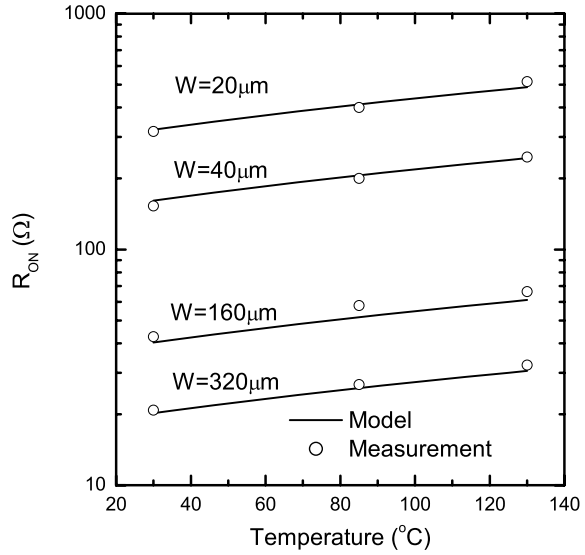

Fig. 20. R_{ON} with temperature for $N_F = 2$ and $W = 20$ μm, 40 μm, 160 μm, 320 μm for VDMOS transistor.

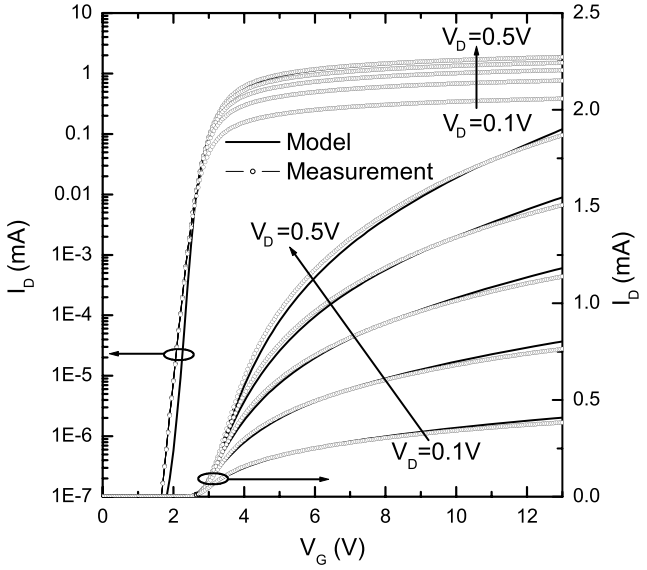

Fig. 21. Transfer characteristics of 40 V LDMOS device ($W = 40$ μm, $L = 1.2$ μm and $N_F = 1$): I_D–V_G for $V_D = 0.1$–0.5 V in steps of 0.1 V at $T = 30$ °C.

with N_F for drain-on-side device. The increase in R_{ON} with number of fingers for drain-on-side device is caused by the interaction of depletion regions of the neighborhood fingers. R_{ON} scalability with temperature is shown in Fig. 20 for different transistor widths. The increase in R_{ON} with temperature is excellently modeled for different transistor widths.

5.2. Case study 2: lateral DMOS device

The schematic representation of the LDMOS device under study is shown in Fig. 1(b). Figs. 21 and 22 show the I_D–V_G and g_m–V_G for $V_D = 0.1$ V to 0.5 V respectively. Figs. 23 and 24 show the I_D and g_m–V_G for $V_D = 1$–5 V and I_D–V_D characteristics respectively for 40 V LDMOS, which demonstrate that the model provides correct simulation of current and transconductance for different bias conditions. The gate-to-drain and gate-to-gate capacitance curves shown in Figs. 25 and 26 respectively demonstrate that the model predicts correct trend for capacitances.

Model scalability: an important issue in any LDMOS model is the scalability with drift length for different voltage handling capability. Figs. 27 and 28 shows the transfer and output characteristics of a 100 V LDMOS device on the same technology, which demonstrates that the model

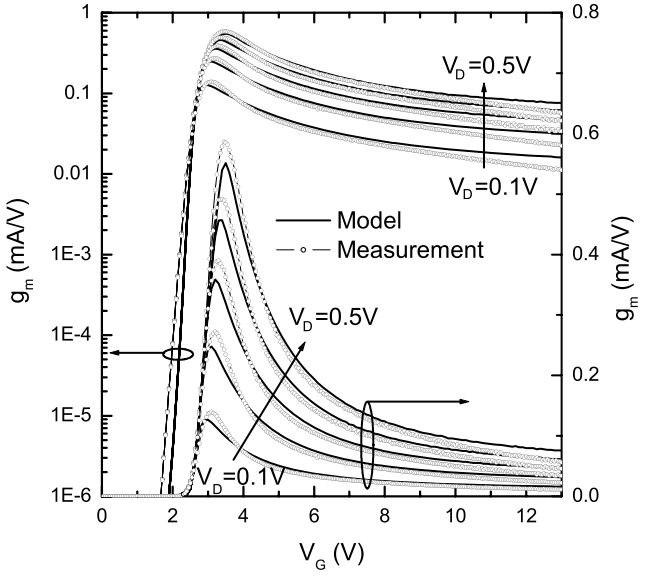

Fig. 22. Transfer characteristics: g_m–V_G for $V_D = 0.1$–0.5 V in steps of 0.1 V at $T = 30$ °C for 40 V LDMOS device ($W = 40$ μm, $L = 1.2$ μm and $N_F = 1$).

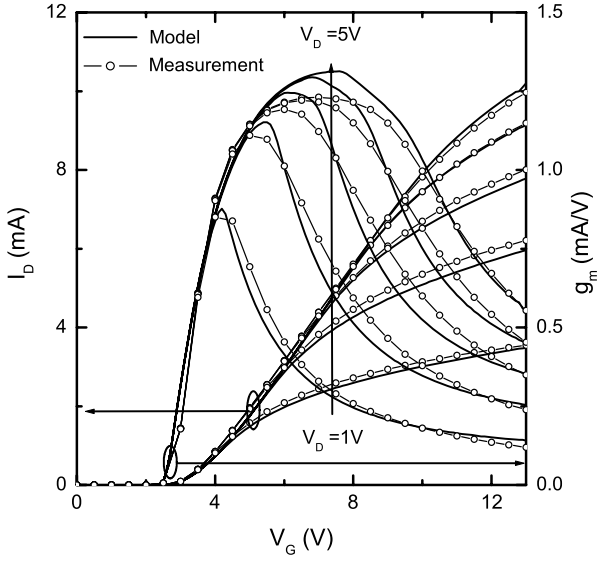

Fig. 23. Transfer characteristics of 40 V LDMOS device ($W = 40$ μm, $L = 1.2$ μm and $N_F = 1$): I_D–V_G for $V_D = 1$–5 V in steps of 1 V at $T = 30$ °C.

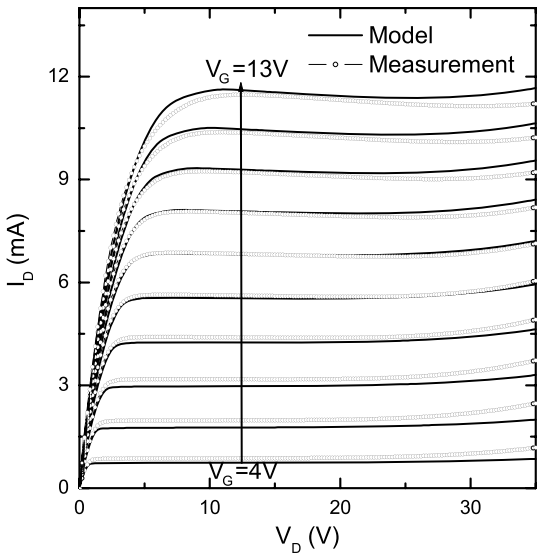

Fig. 24. Output characteristics: I_D–V_D for 40 V LDMOS device ($W = 40$ μm, $L = 1.2$ μm and $N_F = 1$) at $T = 30$ °C. Note self-heating effect and impact ionization effect is well modeled.

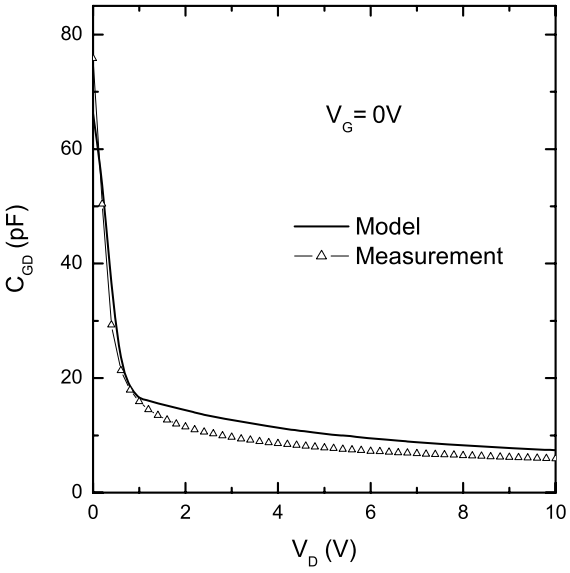

Fig. 25. Plot of gate-to-drain capacitance C_{GD} vs. V_D at $V_G = 0$ V for 40 V LDMOS device. Here C_{GD} includes the drift overlap capacitance.

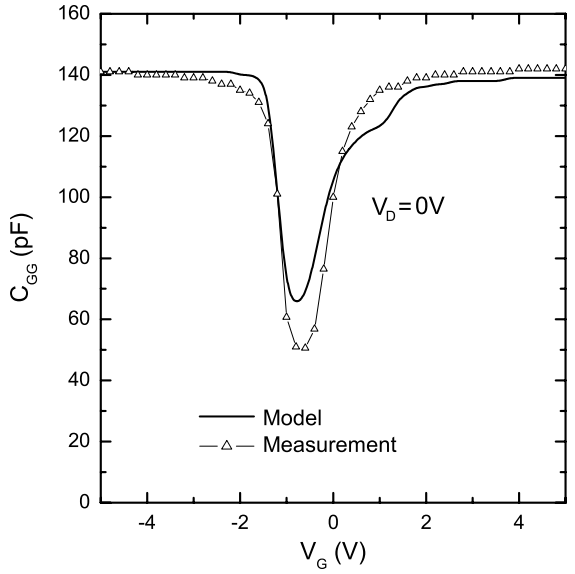

Fig. 26. Plot of gate-to-gate capacitance C_{GG} vs. V_G at $V_D = 0$ V for 40 V LDMOS device.

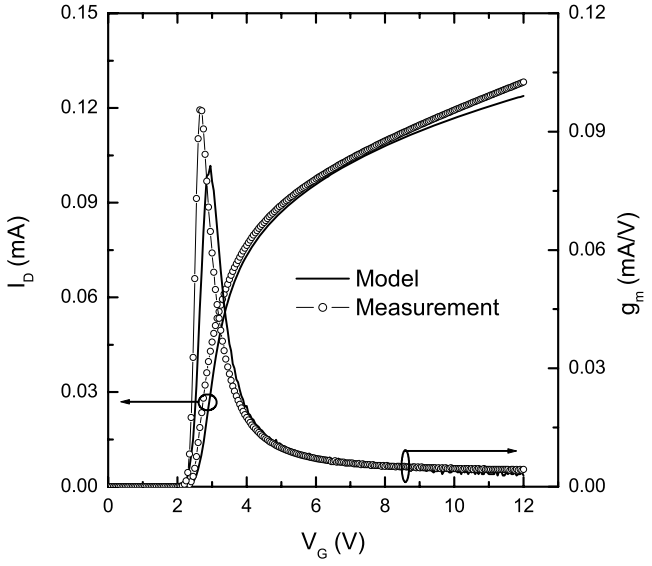

Fig. 27. Drift Scaling: I_D–V_G and g_m–V_G at $V_D = 0.1$ V for 100 V LDMOS device ($W = 40$ μm, $L = 1.2$ μm and $N_F = 1$) at $T = 30$ °C.

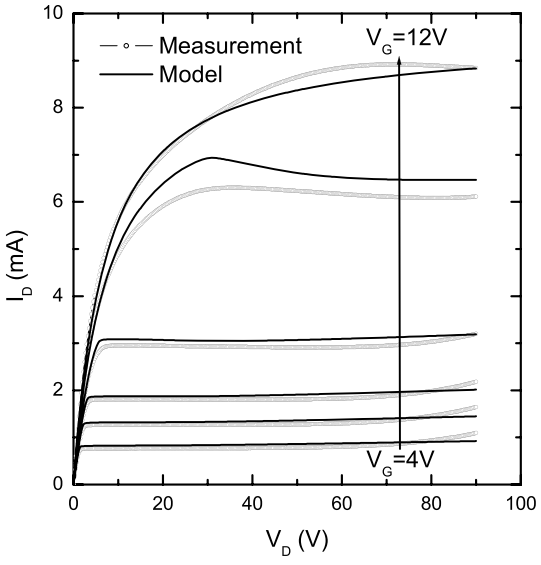

Fig. 28. Drift Scaling: I_D–V_D for 100 V LDMOS device ($W = 40$ μm, $L = 1.2$ μm and $N_F = 1$) for $V_G = 4$, 4.5, 5, 6, 9 and 12 V at $T = 30$ °C.

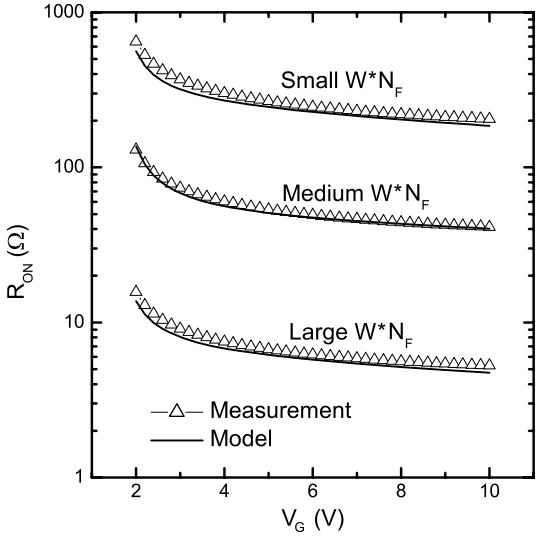

Fig. 29. Width scaling: R_{ON} vs. V_G for three different W^*N_F for 40 V LDMOS device at $T = 30$ °C.

scales well with drift length. It should be noted that not only the self-heating effect [23] is excellently modeled in Fig. 28 but also the quasi-saturation effect observed at higher gate biases. The scalability of the model is also tested for R_{ON} for different widths of LDMOS device. Fig. 29 shows the R_{ON} vs. V_G for three different widths of 40 V LDMOS device.

6. Parameter extraction and model calibration

Tables 1–3 show the list of main parameters used in the model. These basic parameters are used for modeling of any high voltage device at room temperature. The calibration procedure is described below. First threshold voltage [26] and mobility is extracted using any standard extraction method. Other standard EKV parameters [27] are extracted using methodology proposed in [28]. Once we have all of these parameters, *GAMMA* and *PHI* are tuned for sub-threshold slope on I_D–V_G characteristics. *E*0 is tuned on I_D–V_G characteristics in strong inversion for mobility degradation due to vertical field. UCRIT and LAMBDA are tuned on I_D–V_D characteristics for velocity saturation and channel length modulation, respectively. Drift parameters VSAT and α_{vsat} are fitted in the linear region of I_D–V_D characteristics while θ_{Acc} is used to lower the drift resistance on I_D–V_G characteristics at high V_G as described earlier. k_{rd} and N_{CRIT} parameters are fitted to model the effect of number of fingers on drift resistance.

Table 1
Main EKV parameters

Name	Description	Units
Type	P-type/N-type	–
W	Channel width	m
L	Channel length	m
N_F	Number of fingers	–
C_{ox}	Oxide capacitance	F/m^2
V_{T0}	Long-channel threshold voltage	V
U_0	Low field mobility	cm^2/Vs
GAMMA	Body effect parameter	$\sqrt{V}$
PHI	Bulk Fermi potential	V
E_0	Mobility reduction coefficient	V/m
UCRIT	Longitudinal critical field	V/m
LAMBDA	Channel length modulation	–

Table 2
Drift parameters

Name	Description	Units
L_{DR}	Drift length	m
L_{OV}	Gate overlap in the drift region	m
ρ_{Drift}	Drift resistivity	V/Am
VSAT	Velocity saturation parameter	V
α_{vsat}	”	–
θ_{Acc}	Accumulation charge effect	1/V
k_{rd}	Effect of number of fingers	–
N_{CRIT}	”	–
α_T	Thermal coefficient of drift resistance	1/K

Table 3
Self-heating and impact ionization parameters

Name	Description	Units
R_{THNOM}	Thermal resistance	Ks/J
α	Temperature coefficient of R_{THNOM}	1/K
C_{TH}	Thermal capacitance	J/K
NEFF	Effective doping in the drift	$V^{-\frac{4}{3}}$

The extraction of self-heating parameters requires dedicated measurement setup. The extraction of thermal resistance and capacitance has been discussed in detail in [22,23,29]. The impact ionization parameter N_{EFF} is used as a fitting parameter to model the impact ionization in the drift region.

7. Conclusion

A new high voltage compact model based on the EKV model as a core and new bias dependent drift resistance is presented. The model performance was demonstrated for two industrial devices: VDMOS and LDMOS. The model correctly reproduces the special effects of high voltage devices like the quasi-saturation and self-heating effect, and is highly scalable with all physical and electrical parameters such as transistor width, drift length, number of fingers and temperature. The model shows excellent results for entire DC bias range and good behavior for capacitances, especially the peaks and shift of these peaks with bias. The model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any operation regime of HV MOSFETs. The model has been implemented in Verilog-A and tested on SABER (Synopsys), ELDO (Mentor Graphics) and Cadence‘s Virtuoso Spectre circuit simulator and Virtuoso UltraSim fast-Spice simulator for industrial use.

Acknowledgements

The authors would like to thank H. Heinisch, F. Udrea, S. Gamage, G. J. Coram, A. S. Roy, J.-M. Sallese and S. Samala for interesting discussions. This work was supported by the IST-507653 ‘ROBUSPIC’ EC project and the Swiss OFES No. 03-491.

References

[1] Canepari A, Bertrand G, Giry A, Minondo M, Blanchet F, Jaouen H, et al. LDMOS modeling for analog and RF circuit designs. In: IEEE European solid-state device research conference (ESSDERC), September 2005. p. 469–72.
[2] Frere S, Moens P, Desoete B, Wojciechowski D, Walton A. An improved LDMOS transistor model that accurately predicts capacitance for all bias conditions. In: Proceedings of the 2005 international conference on microelectronic test structures (ICMTS), April 2005. p. 75–9.
[3] D’Halleweyn N, Benson J, Redman-White W, Mistry K, Swanenberg M. MOOSE: a physically based compact DC model of SOI LD MOSFETs for analogue circuit simulation. IEEE Trans Computer-Aided Design Integr Circ Systems 2004;23(10):1399–410.
[4] Anghel C. High voltage devices for standard MOS technologies: characterisation and modelling, Ph.D. dissertation, EPFL, 2004, thesis No. 3116.
[5] Hefyene N, Anghel C, Ionescu A, Frere S, Gillon R, Vermandel M, et. al. An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs. In: IEEE European solid-state device research conference (ESSDERC). September 2001. p. 403–6.
[6] Hefyene N. Electrical characterization and modelling of lateral DMOS transistor: investigation of capacitances and hot-carrier impact, Ph.D. dissertation, EPFL, 2005, thesis No. 3200.
[7] Aarts A, D’Halleweyn N, van Langevelde R. A surface-potential-based high-voltage compact LDMOS transistor model. IEEE Trans Electron Dev 2005;52(5):999–1007.
[8] Aarts A, Kloosterman W. Compact modeling of high-voltage LDMOS devices including quasi-saturation. IEEE Trans Electron Dev 2006;53(4):897–902.
[9] Victory J, Sanchez J, DeMassa T, Welfert B. A static, physical VDMOS model based on the charge-sheet model. IEEE Trans Electron Dev 1996;43(1):157–64.
[10] Tsai C-Y, Burk DE, Ngo KDT. Physical modeling of the power VDMOST for computer-aided design of integrated circuit. IEEE Trans Electron Dev 1997;44(3):472–80.
[11] Chauhan YS, Anghel C, Krummenacher F, Gillon R, Baguenier A, Desoete B, et al. A compact DC and AC model for circuit simulation of high voltage VDMOS transistor. In: IEEE international symposium on quality electronic design (ISQED), March 2006. p. 109–14.
[12] Chauhan YS, Anghel C, Krummenacher F, Ionescu AM, Declercq M, Gillon R, et al. A highly scalable high voltage MOSFET model. In: IEEE European solid-state device research conference (ESSDERC), September 2006. p. 270–3.

[13] Enz C, Krummenacher F, Vittoz E. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. J Analog Integr Circ Signal Process 1995;8(1):83–114.
[14] Chauhan YS, Anghel C, Krummenacher F, Ionescu A, Declercq M, Gillon R, et al. Ekv based l-dmos model update including internal temperatures, http://www-g.eng.cam.ac.uk/robuspic/reports.htm, 2004–2006.
[15] Chauhan YS. Ekv based dmos model extension for v-dmos, http://www-g.eng.cam.ac.uk/robuspic/reports.htm, 2004–2006.
[16] Anghel C, Hefyene N, Ionescu A, Vermandel M, Bakeroot B, Doutreloigne J, et al. Investigations and physical modelling of saturation effects in lateral DMOS transistor architectures based on the concept of intrinsic drain voltage. In: IEEE European solid-state device research conference (ESSDERC), September 2001. p. 399–402.
[17] Hefyene N, Vestiel E, Bakeroot B, Anghel C, Frere S, Ionescu A, et al. Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET. In: IEEE international conference on simulation of semiconductor processes and devices (SISPAD), September 2002; p. 203–6.
[18] Anghel C, Chauhan YS, Hefyene N, Ionescu A, A physical analysis of HV MOSFET capacitance behaviour, in: IEEE international symposium on industrial electronics (ISIE), vol. 2, June 2005. p. 473–7.
[19] Sallese J-M, Bucher M, Krummenacher F, Fazan P. Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model. Solid-State Electron 2003;46(11):677–83.
[20] Kreuzer C, Krischke N, Nance P. Physically based description of quasi-saturation region of vertical DMOS power transistors. In: IEEE international electron devices meeting (IEDM). December 1996. p. 489–92.
[22] Anghel C, Hefyene N, Gillon R, Tack M, Declercq M and Ionescu A. New method for temperature-dependent thermal resistance and capacitance accurate extraction in high-voltage DMOS transistors. In: IEEE international electron devices meeting (IEDM), December 2003. p. 5.6.1–4.
[23] Anghel C, Gillon R, Ionescu A. Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs. IEEE Electron Dev Lett 2004;25(3):141–3.
[24] Rossel P, Tranduc H, Montcoqut D, Charitat G, Pages I, Avalanche characteristics of MOS transistors. In: IEEE international conference on microelectronics, vol. 1, September 1997. p. 371–81.
[25] Chauhan YS, Krummenacher F, Anghel C, Gillon R, Bakeroot B, Declercq M, et al. Analysis and modeling of lateral non-uniform doping in high-voltage MOSFETs. In: (accepted at) IEEE Intnational Electron Devices Meeting (IEDM), December 2006.
[26] Anghel C, Bakeroot B, Chauhan YS, Gillon R, Maier C, Moens P, et al. New method for threshold voltage extraction of high-voltage MOSFETs based on gate-to-drain capacitance measurement. IEEE Electron Dev Lett 2006;27(7):602–4.
[27] "Ekv mos model," http://legwww.epfl.ch/ekv.
[28] Bucher M, Lallement C and Enz CC. An efficient parameter extraction methodology for the EKV MOST model. In: IEEE international conference on microelectronic test structures (ICMTS), March 1996. p. 145–50.
[29] Anghel C, Ionescu A, Hefyene N and Gillon R. Self-heating characterization and extraction method for thermal resistance and capacitance in high voltage MOSFETs. In: IEEE European solid-state device research conference (ESSDERC), September 2003. p. 449–52.