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Modeling of bias-induced changes of organic field-effect transistor characteristics

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Chapter 1

General Introduction

Organic-based semiconductors in thin film form are projected to be active elements in plastic-based circuits, particularly those using field-effect transistors as switching or logic elements. Progress in the understanding of charge transport in organic semiconductors and advances in fabrication techniques have paved the way for successful commercialization of organic light-emitting diodes. However, the performance of organic field-effect transistors (OFETs) is not only dependent on the organic semiconductor but also on the gate dielectric used. Moreover, charge transport in OFETs occurs in a very thin layer of the organic semiconductor. A proper understanding of how charge transport in OFETs is influenced by these factors is still lacking. In particular, how these factors contribute to the operational instability known as the bias-stress effect observed in OFETs is an important issue that needs to be addressed. It is the objective of this thesis to understand and model the electrical characteristics of OFETs and identify the mechanism of the bias-stress effect. The purpose of this chapter is to introduce the reader to organic electronics and to give an outline of this thesis. We begin the chapter by an introduction to the field of organic electronics. We briefly describe the main characteristics of charge transport in organic semiconductors. Next, we discuss the conduction mechanism of organic field-effect transistors and the typical measurements performed to characterize charge transport. Finally, we define the research goals and give an outline of the thesis.

1.1   Organic electronics

Materials can be classified into four different categories based on their electrical properties. These categories are conductors, superconductors, insulators, and semiconductors. In the first two categories of materials charges can travel with a small resistance or no resistance at all. In the third category, the insulators, the charges are localized or energetically separated from conducting states by a large band gap and therefore no conduction can occur. Semiconductors present a situation that lies in between conductors and insulators. Under different conditions these materials can be either insulators or conductors.

   In organic semiconductors the band gap[1,2] is in the range of 1-4 eV.[3] In 1977, the first report on electrical conduction in organic semiconducting polymers showed that when appropriately doped, organic semiconductors show metallic behavior.[4] Nowadays, organic semiconductors are a well-established class of functional materials and are highly promising candidates as active components in several optoelectronic devices such as organic field-effect transistors (OFETs),[1,5] light-emitting diodes (OLEDs),[6,7] photovoltaic cells,[8,9] and sensors.[10] Important advantages of organic semiconducting materials over their inorganic counterparts are their almost limitless chemical tunability, their low weight, their relative low cost, and the ease with which they can be processed. Many organic semiconductors can be processed from solution by using relatively cheap techniques like ink-jet printing or spin-coating, whereas ultra-clean high-vacuum conditions and high temperatures are required for processing inorganic semiconductors. Organic field-effect transistors, light emitting diodes, photovoltaic cells, and sensors are paving the way for applications, such as large-area lighting systems, biomedical sensors, radio-frequency identification tags, electronic paper, and flexible displays and solar cells. It is much easier to obtain flexibility of the latter devices than when using more conventional materials like copper or silicon. As an example, Fig. 1.1 shows a bendable polymer foil containing several electronic components and circuits. This combination of the advantages of organic materials with properties of metals or semiconductors has opened the way for major interdisciplinary research.

1.1.1   Organic semiconductors

The optoelectronic properties of the organic semiconductors originate from the presence of π-conjugation.[3] π-conjugation refers to the alternation of single (σ) and double (σ and π) bonds within the oligomer or polymer. In non-conjugated materials, like poly-ethylene, all four electrons in the outer shell of the carbon atoms occupy hybridized sp^3-orbitals, leading to a strong σ-bonding between the carbon atoms. Figure 1.2 shows the chemical structures of some of the π-conjugated organic semiconductors. In conjugated organic materials, only three electrons in the outer shell of the carbon atoms occupy hybridized sp^2-orbitals in the plane of the backbone and contribute to the single σ-bonding of the carbon atoms. The fourth electron is located in a p_z-orbital pointing out of the plane of the backbone. The p_z-orbitals of neighboring carbon atoms overlap with each other and form a π-bond, which is weaker than the σ-bonds. The combination of a σ- and π-bond leads to a double carbon bond. The electrons belonging to π-orbitals formed by the overlapping p_z-orbitals are delocalized over the whole conjugated part
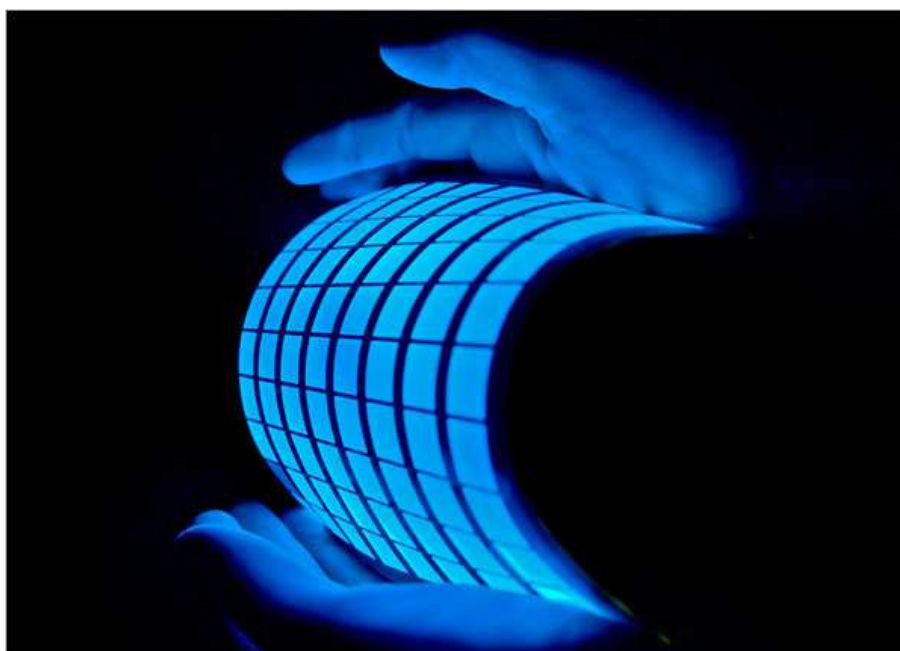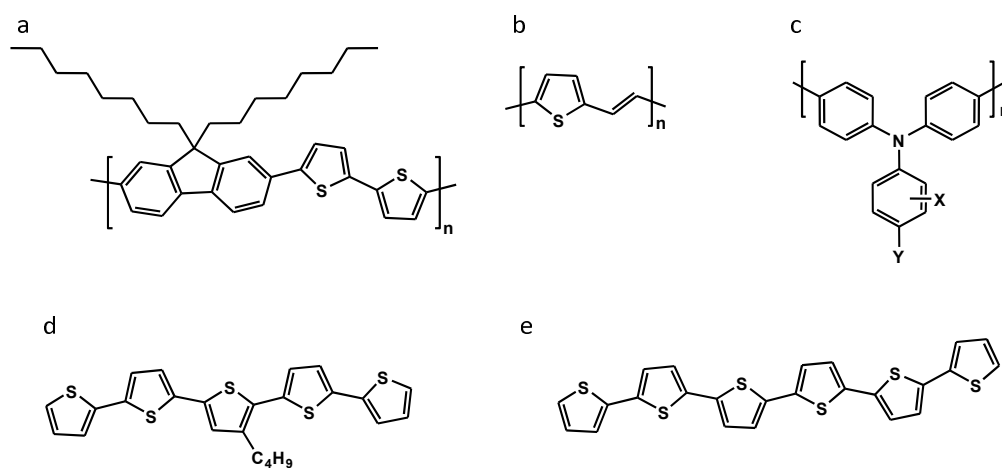
Figure 1.1: A photograph of a flexible OLED.[11]

Figure 1.2: Typical π-conjugated organic semiconductors. (a) poly(9,9'-dioctyl-fluorene-co-biothiophene) (F8T2) (b) polythienylene-vinylene (PTV) (c) polytriarylamine (PTAA) (d) 3-butyl α-quinquethiophene (3BuT5) (e) sexithiophene (T6)

of the molecule. The formation of a system of π-bonds via the overlap of p_z-orbitals is called π-conjugation. Molecules with an alternating series of single and double carbon bonds in the carbon backbone are not the only molecules in which conjugation occurs. π-conjugation can also occur with interruption of the carbon backbone by a single nitrogen or sulfur atom. The total set of occupied molecular π-orbitals can be compared to the states in the valence band of inorganic materials, while the set of unoccupied molecular π orbitals, or π^*-orbitals, can be compared to states in the conduction band of inorganic materials. The occupied molecular orbital with the highest energy is called the Highest Occupied Molecular Orbital (HOMO), whereas the unoccupied molecular orbital with the lowest energy is called the Lowest Unoccupied Molecular Orbital (LUMO). An important aspect of organic semiconductors is the presence of a strong electron-phonon coupling. This leads to a significant lattice deformation around a charge. The combination of a charge and its surrounding lattice deformation is called a polaron.

If one zooms in on a thin film of a π-conjugated polymer, one would find coils, kinks, and impurities. On a microscopic scale, the film would look amorphous. This structural disorder disrupts the π-conjugation of the polymer chains and each chain may therefore be considered to consist of a number of separated conjugated segments. This leads to the splitting up of the π-conjugated system of overlapping p_z-orbitals into separate electronic states that are spatially delocalized over a few monomer units. This results in energetic disorder, because the energies of the conjugated segments vary due to their different local arrangements and their different lengths. In addition, structural disorder leads to poor electronic coupling between neighboring chains. The energetic disorder is quantified by a standard deviation σ. Typically, σ varies between 0.1 and 0.2 eV.

1.1.2 Charge transport

The electrical properties of organic semiconductors are usually studied by measuring the mobility, which represents the ease with which charges travel through the material. The measurement of this parameter gives information about the physical processes involved in the conduction process. Its temperature dependence gives important information about the energy distribution of the localized states. However, mobility is an ensemble property of a collection of such states and the values obtained result from an average of microscopic events. It is then difficult from the macroscopic measurements to distinguish between several possible microscopic mechanisms involved in the conduction process. Charge-carrier mobilities in polymers are in general several orders of magnitude lower in comparison to those in the organic crystals. The low mobility is mainly caused by the inherent structural disorder of these materials.

The mobility of charge carriers in organic semiconductors can be calculated by performing Master-equation calculations or Monte-Carlo simulations. In these calculations, charge transport is modeled by a phonon-assisted tunneling process, referred to as "hopping". Charge hopping takes place from one site to another and the energies on the sites are distributed according to a certain density of states (DOS).[12] Often, the DOS in organic materials is assumed to be Gaussian.[13]

$$g(E) = \frac{N_t}{\sqrt{2\pi}\sigma} \exp\left[-\frac{E^2}{2\sigma^2}\right],$$ (1.1)

where E is the site energy, σ is the standard deviation of the DOS, and N_t is the density of sites. The on-site energies can be either spatially uncorrelated or correlated. In the case of spatially uncorrelated disorder, the site energies are randomly distributed according to the Eqn. (1.1). On the other hand, if dipoles of equal magnitude d are placed at each site with a random orientation, the distribution of the resulting electrostatic energy is a spatially correlated Gaussian with a width σ proportional to d. The rate of hopping of a charge carrier between two sites depends on the overlap of the localized electronic wave functions of these two sites, which allows tunneling from one site to another. Whenever a charge carrier hops to a site with a higher (lower) site energy than the site that it came from, the difference in energy is accommodated for by the absorption (emission) of a phonon. The mechanism of phonon-assisted tunneling or "hopping" was proposed by Mott and Conwell to explain DC conduction properties of inorganic semiconductors.[14–16] Nowadays this mechanism is also used to describe the conductivity in a wide variety of organic materials. In the description of charge transport in organic semiconductors, the hopping formalism of Miller and Abrahams[17] has been extensively employed. According to this formalism, the rate of hopping of a charge carrier from site i to site j, W_{ij}, is given by

$$
\begin{aligned}
W_{ij} &= \nu_0 exp\left[-2\alpha R_{ij} - \beta(E_j - E_i)\right], E_j \geq E_i \\
&= \nu_0 exp[-2\alpha R_{ij}], \qquad\qquad E_j < E_i.
\end{aligned}
\tag{1.2}
$$

Here, $\beta = 1/k_B T$, with k_B Boltzmann's constant and T temperature, ν_0 is a phonon frequency, $|\mathbf{R}_i - \mathbf{R}_j|$ is the distance between sites i and j, and E_i and E_j are the on-site energies of sites i and j. α is the inverse localization length of the wave functions. The energy difference in Eqn. (1.2) contains a contribution $-eFR_{ijx}$ due to an electric field F, taken in the x direction of the lattice (e is the unit charge), and a contribution due to the Coulomb interactions with all other, mobile and immobile, charges.

From Eqn. (1.2) it becomes clear that the hopping transport depends on several factors. The energetic disorder and electric field play an important role. Charge carriers preferably hop to sites with a low site energy. By increasing the temperature the Boltzmann penalty for hops upwards in energy becomes less strong. Furthermore, there is a trade-off between hops over a long distance to energetically favorable sites and hops over a short distance to energetically less favorable sites, leading to the phenomenon of variable-range hopping.

The main features of charge transport based on hopping in a Gaussian density of states are the following:

1. Electric field dependence: In time-of-flight experiments on polymers containing π-conjugated copolymerized molecules the mobility was found to increase strongly with voltage. It was found that for a rather broad range of voltages, the mobility μ could be described using a Poole-Frenkel type electric field dependence of the form

$$
\mu = \mu_0 \exp(\gamma \sqrt{F}).
\tag{1.3}
$$

Here, μ_0 is the zero-field mobility and γ is a field activation parameter. Bässler *et al*[18,19] showed that for a limited field range the functional field dependence of the mobility of

Eqn. (1.3) could be understood when hopping transport is assumed in a spatially uncorrelated energy landscape with a Gaussian distribution of site energies (Gaussian Disorder Model, GDM). Gartstein and Conwell[20] demonstrated that introduction of correlation of the energies of sites close together can lead to field dependence similar to the Poole-Frenkel one over the wide range of fields where it is usually seen experimentally. Such correlation arise naturally in systems in which the fluctuations of site energy are due to the interaction of charge carriers with permanent dipoles or to molecular density fluctuations.

2. Non-Arrhenius temperature dependence: Within the framework of the Gaussian Disorder Model, the mobility is found to be thermally activated with a temperature-dependent and disorder-dependent activation energy,[18,19,21] so that in zero-field limit the mobility can be described by

$$\mu = \mu_0 \exp\left[-C\left(\frac{\sigma}{k_\mathrm{B} T}\right)^2\right], \tag{1.4}$$

with a typical value of C in the range of 0.36 to 0.46. The $1/T^2$ temperature dependence of the logarithm of the mobility as given in the Eqn. (1.4) is compatible with the temperature dependence observed in time-of-flight experiments on many organic semiconductors.[22] However, the temperature dependence is still debated, since, depending on the measurement technique and on the method used to analyze the experimental results, support for both a $1/T$ and a $1/T^2$ dependence is reported.[22,23]

3. State-filling effect: An increasing charge-carrier density leads to a higher mobility.[13,24] At low carrier density, the average distance between charge carriers is so large that one carrier's motion is not affected by the presence of other carriers. The charge carriers occupy the low-lying states of the DOS and the energy barriers for charge transport are substantial, which results in a low mobility. Above a certain critical density,[25] the average energy of the charges increases substantially with increasing density, as the lowest-energy states are already filled. The activation energy for transport will therefore decrease, resulting in a higher mobility.

It is noted that in the above mentioned studies in the framework of the Gaussian Disorder Model, the effect of polaron formation was neglected. When polaronic effects are more important than the disorder effect, it is proper to use the transition rates that follow from Marcus theory.[26,27]

1.2 Organic field-effect transistors

An organic field-effect transistor has three electrodes; a source, a drain, and a gate electrode, as shown in Fig. 1.3. The source and the drain are co-planar and are directly connected to the semiconductor. The gate is electrically separated from the source and drain electrode by the gate dielectric. The device configuration in which source and drain contacts are put on top of the organic semiconductor is known as the top-contact bottom-gate transistor. This
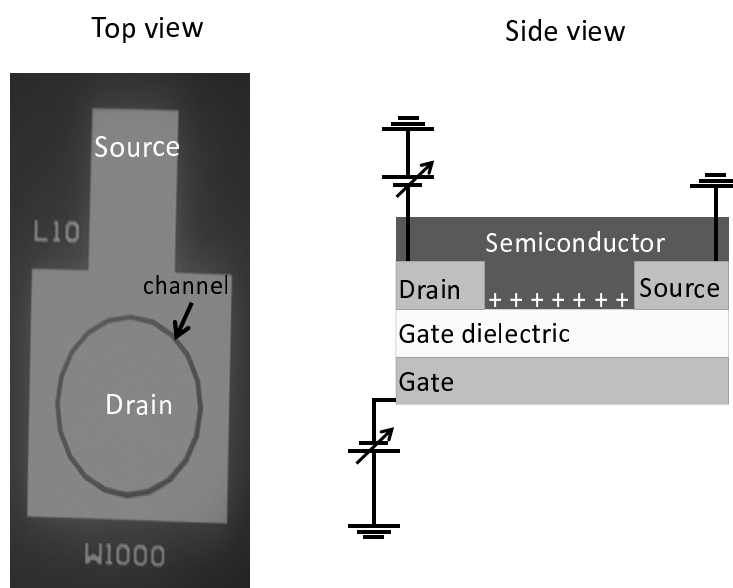
Top view   Side view

Figure 1.3: Optical micrograph (top view) together with a schematic representation of the transistor (side view). The channel length is 10 μm. This device architecture is called bottom-contact bottom-gate transistor. If the source and drain electrodes are put on top of the semiconductor, it is referred to as top-contact bottom-gate transistor.

configuration is also known as the staggered configuration. In this thesis all the experimental data was measured on transistors having a bottom-contact bottom-gate architecture in which source and drain contacts are patterned on the gate dielectric before deposition of the organic semiconductor atop. This architecture is shown in Fig. 1.3. On applying a bias to the gate electrode, charge accumulation occurs in the semiconductor. The accumulated charge resides in the organic semiconductor near the interface with the gate dielectric. In this thesis, we consider only *p*-type organic semiconductors. If a negative gate bias is applied, holes accumulate between the source and drain electrode. This accumulation layer creates a conducting path between the source and the drain electrode. On applying a bias to the drain electrode (with source electrode grounded), charges in the accumulation layer move in the direction of decreasing potential giving rise to a source-drain current. On applying a positive gate bias, the semiconductor is depleted of holes and the transistor is switched off. If the bias between source and drain is kept fixed and the bias applied to the gate electrode is swept from positive to negative value, the current curve obtained is called a transfer curve. A typical transfer curve is shown in Fig. 1.4 for a bottom-contact device.

In inorganic transistors, the threshold-voltage refers to the value of the gate bias at which charge inversion occurs in the channel of the transistor. In organic transistors, there is no charge inversion. In OFETs, the threshold-voltage V_{th} can be empirically defined as the intercept of the extrapolated linear part of the transfer curve with the gate voltage axis. The threshold
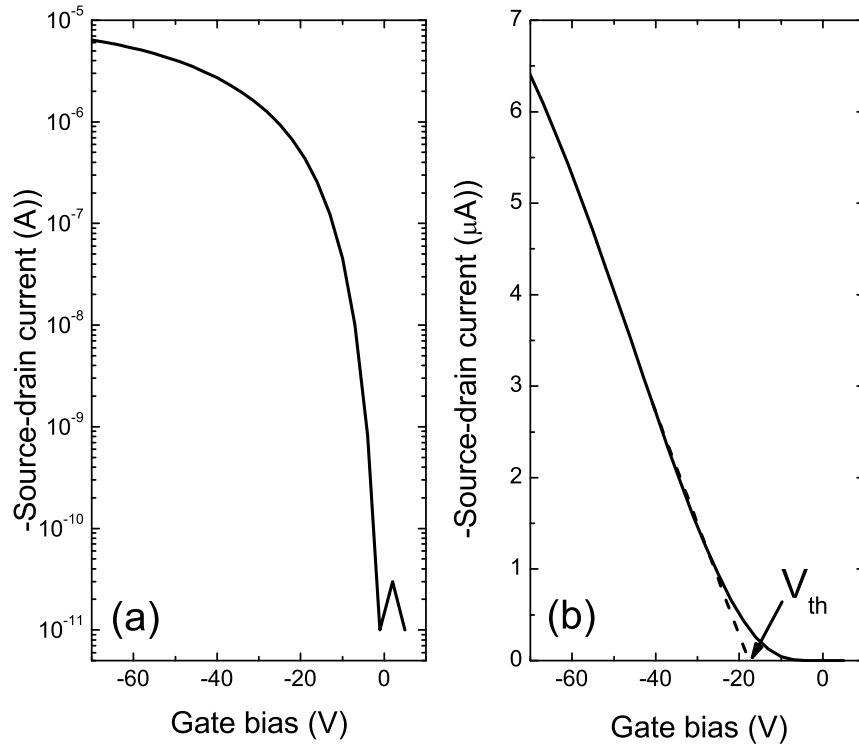
Figure 1.4: Typical transfer curve of a transistor comprising a *p*-type semiconductor, shown on log
scale (a) and linear scale (b). At negative gate bias current flows, at positive gate bias
the current is zero. The threshold voltage V_{th} can be obtained by extrapolating the linear
part of the transfer curve to the gate-voltage axis.

voltage defined in this way is no longer a material parameter but a device parameter, because
it depends on the gate dielectric, the intrinsic mobility of charge carriers in the channel, as well
as the injection properties of the source/drain electrode. When the applied source-drain bias,
V_{SD}, is much smaller than the bias on the gate, V_{G0}, the transistor is said to operate in the
linear regime. In this regime, the charge density in the accumulation layer is uniform throughout
the region between source and drain. On the other hand, when the source-drain bias is much
larger than the gate bias, the charge density in the accumulation layer is no longer uniform. In
this case the charge density decreases continuously to zero as one moves away from the source
electrode to the drain electrode.[28] A transistor operating with drain bias larger than the gate
bias is said to operate in the saturation regime. In both regimes, an approximate expression
for source-drain current can be derived.[28] In the linear regime, where $|V_{SD}| \ll |V_{G0} - V_{th}|$, the
source-drain current, I_{SD}, can be written as

$$I_{SD} = \mu_{lin} \frac{C_{ox} W}{L} \left((V_{G0} - V_{th}) V_{SD} - \frac{1}{2} V_{SD}^2 \right), \tag{1.5}$$

where W and L are the width and length of the transistor, C_{ox} the gate dielectric capacitance
per unit area, μ_{lin} the mobility of the charge carriers in the linear regime. On increasing the

applied source-drain bias to a value such that $V_{SD} = (V_{G0} - V_{th})$, the charge density in the accumulation layer goes to zero near the drain electrode. For $V_{SD} > (V_{G0} - V_{th})$, the source-drain current does not increase with the applied source-drain bias. In the saturation regime, where $|V_{SD}| \geq |V_{G0} - V_{th}|$, the source-drain current can therefore be obtained from Eqn. 1.5 by substituting $V_{SD} = (V_{G0} - V_{th})$ as shown below.

$$I_{SD} = \mu_{sat} \frac{C_{ox} W}{2L} (V_{G0} - V_{th})^2 . \tag{1.6}$$

The mobility μ_{lin} in the linear regime can be extracted from Eqn. (1.5) by taking the first derivative of the source-drain current with respect to the gate bias:

$$\mu_{lin} = \frac{L}{V_d C_{ox} W} \left| \frac{\partial I_{SD}}{\partial V_{G0}} \right| . \tag{1.7}$$

Similarly, the mobility μ_{lin} in the saturation regime can be extracted from Eqn. (1.6) by taking the second derivative of the source-drain current with respect to the gate bias:

$$\mu_{sat} = \frac{L}{C_{ox} W} \left| \frac{\partial^2 I_{SD}}{\partial V_{GS}^2} \right| . \tag{1.8}$$

The mobility extracted as described above is not the intrinsic mobility of the charge carriers. μ_{lin} and μ_{sat} are also device parameters. For the same organic semiconductor these values will depend on the trap states at the surface of the the gate dielectric, the permittivity of the gate dielectric, chemical impurities, the type of contacts used in the device architecture, etc.. As mentioned earlier, the intrinsic mobility of charge carriers depends strongly on the state-filling effect.[13] This implies that the mobility is strongly dependent on the applied gate bias. In writing Eqns. (1.7) and (1.8), this dependence has been neglected. Reese *et al.* performed a detailed study on the extraction of the intrinsic charge-carrier mobility from current-voltage characteristics.[29]

The intrinsic mobility of holes in organic field-effect transistors depends on the temperature as well as the applied gate bias.[24,30] Vissenberg and Matters[24] derived an analytic expression for the field-effect mobility in an organic field-effect transistor using percolation theory and the concept of hopping in an exponential density of localized states. The authors used the concept of variable-range hopping to describe charge transport in OFETs. The calculated temperature dependence and gate voltage dependence agreed well with those of the observed field-effect mobility in both a pentacene and a poly(thienylene-vinylene) (PTV) thin-film transistor. According to their theory, the differences in the magnitude and in the temperature dependence of the field-effect mobility of pentacene and PTV transistors were due to differences in the structural order of the organic films. Tanase *et al.*[31] showed that the large mobility differences reported for conjugated polymers used in organic light-emitting diodes (poly(2-methoxy-5-(3′,7′-dimethyloctyloxy)-p-phenylene vinylene)) and field-effect transistors (poly(3-hexyl thiophene)) originate from the strong dependence of the mobility on the charge-carrier density. In their study, they showed that an exponential density of states is a good approximation of the tail states of the Gaussian and can be used to describe charge transport in OFETs.

To summarize, the dependence of the mobility of charge carriers in OFETs on temperature and gate-voltage is understood within the framework of hopping in a disordered energy landscape.[24,30,31] The model for the mobility of the charge carriers[24] can successfully describe the static current-voltage characteristics of an OFET.

1.3   Scope of this thesis

The electrical characteristics of an OFET are dynamic in nature. During operation, under application of a prolonged gate bias, the source-drain current decreases monotonically with time. This decrease in the current is not related to decrease in mobility of charge carriers during operation. The decreasing source-drain current is due to a shift of the threshold voltage with time, which finally leads to a disfunctioning of the transistors. This highly undesirable effect is referred to as the "bias-stress effect". This electrical instability of OFETs was essentially not understood.[32–43] In the next chapter, the bias-stress effect will be discussed in detail. It is the main impediment for the commercialization of OFETs and its resolution is therefore of crucial importance. The main motivation for this thesis work was to uncover the origin of this effect. In order to understand and model bias-induced changes of the characteristics of OFETs, the following questions are addressed in this thesis:

1. What are the main features of the bias-stress effect?

2. What is the origin of the bias-stress effect?

3. Can the bias-stress effect be quantitatively modeled?

4. Does the bias-stress effect involve other changes in the characteristics of OFETs but a shift of the threshold voltage?

5. Can the bias-stress effect be eliminated?

This thesis work involved a collaboration with experimental groups at Philips and the TU/e. Most experiments in these groups were done on bottom-contact bottom-gate transistors using polytriarylamine (PTAA) as the organic semiconductor. In the work described in Chapter 6 the organic semiconductor was a self-assembled monolayer (SAM). In all experiments SiO_2 (silicon-dioxide) was used as the gate dielectric.

In Chapter 2, the bias-stress effect in p-type organic field-effect transistors with silicon-dioxide as the gate dielectric is discussed. The main features of the bias-stress effect are presented. Some of the previously reported mechanisms that have been proposed as an explanation of the effect are briefly discussed. It is shown that there are many aspects of the bias-stress effect that cannot be explained by the proposed mechanisms. It is argued that water present on the surface of the gate dielectric is the primary cause of the bias-stress effect. Experimental studies are discussed that highlight the influence of water on the dynamics of the bias-stress effect.

A mechanism for the bias-stress effect is proposed in Chapter 3. This mechanism, referred to as the proton-migration mechanism, is based on the hole-assisted production of protons from water in the accumulation layer of the transistor and their subsequent migration into the gate dielectric. It is proposed that the time scale of the bias-stress effect is governed by the diffusion of protons in the gate dielectric. Based on the proton-migration mechanism, a quantitative model with a single parameter is developed for the bias-stress effect and is compared with the experiments. It is shown that the proposed model explains the much debated role of water and several other unexplained aspects of the instability of these transistors.

On applying a zero gate bias to a device that has been exposed to bias stress for an extended period of time, the threshold voltage shifts back to its original value prior to stressing. This phenomenon, known as recovery, is discussed in Chapter 4. It is shown that recovery can be explained within the framework of the proton-migration mechanism. A quantitative model of recovery is developed and is compared with experiments. It is shown how a shorter period of application of a gate bias leads to a faster backward shift of the threshold voltage when the gate bias is removed.

In Chapter 5, the predictions of the model based on the proton-migration mechanism are explored. It is shown that that the model predicts that anomalous current transients should occur for a non-constant gate bias. Stirred by this prediction, experiments were performed that indeed showed these anomalous current transients. The current transients can be quantitatively modeled with the same parameters as the bias-stress effect.

In Chapter 6, it is shown that application of a prolonged gate bias also leads to a subtle change in the shape of the transfer curves implying that the mobility of charge carriers changes during bias stress. It is shown that the subtle change in shape of the curve can be used to identify the location of the trapped charges. Simulations of the charge transport in the Coulomb field of the trapped charges cannot reproduce this subtle change if the trapped charges are located in or close to the monolayer. Agreement is only found for a finite penetration depth of the trapped charges into the dielectric. The conclusion that charge trapping takes place in the bulk of the dielectric is in line with the proton-migration mechanism for the bias-stress effect.

The production of protons in the accumulation layer of the transistor should depend on the energy of the Highest Occupied Molecular Orbital (HOMO) of the organic semiconductor. In Chapter 7, an expression is derived for the dependence of the time scale of the bias-stress effect on the HOMO energy of the semiconductor. It is shown that this time scale decreases exponentially with increasing HOMO energy of the organic semiconductor. This trend is in agreement with the observed experimental trend.

Finally, the conclusions and an outlook are presented in Chapter 8.

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Chapter 2

The bias-stress effect in organic field-effect transistors

The purpose of this chapter is to introduce the reader to the operational instability in organic field-effect transistors known as the bias-stress effect. During prolonged application of a gate bias, this effect is manifested as a gradual shift of the threshold voltage towards the applied gate bias voltage. The time scale over which the shift occurs depends strongly on the ambient conditions. The shift is completely reversible and the backward shift upon removal of the gate bias occurs on a time scale similar to that of the bias-stress effect. The bias-stress effect severely limits the commercial introduction of organic field-effect transistors. In this chapter, we present the main aspects of the bias-stress effect observed in p-type organic field-effect transistors with silicon-dioxide as the gate dielectric. We describe some of the mechanisms that were proposed as an explanation of the effect. We show that there are many aspects of the effect that cannot be explained by the previously suggested mechanisms. Finally, we present experimental studies that lead to the identification of water as being the primary cause of the bias-stress effect.

2.1   Reliability of organic field-effect transistors

Over the last decade, organic field-effect transistors (OFETs) have become an integral part of an emerging technology enabling integration of electronic functionalities on flexible, plastic substrates. They are presently introduced in ultra low-cost contactless identification transponders (electronic barcodes) and in pixel drivers of flexible active matrix displays.[1–3] Optimization of material properties and device architecture has enabled rapid movement of OFETs towards their use in applications. However, their reliability under atmospheric as well as electrical operating conditions is still impeding commercialization. Much of the effort in the past has focussed on development of materials having a high field-effect mobility and good environmental stability. In fact, some of the recently developed materials exhibit much improved environmental stability and device shelf life. On the other hand, OFETs also display an electrical instability under application of a prolonged gate bias. Unlike environmental instability, the electrical instability in OFETs is reversible and is manifested only during application of a prolonged gate bias. During operation, i.e. under application of a prolonged gate bias, the source-drain current decreases monotonically with time. As we mentioned in the previous chapter, the source-drain current in OFETs depends on the applied gate bias as well as on the threshold voltage. The threshold voltage is a measure of the applied gate bias at which a transistor switches to the on-state. The decreasing source-drain current is due to a shift of the threshold voltage with time, which finally leads to a disfunctioning of the transistor. This highly undesirable effect is referred to as the "bias-stress effect". As an example, in an active matrix display, where light emission from each pixel is proportional to the current supplied by the driving transistor, any change in source-drain current with time is going to impact the brightness of the pixel.

The bias-stress effect has been studied for many organic semiconducting materials and device structures. In a typical bias-stress measurement a constant bias is applied to the gate electrode over a certain period of time. This period of time (stressing period) can vary from hours to days, depending on the ambient conditions and temperature. This will be discussed further later in the chapter. All the measurements reported in this section were done on a *p*-type transistor with polytriarylamine (PTAA) as the organic semiconductor. The gate dielectric used was SiO_2. The gate bias during stressing was -20 V and the source-drain bias was -3 V. The source-drain current during a stress experiment is shown in Fig. 2.1. It is clear from the figure that during stressing the source-drain current monotonically decreases. This decreasing source-drain current is due to the shift of the threshold voltage with time. The threshold voltage as a function of time is obtained by measuring the transfer curves during the experiment. A typical measurement of a transfer curve would proceed as follows. The prolonged application of a gate bias is briefly interrupted (for a few seconds) by a period during which a source-drain bias is applied to the transistor and the gate voltage is swept from positive to negative values. This measurement yields the source-drain current as a function of gate voltage for a given source-drain bias. Once a transfer curve has been measured, the gate voltage is set back to the original gate bias and stressing continues. This process of measuring transfer curves is repeated several times during the course of time (stressing period). A set of such measurements is shown in Fig. 2.2. As shown in Fig. 2.2, the main effect of applying a prolonged gate bias is a shift of the transfer curves. The threshold voltage can be extracted by extrapolating the linear part
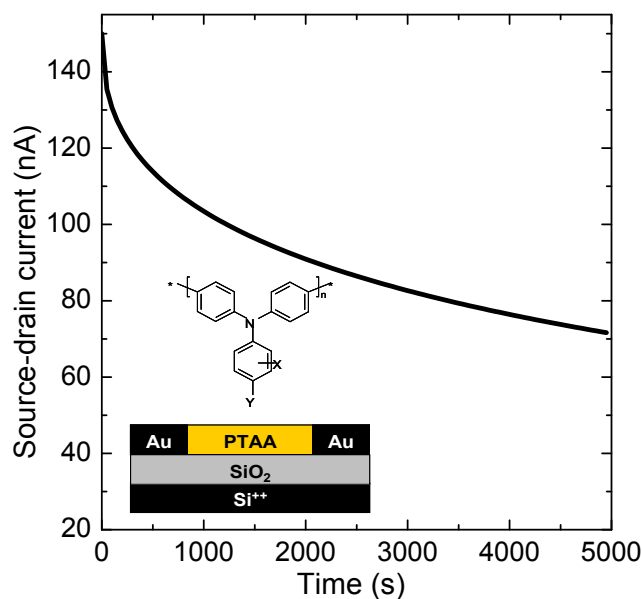
Figure 2.1: Source-drain current of a polytriarylamine (PTAA) transistor as a function of time during gate bias stress. The transistor is in ambient atmosphere at a temperature of 30 °C. The gate bias $V_{G0} = -20$ V and the source-drain voltage is $V_{SD} = -3$ V. The inset shows the schematic cross section of the transistor and the chemical structure of PTAA, where X and Y are short alkyl side chains. The transistor has a channel width and length of 2500 and 10 μm, respectively. The thickness of the organic semiconductor and the SiO$_2$ gate dielectric is 80 and 200 nm, respectively.
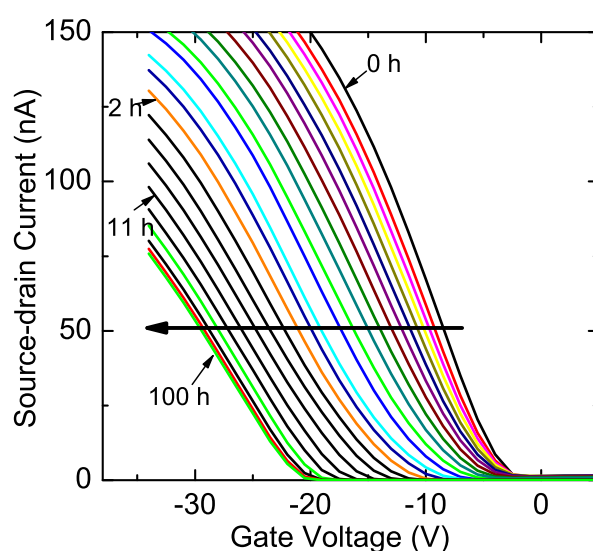
Figure 2.2: Transfer curves of the transistor after different stressing times, indicated in hours (h). The arrow indicates the direction of the shift of the transfer curves.
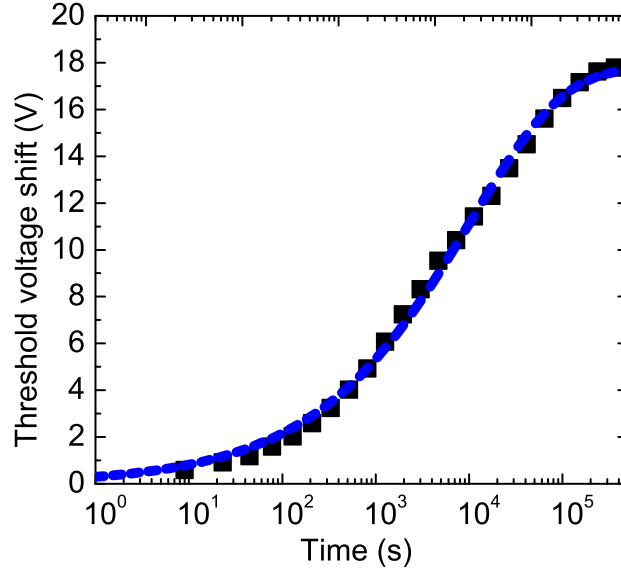
Figure 2.3: Symbols: experimental threshold-voltage shift $\Delta V_{th}(t)$ vs. time t extracted from Fig. 2.2. Dashed blue line: fit to a stretched-exponential function Eqn. (2.1). The fitting parameters are $\beta = 0.43$, $\tau = 10^4$ s, and $V_0 = 19$ V.

of these transfer curves to the gate voltage axis. The threshold-voltage shift obtained from Fig. 2.2 is shown in Fig. 2.3. In studies of the bias-stress effect it has become customary to describe the threshold-voltage shift $\Delta V_{th}(t)$ with a stretched-exponential function,[4–6]

$$\Delta V_{th}(t) = V_0 \left(1 - \exp[-(t/\tau)^\beta]\right). \qquad (2.1)$$

This fitting practice is analogous to the analysis used to describe threshold-voltage shifts in amorphous silicon-based field-effect transistors. In analyzing threshold-voltage shifts in OFETs, β and τ are treated as fitting parameters. V_0 is close to the applied gate bias voltage. τ is referred to as relaxation time. It is essentially a measure of the time scale of the threshold-voltage shift in OFETs. β is an exponent and an indicator of the non-exponential behavior of the threshold-voltage shift. This fitting procedure is useful when comparing the stability of different OFETs. The fitting procedure provides no information on the physical parameters that determine τ and β.

Below we mention important aspects of the bias-stress effect in OFETs with SiO_2 as the gate dielectric. These aspects will be discussed in more detail in the following chapters.

1. Humidity has a profound influence on the bias-stress effect. Under vacuum conditions, with practically no water present on the SiO_2 interface, the bias-stress effect is greatly slowed down.[5–9] This is evident from the relaxation time of $\tau = 2 \times 10^6$ s, obtained from the bias-stress measurements on a PTAA transistor in vacuum.[6] This value is more than two orders of magnitude larger than the value of $\tau = 10^4$ s in ambient (see Fig. 2.3). Furthermore, pretreatment of the SiO_2 with hydrophobic hexamethyldisilazane (HMDS)

or octadecyltrichlorosilaneis (OTS) is known to decelerate the effect.[10,11] Use of a hydrophobic organic gate dielectric practically eliminates the effect,[8] while coverage of the SiO_2 with a layer that is impenetrable to water does the same.[12]

2. The bias-stress effect is reversible and the reverse process is known as "recovery". Transistors that have been exposed to stressing undergo recovery when the gate bias is set to zero. With time, the threshold voltage shifts back towards its original value prior to stressing. The time scale of recovery is similar to that of the bias-stress effect.[6]

3. The dynamics of the threshold-voltage shift during stressing does not depend on the source-drain bias.[6] This was demonstrated in a study in which the source-drain current of a device undergoing stress was monitored under constant source-drain bias and then compared to the case when the gate bias was kept constant but the source-drain bias was switched off from time to time during the stressing period. It was found that switching off the source-drain bias during stressing had no impact on the source-drain current, which was identical to that obtained with a constant source-drain bias.[6]

4. The dynamics of the threshold-voltage shift during stressing does not depend on the gate voltage. Applying a different gate voltage during stressing only leads to a change of the prefactor V_0 in the stretched-exponential fit.[6]

5. The dynamics of the bias-stress effect has been measured at various temperatures.[6] It was found that for transistors with SiO_2 as gate dielectric and PTAA as the semiconductor, the relaxation time τ decreases exponentially with increasing temperature, with an activation energy of about 0.6 eV. The exponent β increases slowly with increasing temperature.[6] Interestingly, OFETs of other organic semiconducting polymers, such as poly-3-hexylthiophene (P3HT), poly-thienylene-vinylene (PTV), and poly-dioctyl-fluorene-co-bithiophene (F8T2) show under identical conditions thermally activated behavior with the same activation energy of about 0.6 eV.[6]

2.2   Proposed mechanisms for the bias-stress effect

One of the most commonly proposed mechanisms for the bias-stress effect is the charge trapping mechanism in which traps are located either in the channel or at the interface with the dielectric. Other explanations are pairing of mobile carriers to form bipolarons in the semiconductor,[13,14] charge localization by water-induced polaron formation,[15] and contact degradation.[16] We will now briefly discuss these mechanisms.

2.2.1   Trapping in channel or dielectric interface

Prior to this thesis, many mechanisms have been suggested for the bias-stress effect. The general line of argument is that charges in the channel of the transistor are gradually trapped, giving rise to the observed threshold-voltage shift over time. The location of the traps could be

in the semiconductor at the grain boundaries,[17,18] at the semiconductor/dielectric interface,[19] or in the bulk of the semiconductor.[20] Normal trapping in a semiconductor, with a typical capture cross-section of the order of 10^{-16} cm^2, is generally too fast to explain stress effects because equilibrium between the free and trapped carriers is established by the time the channel is fully populated.[13] Slow trapping in the dielectric should occur by tunneling, where the exponential dependence of the tunneling probability on distance provides the long time scale.[21] The nature of the trapping mechanism is not clear, but based on experiments the following features of trapping have been proposed:

1. A wide distribution of trapping time constants. The dynamics of the bias-stress effect becomes increasingly slower with time.[6] This implies that there is a wide distribution of trapping time-constants. At the beginning of stress, traps with small time constants are filled. As time proceeds, traps with increasingly higher trapping time constants get filled. A mechanism to provide a wide distribution in trapping time constants is to have either a distribution of energy barriers or a distribution of distances between the conducting holes and the traps, or a combination of both.

2. The absence of a trap-filling effect. The bias-stress effect occurs for any value of the applied gate bias. The threshold voltage shifts all the way to the applied gate bias, no matter matter how strongly negative this bias is chosen. This implies that either the number of available traps is practically unlimited or that traps are created dynamically during the stressing process. An experimental observation is that if the number of traps is reduced by passivating the surface of SiO$_2$, the bias-stress effect is not eliminated but only slowed down.[8,10–12]

The mechanisms based on trapping of charges in the channel or at the interface with the gate dielectric have focussed primarily on one aspect of the bias-stress effect, namely on explaining the threshold-voltage shift during application of a constant gate bias. On considering the other known aspects of the bias-stress effect we find that they cannot straightforwardly be explained by these trapping mechanisms:

1. If the bias-stress effect is associated with the trapping of charges in the channel, recovery should be associated with detrapping of these charges on grounding the gate electrode. Since the bias-stress effect is monotonous, with the threshold voltage shifting all the way to the applied gate bias, it is expected that "recovery" proceeds at a much different rate than the bias-stress effect. On the contrary, experiments show that the time scale of recovery is similar to that of the bias-stress effect.[6,22]

2. If the bias-stress effect is due to trapping of charges in the channel of the transistor, it is not clear why the activation energy should be independent of the semiconductor used.

2.2.2 Bipolaron mechanism

The bipolaron mechanism for the bias-stress effect is based on the following idea. During prolonged application of a gate bias, two holes in the channel of the transistor form a tightly

bound state that is either nonconducting or of very low mobility.[13] This paired hole state is called a bipolaron. The pairing occurs by a shared lattice distortion, which causes an energy gain when two holes are on the same site. The formation of bipolarons is analogous to trapping in the sense that the tightly bound state is immobile. Also, the Coulomb repulsion between the two holes should give a very small capture cross section for bipolaron formation and therefore to long trapping times, in accordance to what is observed in the bias-stress effect. Break-up of the bipolaron should occur by tunneling through the large energy barrier caused by the Coulomb repulsion and should therefore be slow. This could explain the long time scale involved in the recovery. The bipolaron mechanism could also account for the absence of a trap-filling effect, since the number of bipolarons that can be formed is unlimited.

According to the bipolaron mechanism, the following reaction occurs between holes, h, in the channel of the transistor:

$$h + h \rightarrow (hh)_{BP}, \tag{2.2}$$

where hh_{BP} is the bipolaron state. The rate equation for the hole concentration, N_h, is given as

$$\frac{d}{dt}N_h = -kN_h^2 + bN_{BP}, \tag{2.3}$$

where the first term on the right accounts for bipolaron formation and the second term for the break-up of bipolarons of concentration N_{BP}, with k and b the corresponding rate constants.

On a short time scale, the time scale for which threshold voltage shift is less than 10% of its total shift, the experimentally measured rate of the decrease of hole concentration, dN_h/dt, follows Eqn (2.3).[13] In other words, the rate at which the threshold-voltage shift occurs is proportional to the square of the hole concentration in the channel. The bipolaron mechanism can also explain illumination-induced recovery in a transistor with the polymer poly(9-9'-dioctyl-fluorene-co-bithiophene) (F8T2) as the organic semiconductor. The idea is that the absorbed light creates free electron-hole pairs in the polymer. The bipolaron state has a double positive charge to which an electron is strongly attracted. The electron recombines with one of the holes and a mobile hole is left.[13]

Although the bipolaron mechanism can explain some aspects of the bias-stress effects, there are various experimental observations that cannot be explained by this mechanism:

1. For longer time scales, when the threshold-voltage shift is more than 50% of the total final shift, the rate at which the threshold-voltage shift occurs is proportional to the fourth power of the gate voltage.[23] This would suggest that four holes are involved in the trapping proces. This is highly unlikely, because of the high Coulomb energy penalty associated with a quartet hole state.

2. Illumination-induced recovery has been observed only for F8T2 and no such effect was observed in pentacene transistors.[13] Illumination-induced recovery has not been reported for any other polymer.

3. The bipolaron binding energy should vary with the organic semiconductor, whereas the activation energy of the bias-stress effect is apparently independent of the organic semi-conductor.[6]

4. In regioregular polythiophenes, the energy gain involved in bipolaron formation should be very small because of the delocalization of the holes arising from the $\pi - \pi$ stacking in the two-dimensional structure of the ordered lamellae. Consistent with this finding is the fact that bipolarons are not identified in the absorption spectra of regioregular polythiophene,[24] whereas transistors with regioregular polythiophene as the organic semiconductor show a threshold-voltage shift during bias-stress.[13]

5. The bias-stress effect is also present in single-crystal OFETs.[25] In single-crystal semiconductors bipolaron formation is unlikely, due to the relatively larger delocalization of holes than in disordered polymer semiconductors.

2.2.3 Water-induced polaron formation

Recently, Cramer *et al.*[15] performed quantum-mechanical molecular simulations to study the formation of water-induced polarons at the pentacene surface. Traces of water are always present either at the interface between the dielectric and the pentacene film or within the nanocavities that may exist in the pentacene film.[26,27] Coulomb forces couple the water dipoles to the electronic structure of the semiconductor. It was shown that the presence of water induces amorphous band tails in the semiconductor. Interestingly, water polarization leads to a polaronic trap state with an average binding energy of 0.6 eV, which is comparable to the activation energy barrier in temperature-dependent bias-stress measurements. This result for pentacene can be generalized to other organic semiconductors, as the polaron binding energy depends only on the polarization of water and on the spatial extension of the hole charge. However, water polarization occurs on a very fast time scale ($<$0.5 ps) and therefore cannot account for the bias-stress effect, which occurs on a much longer time scale.

2.2.4 Contact degradation

The relative arrangement of the charge injecting source/drain contacts with respect to the charge accumulation layer at the interface influences the device degradation upon application of a gate bias.[16] Using scanning Kelvin probe microscopy, a real-time measurement of the potential drop near the source and drain contacts was performed.[16] Two types of device architectures were investigated: a coplanar and a staggered architecture. In the coplanar device configuration, the source and drain contacts are patterned on the gate dielectric before deposition of the semiconductor atop. In the staggered configuration, the source and drain contacts are put on top of the organic semiconductor. Based on their measurements, the authors claim that in coplanar device configurations an increase in source contact resistance during current flow is primarily responsible for a rapid device degradation. On the other hand, in staggered device configurations, the current reduction is significantly lower and is attributed to charge trapping in the channel, leading to an increase in the threshold voltage. In the staggered device configuration, the contacts do not exhibit a significant degradation upon bias stress.[16] The authors did not suggest any mechanism for the increase in contact resistance on application of

a gate bias. Also no explanation was provided for the observed time scale of the device degradation and the factors influencing it. Moreover, the question whether the observed degradation is reversible or not was not addressed.

Except for the mechanism based on water-induced polaron formation, none of the mechanisms discussed up to now identifies water as an important factor in the bias-stress effect. In the next section we will briefly describe experiments that highlight the important role played by water.

2.3   The role of water in the bias-stress effect

Gomes *et al.*[27] demonstrated that water on the surface of SiO_2 is highly likely to be the main factor responsible for the bias-stress effect observed in OFETs. Current measurements as a function of temperature were done on OFETs having SiO_2 as the gate dielectric in a bottom-contact device configuration. An anomaly occurred systematically at around 200 K while measuring the source-drain current for a fixed gate bias as a function of temperature. While heating the device, the source-drain current initially increases in a thermally activated way. However, at around 200 K a noticeable change in slope occurs, as shown in Fig. 2.4. This anomaly is observed in a variety of materials, independent of the deposition technique, and coincides with a known phase transition of supercooled water. Confined water does not freeze at 273 K but forms a metastable liquid down to this transition temperature. Fig. 2.4 shows that there are no pronounced changes in the behavior of the source-drain current with temperature near the melting temperature of 273 K. The bias-stress effect is absent below 200 K and is present only above that temperature. From these observations, the authors conclude that liquid water causes charge trapping, which then leads to the bias-stress effect.

Goldmann *et al.*[26] reported on the generation of trap states, after exposure to water, during gate bias stress with a negative voltage in pentacene single-crystal "flip-crystal" field-effect transistors with a SiO_2 gate dielectric. In devices in which a self-assembled monolayer on top of the SiO_2 provides a hydrophobic insulator surface no trap formation was observed. Their results indicated that the microscopic origin of the trap state is related to the molecular layers of water adsorbed on the SiO_2 surface.

Jurchescu *et al.*[28] reported on the influence of air on the charge-carrier conduction in pentacene single crystals. They demonstrated that absorbed water molecules create new defect states in the semiconductor that trap the injected charges.

Recently, Mathijssen *et al.*[10] performed scanning Kelvin probe microscopy measurements on bare devices consisting of an OFET electrode structure, but without depositing the organic semiconductor. The devices were made on SiO_2 with gold source and drain electrodes. Fig. 2.5 shows the potential profiles obtained when a $+10$ V bias is applied to the drain electrode, while the source and gate electrodes are grounded. With no charges present on the surface of SiO_2, the potential profile follows a step-like function with 0 V above the source electrode and $+10$ V above the drain electrode. However, as a function of time the potential profiles becomes smoother. This indicates that either positive charges are injected onto the surface of SiO_2 from the drain electrode or electrons are extracted by the drain electrode from the surface of SiO_2.
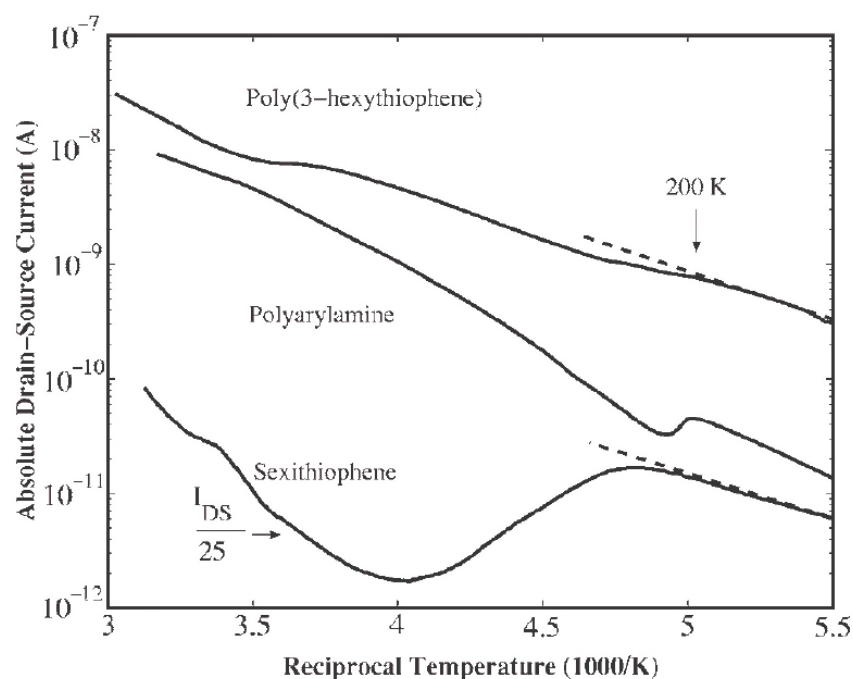
Figure 2.4: Temperature dependence of the source-drain current for three transistor devices fabricated using different active layers. The curves were measured in the linear region (typical bias voltages $V_{G0} = -10$ V and $V_{SD} = -0.5$ V). The heating rate was 2 K/min for all the curves. For clarity, the curve for sexithiophene is vertically shifted. Figure taken from Ref. [27].

Surprisingly, this effect is present for charges of both polarities at similar time scales, as shown in the inset of Fig. 2.5b, where potential profiles as a function of time are shown when the source and gate are grounded and the drain is at -10 V. The independence of the time scales on the polarity of the applied drain bias is surprising, because hole and electron trapping on SiO_2 is expected to be very different.

It is known that the SiO_2 surface has electron traps that severely limit the conduction in n-type OFETs.[29] The amount of water present at the surface of SiO_2 depends on the density of hydroxyl (OH) groups. The presence of OH groups leads to chemisorption of water on the surface of SiO_2.[30–32] Once a monolayer of water is formed, it acts as an anchor for further physisorption of water. By covering the surface of SiO_2 with hexamethyldisilazane (HMDS), the density of OH groups can be regulated. HMDS binds to the OH groups present at the SiO_2 surface. The coverage, or degree of silylation, is controlled by the exposure time to HMDS vapor. With increasing silylation, the surface becomes more hydrophobic. This is verified by measuring the contact angle of water at the SiO_2 surface.[33,34] The surface potential profiles of three substrates with water contact angles of 70, 60, and 40 degrees are shown in Figs. 2.5a-c, respectively. The rate at which the potential profile at the surface of SiO_2 evolves increases
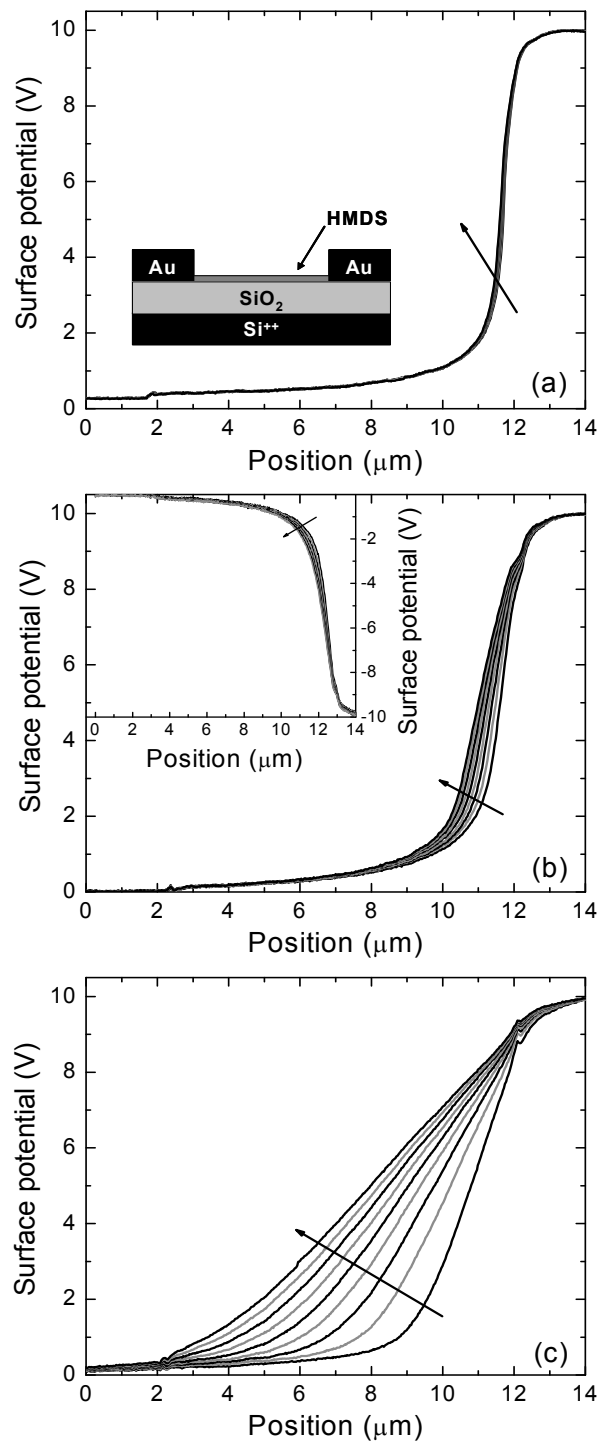
Figure 2.5: Potential profiles as a function of time for an OFET electrode structure, without deposition of the organic semiconductor. A decreasing coverage of hexamethyldisilazane (HMDS) is used in (a)-(c). The applied bias on the drain electrode is 10 V, while the source and gate electrodes are grounded at 0 V. The time step between consecutive curves is 6 seconds. The measured contact angle of a water droplet on the surface in (a)-(c) is 70, 60, and 40 degrees, respectively. The inset of (a) shows the cross section of the device layout used. The inset of (b) shows the potential profiles when −10 V is applied to the drain electrode and 0 V to the source and gate electrode.

with decreasing HMDS coverage. This indicates that indeed there are charges present on the surface of SiO_2 and that their mobility is highly dependent on the amount of water present at the surface. The potential profiles shown in Fig. 2.5a-c relax to zero if the drain electrode is grounded (not shown). The rate at which this relaxation occurs also increases with decreasing HMDS coverage.[10] Moreover, when the same set of experiments are done by purging with dry nitrogen gas, a drastic decrease in the amount of injected charges is observed along with slowing down of their kinetics. The decreasing amount of injected charges during application of a drain bias upon increasing the HMDS coverage of the surface suggests that the generally observed bias-stress effect in OFETs is due to the water present at the surface of SiO_2.

This experimental study on bare-oxide device highlights the role of water in the bias-stress effect. Moreover, the similar timescales observed in evolution of potential profiles on switching bias polarity suggests the following possibility. Maybe the charges moving on the surface of SiO_2 on application of a drain bias are neither holes nor electrons, but ions or water itself, of which the movement across the surface is the time-limiting factor. We will show in the next chapter that this is indeed the case and we then rationalize the experimental observations mentioned above.

2.4 Summary and conclusions

In this chapter we described the instability in organic field-effect transistors known as the bias-stress effect. We presented some of the early studies done on this effect. We described some of the proposed mechanisms for the effect. We argued that the earlier proposed mechanisms fail to consistently describe all the known aspects of the bias-stress effect. The identification of water as the primary agent causing this device instability is a big step forward towards understanding the effect. We will use the experimental studies described in this chapter and many other studies as well to develop a mechanism for the bias-stress effect in the next chapter.

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Chapter 3

Proton migration mechanism for the bias-stress effect

During prolonged application of a gate bias, organic field-effect transistors show an instability involving a gradual shift of the threshold voltage towards the applied gate bias voltage. The time scale over which the shift occurs depends strongly on the ambient conditions and temperature. We propose a model for the threshold-voltage shift during stressing of p-type transistors with a silicon-dioxide gate dielectric. The mechanism is based on hole-assisted production of protons in the accumulation layer and their subsequent migration into the gate dielectric. This model explains the much debated role of water and several other hitherto unexplained aspects of the instability of these transistors.[*]

3.1   Introduction

Organic field-effect transistors (OFETs) are presently introduced in ultra low-cost contactless identification transponders (electronic barcodes) and in pixel drivers of flexible active matrix displays.[1–3] Impressive progress has also been made in realizing logic circuits based on OFETs for applications in chemical or biological sensing. However, the operational instability of OFETs is impeding widespread commercial introduction.[4–17] The instability under application of a prolonged gate bias is due to a shift of the threshold voltage with time, leading to a decreasing source-drain current and finally to a disfunctioning of the transistors. This highly undesirable effect is referred to as the "bias-stress effect" and the identification of its origin is of paramount importance.[4–17]

The bias-stress effect has been extensively studied in p-type organic transistors with silicon-dioxide, SiO_2, as the gate dielectric.[4–11,13,15] SiO_2 is chosen to prevent effects of ionic movements, which are known to occur in organic gate dielectrics.[18] Nevertheless, transistors with SiO_2 as gate dielectric suffer from the bias-stress effect. The effect is usually studied by applying a constant stressing gate bias, interrupted by short time intervals in which the transfer curve – the source-drain current as a function of gate bias for a small applied source-drain voltage – is measured. The main observation in these measurements is that the whole transfer curve shifts in the direction of the constant stressing gate bias.

The threshold-voltage shift as a function of time is customarily fitted with a stretched-exponential function, as is done in similar studies on the bias-stress effect in amorphous-silicon FETs.[19] Despite the success of such a fit, there is no agreement on the microscopic mechanism behind the effect. Several mechanisms have been suggested as an explanation, such as (i) trapping of mobile carriers in the bulk of the semiconductor,[20] (ii) trapping in disordered areas of the semiconductor,[6] (iii) trapping in regions in between crystalline grains of the semiconductor,[14,21] (iv) trapping in states at the semiconductor/dielectric interface,[7] and (v) pairing of mobile carriers to bipolarons in the semiconductor.[4,22] Two other important observations are that the effect is influenced by humidity[12,13,23] and that the effect is thermally activated, with an activation energy of about 0.6 eV, apparently independent of the organic semiconductor used.[10]

One of the other interesting aspects of the bias-stress effect is that it is reversible: on applying a zero gate bias after stressing, the threshold voltage shifts back towards its original value, an effect usually referred to as "recovery". While the bias-stress effect has been thoroughly investigated, recovery has received little attention. It has been established that the dynamics of the threshold-voltage shift for recovery is different from that for stress,[10] but an explanation for this observation is still lacking.

In this chapter, we will propose a mechanism to explain the bias-stress effect. The mechanism is based on a hole-assisted reaction involving water, producing protons in the channel. The chapter is organized as follows. In Section 3.2, we present measurements of the bias-stress effect for a p-type OFET and discuss the main experimental features of the effect. In Section 3.3, we introduce the proton migration mechanism and discuss its experimental and theoretical basis. In Section 3.4, we discuss the modeling of the proton migration mechanism and its application to the bias-stress effect. Finally, Section 3.5 contains a summary and the

conclusions.

3.2 The bias-stress effect: experimental

We investigated the bias-stress effect for a p-type OFET fabricated using heavily doped p-type Si wafers as the common gate electrode, with a 200 nm thermally oxidized SiO_2 layer as the gate dielectric. Using conventional photolithography, gold source and drain electrodes were defined in a bottom-contact device configuration with a channel width (W) and length (L) of 2500 μm and 10 μm, respectively. A 10 nm thick layer of titanium was used as an adhesion layer for the gold on SiO_2. The SiO_2 layer was treated with the primer hexamethyldisilazane (HMDS) prior to semiconductor deposition in order to passivate its surface. Polytriarylamine (PTAA) films were spun from a 1% toluene solution at 2000 rpm for 20 s, resulting in a film thickness of 80 nm. The electrical characterization was carried out using an HP 4155C semiconductor parameter analyzer under conditioned ambient atmosphere at a temperature of 30 °C.

Fig. 3.1 shows the development in time of the transfer curves of the transistor, undergoing bias stress with a constant gate voltage $V_{G0} = -20$ V for a total time of 100 hours $\approx 4 \times 10^5$ s. The transfer curves were measured by interrupting the stress for brief periods of time, during which a source-drain voltage of $V_{SD} = -3$ V was applied and the gate voltage was swept. As is clearly observed, the main effect of the bias stress is a shift of the transfer curves in the direction of V_{G0}. In the course of time, the threshold voltage V_{th} (defined here as the intercept of the extrapolated linear part of the transfer curve with the voltage axis) shifts all the way down to V_{G0}. The symbols in Fig. 3.2 show the threshold-voltage shift $\Delta V_{th}(t) = V_{th}^0 - V_{th}(t)$ as a function of time t. Here, V_{th}^0 is the threshold voltage shift at the start of the experiment, which is close to zero. In studies of the bias-stress effect it has become customary to describe the shift $\Delta V_{th}(t)$ with a stretched-exponential function,[5,10,19] $\Delta V_{th}(t) = V_0 \left(1 - \exp[-(t/\tau)^\beta]\right)$, where the prefactor V_0 is close to $|V_{G0}|$, τ is a relaxation time, and $0 < \beta < 1$ an exponent. As can be seen in Fig. 3.2a this function (dashed curve) yields a very good fit. The fit parameters are $V_0 = 19$ V, $\tau = 10^4$ s, and $\beta = 0.43$.

Many studies have shown that humidity has a profound influence on the bias-stress effect. Under vacuum conditions, with practically no water present on the SiO_2 interface, the bias-stress effect is greatly slowed down.[5,10,12,23] This is evident from the relaxation time of $\tau = 2 \times 10^6$ s obtained from the bias-stress measurements on a similar PTAA transistor in vacuum,[10] which is more than two orders of magnitude larger than the above value in ambient. Furthermore, pretreatment of the SiO_2 with hydrophobic HMDS or octadecyltrichlorosilane (OTS) is known to decelerate the effect.[8,13] Use of a hydrophobic organic gate dielectric practically eliminates the effect,[12] while coverage of the SiO_2 with a layer that is impenetrable to water does the same.[9] These observations indicate that the threshold-voltage shift in organic transistors is related to residual water.

Another aspect of the bias-stress effect is that the dynamics of the threshold-voltage shift during stressing does not depend on the source-drain bias. This was demonstrated in a study in which the source-drain current of a device undergoing stress was monitored under constant source-drain bias and then compared to the case when the gate bias was kept constant but the
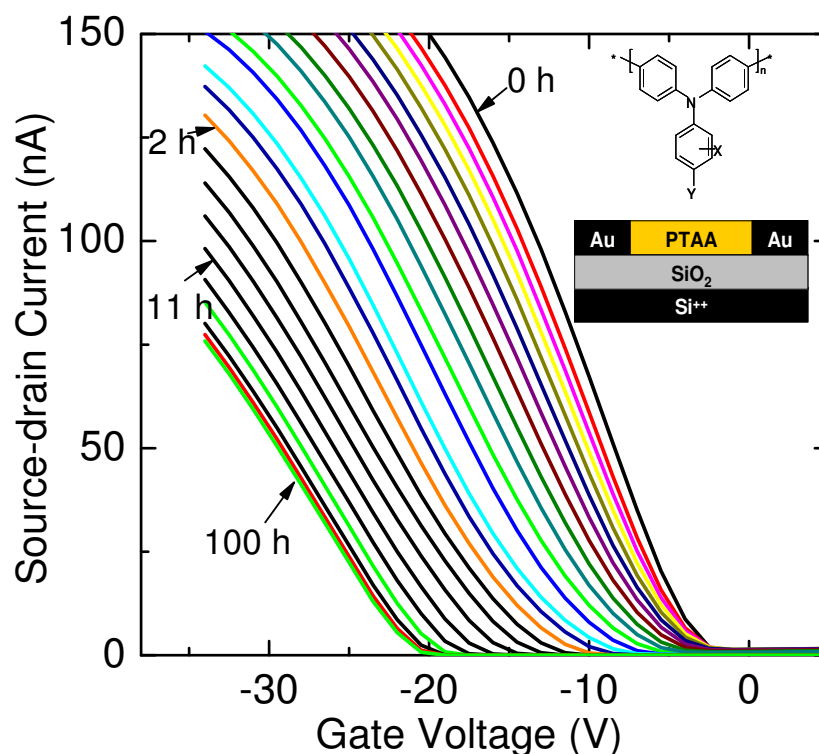
Figure 3.1: Transfer curves of a polytriarylamine (PTAA) transistor in ambient atmosphere at a temperature of 30 °C for different stressing times, indicated in hours (h). The gate bias during stressing is -20 V. The inset shows the schematic cross section of the transistor and the chemical structure of PTAA, where X and Y are short alkyl side chains. The fabrication of the transistor was equivalent to that in Ref. [10], with pretreatment of the SiO_2 surface with HMDS. The transistor has a channel width and length of 2500 and 10 μm, respectively. The thickness of the organic semiconductor and the SiO_2 gate dielectric is 80 and 200 nm, respectively.

source-drain bias was switched off from time to time during the stressing period. It was found that switching off the source-drain bias during stressing had no impact on the source-drain current, which was identical to that obtained with a constant source-drain bias.[10]

The dynamics of the bias-stress effect has been measured at various temperatures.[10] It was found that for transistors with SiO_2 as gate dielectric and PTAA as the semiconductor the relaxation time τ decreases exponentially with increasing temperature, with an activation energy of about 0.6 eV. Interestingly OFETs of other organic semiconducting polymers such as poly-3-hexylthiophene (P3HT), poly-thienylene-vinylene (PTV), and poly-dioctyl-fluorene-co-bithiophene (F8T2) showed under identical conditions thermally activated behavior with the same activation energy of 0.6 eV.[10] The independence of the activation energy on the semiconductor indicates that the bias-stress effect in transistors with SiO_2 gate dielectric has a common origin. It should be noted that although the activation energy for different semiconductors is
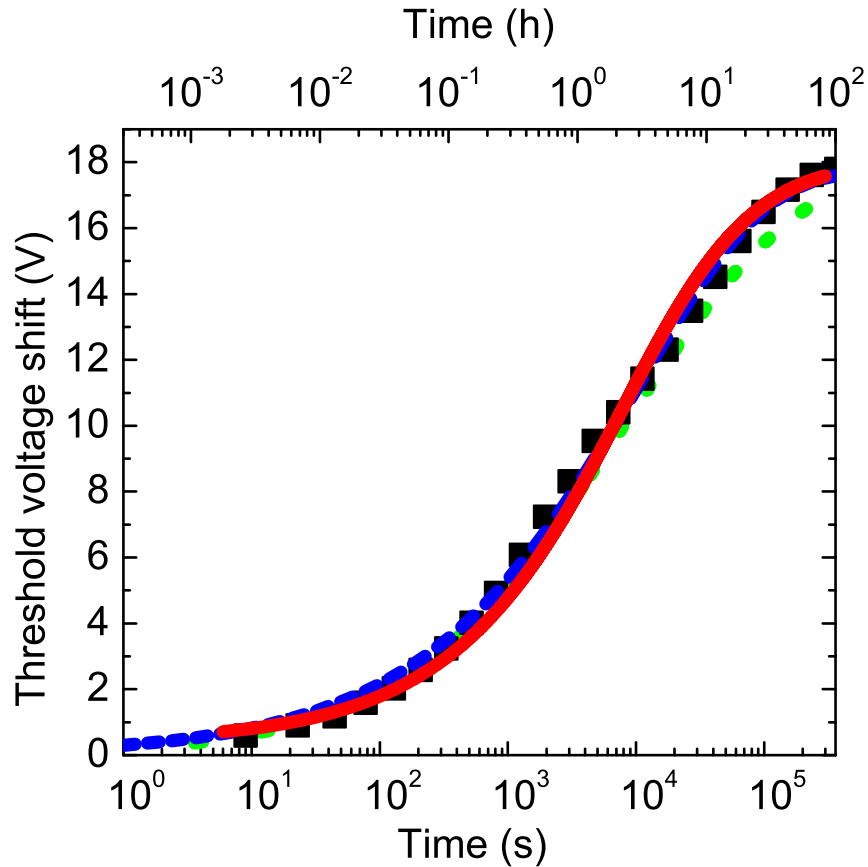
Figure 3.2: Symbols: experimental threshold-voltage shift $\Delta V_{th}(t)$ vs. time t, obtained from Fig. 2.1. Dashed blue line: fit to a stretched-exponential function with $\beta = 0.43$, $\tau = 10^4$ s, and $V_0 = 19$ V. Solid red line: fit to the drift-diffusion model, with $D = 1.6 \times 10^{-19}$ cm^2/s and $\alpha = 2.2$ nm^{-1}. Dotted green line: the same, but with the drift contribution neglected.

the same, the value of the relaxation time is different for each of the semiconductors.

3.3 Proton migration mechanism for the bias-stress effect

A strong indication that the bias-stress effect is not caused by trapping of charges in the organic semiconductor but by processes occurring on the SiO$_2$ surface comes from scanning Kelvin-probe microscopy (SKPM) measurements of the potential on a structure similar to the OFET investigated in the present chapter, but without deposition of the organic semiconductor.[13] We described this experiment in details in the previous chapter. Here, we summarize the main findings. With application of a drain bias (and a grounded source and gate) a time evolution of the potential profile at the SiO$_2$ surface was measured. The dynamics of this evolution was found to be determined by the amount of water on the SiO$_2$, which could be regulated by

treatment with HMDS.[13] The time evolution of the potential profile of this structure shows that charges can move around reversibly on the SiO_2 surface even in absence of a semiconductor. Surprisingly, the time evolution was found to occur on equal time scales for both positive and negative polarity of the drain bias.[13] Since carriers with different polarities should have different transport characteristics, this observation implies that the dynamics of the potential profile is in both cases governed by one type of charge carrier.

Surface-conductivity measurements on SiO_2 performed in the 1960s and repeated a decade ago have revealed an ionic nature of the conductivity and it was suggested that protons (H^+) that are electrolytically produced from physisorbed water are the charge carriers.[24–26] It was shown that the mobility of protons on the surface of SiO_2 increases with increasing amount of water. It was also shown that protons can be produced electrolytically from water on the SiO_2 surface by replacing water in the ambient by heavy water (D_2O) and detecting deuterium gas (D_2) after performing surface-conductivity measurements.[24] Therefore, we suggest that in the above experiments protons are responsible for the time evolution of the potential profiles. Because of the presence of silanol groups (SiOH) protons will be present on the SiO_2 surface because of the reaction $SiOH \rightleftharpoons SiO^- + H^+$, creating an acidic environment. On applying a positive bias at the drain electrode, oxidation of water occurs at this electrode, producing excess protons in the reaction

$$H_2O \rightarrow 2H^+ + 2e^- + \frac{1}{2}O_2(g). \tag{3.1}$$
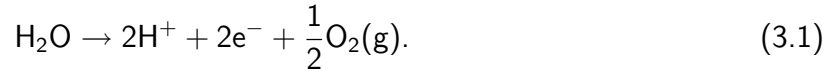
The motion of protons away from the drain electrode towards the source electrode gives rise to a positive potential profile. On the other hand, when applying a negative bias, the reaction

$$2H^+ + 2e^- \rightarrow H_2(g) \tag{3.2}$$

occurs at the drain electrode, leading to a deficit of protons. This results in a motion of protons towards the drain electrode, giving rise to a negative potential profile. Under the application of both negative and positive bias it is the motion of protons that determines the time evolution of potential profiles. This explains why the evolution of potential profiles occurs on the same time scale upon application of both negative and positive bias.

Since organic semiconductors are permeable to water,[27,28] water molecules can also reach the SiO_2 surface in the presence of an organic semiconductor. We therefore propose that in a *p*-type OFET under bias stress the electrolytic production of protons now takes place at the interface between the semiconductor and the SiO_2, where the whole accumulation layer in the semiconductor acts as a positive electrode. In this electrolytic reaction, holes in the semiconductor are converted into protons. Calculations within the framework of density-functional theory (DFT) have shown that water at the Si-SiO_2 interface can undergo oxidation to produce protons in the presence of holes.[29] Although we do not know of equivalent studies for the interface between an organic semiconductor and SiO_2, it is natural to assume that the same reaction will take place. Regarding the above discussion, it is then also natural to assume that the reverse reaction occurs in which protons are converted into holes.

The reversible motion of protons in SiO_2 has been demonstrated by memory effects occurring in Si/SiO_2/Si devices, where protons move through the SiO_2 from one Si layer to the other.[30,31]

DFT calculations on transport of protons in SiO_2 predict an activation energy of about 0.5 eV,[32] which is close to the 0.6 eV activation energy found in bias-stress experiments on different organic semiconductors.[10] This strongly suggests that proton motion in the SiO_2 determines the dynamics of the bias-stress effect.

Based on these experimental and theoretical results we propose the following scenario.

1. In the presence of water, holes in the organic semiconductor, indicated below by OS^+, can be converted into protons in the electrolytic reaction

$$2H_2O + 4OS^+ \rightarrow 4H^+ + O_2(g) + 4OS,$$ (3.3)
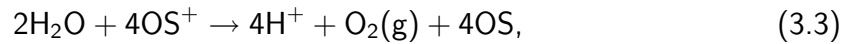
   where OS refers to electrically neutral sites in the organic semiconductor.

2. Protons can be converted back into holes in the reverse reaction[†]

$$4H^+ + O_2(g) + 4OS \rightarrow 2H_2O + 4OS^+.$$ (3.4)
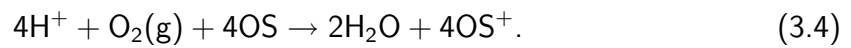
3. Protons in the accumulation layer of the semiconductor are in equilibrium with protons in the oxide at the interface with the semiconductor:

$$H^+(semi) \rightleftharpoons H^+(oxide).$$ (3.5)

4. Protons in the oxide at the interface can diffuse into the bulk of the oxide.

We note that reactions Eqns. (3.3) and (3.4) will establish an equilibrium between holes and protons in the accumulation layer. This essentially implies the reversibility of the bias-stress effect, as we will see further on. It is reasonable to assume that the dynamics of the reactions Eqns. (3.3)-(3.5) is much faster than the diffusion of protons into the bulk of the oxide. This leads to the conclusion that the dynamics of the bias-stress effect is governed primarily by the motion of protons in the oxide and not by the specific details of the reactions. Under this assumption, there will be an equilibrium between the surface density $[OS^+]$ of holes in the semiconductor and the volume density $[H^+]$ of protons in the oxide at the interface with the semiconductor, leading to the linear relation

$$[H^+] = \alpha[OS^+],$$ (3.6)

where the parameter α is a proportionality constant, which is determined by the reaction constants. We treat α as a parameter in what follows. We note that protons in the semiconductor in the presence of water probably occur in a hydrated form (H_3O^+ or more complex coordination) but this is not central to our analysis. We sketch the proton-migration mechanism

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[†]In our published articles we reported the following reaction for the conversion of protons into holes:[15,33,34] $2H^+ + 2OS \rightarrow H_2(g) + 2OS^+$. This equation, along with Eqn. (3.3), implies the continuous production of oxyhydrogen (O_2 and H_2) during stressing. Recently, we found out that Aguirre *et al.*[35] demonstrated that, under suitable conditions, the following reaction occurs reversibly in the channel of an OFET: $O_2 + 4H^+ + 4e^- \rightleftharpoons 2H_2O$. In presence of solvated oxygen we need only Eqn. (3.3) and its reverse to explain the bias-stress effect as well as recovery.
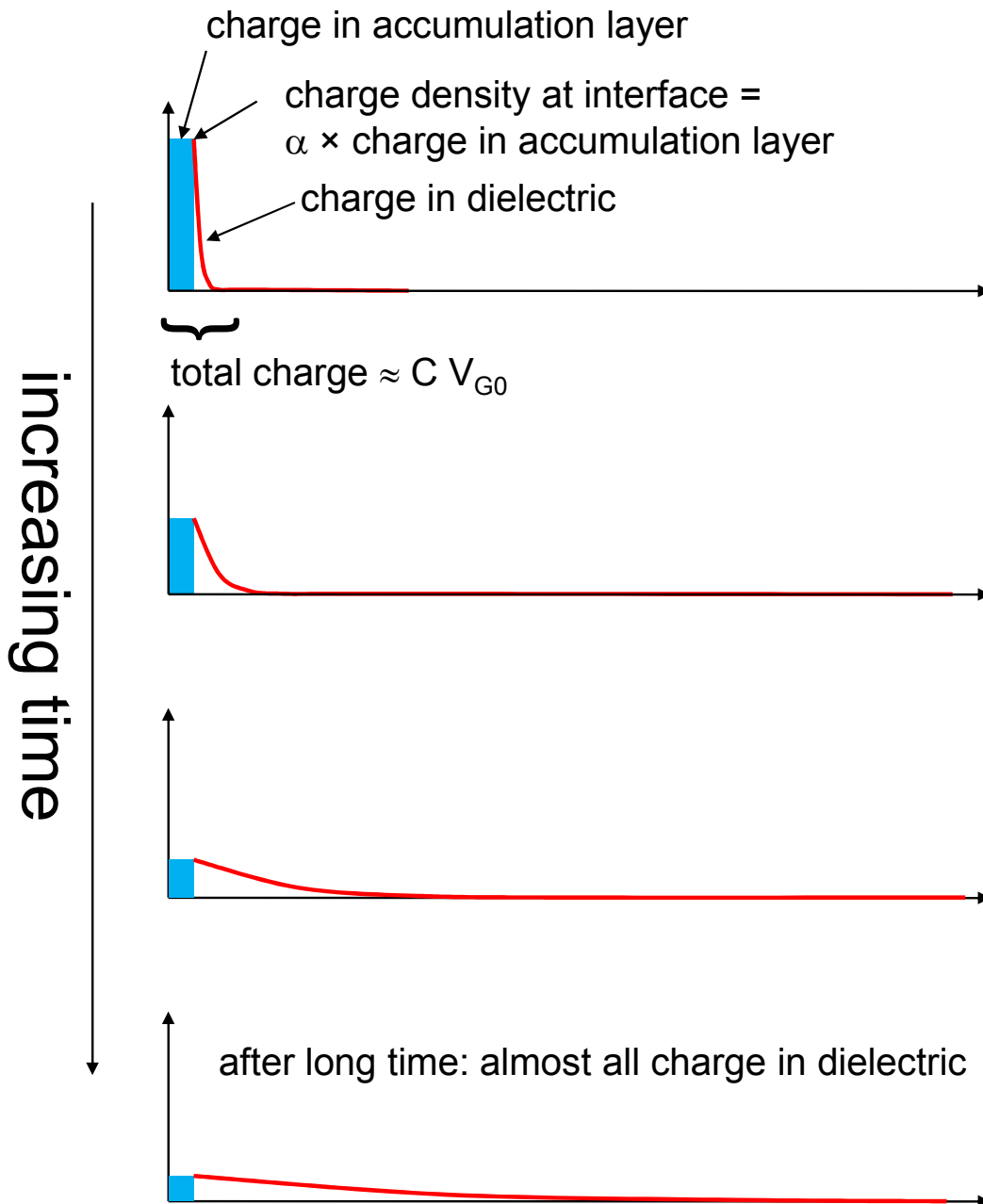
Figure 3.3: Sketch of the proton migration mechanism for the bias-stress effect. Blue bars: Hole density in the accumulation layer. Red lines: proton density in the dielectric, scaled such that the lines connect continuously to the blue bars at the interface. At time $t = 0$, charge density in the accumulation layer is CV_{G0} with C the capacitance of the oxide per unit area and V_{G0} the applied gate bias. With time, protons migrate into the dielectric. After a long time, almost all charge is present in the dielectric in form of protons.

for the bias-stress effect in Fig. 3.3. As shown in the figure, at the start of stressing, all the charge is present in the accumulation layer. With time, protons migrate into the dielectric. Correspondingly the number of holes in the accumulation layer decreases. After a long time, almost all the charge is present in form of protons in the dielectric with a vanishing hole density in the accumulation layer.

3.4   Model for the proton migration mechanism

The proposed proton migration mechanism can be made quantitative in the following way. Under the assumption that the protons do not penetrate deep into the oxide, we can write down the following charge-balance equation while stressing the OFET with a constant gate bias V_{G0}:

$$\int_0^\infty p(x, t)dx + h_0(t) = c_0 \equiv \frac{CV_{G0}}{e}, \tag{3.7}$$

where $p(x, t)$ is the time-dependent volume density of protons in the oxide at a distance x from the interface with the semiconductor, $h_0(t)$ is the time-dependent surface density of holes in the accumulation layer of the semiconductor, C is the capacitance of the oxide per unit area, and e is the elementary charge. In principle, diffusion as well as drift of protons in the oxide occurs. In the present derivation we will neglect drift and only take diffusion of protons into account. Clearly, in the initial stage after the application of a gate bias there will be a large density gradient – perpendicular to the interface with the semiconductor – of protons in the oxide, such that diffusion automatically dominates over drift. The advantage of neglecting proton drift is that a clear picture of the mechanism arises and that the modeling is considerably simplified. We can then write the equation of motion for protons in the oxide as

$$\frac{\partial}{\partial t}p(x, t) = D\frac{\partial^2}{\partial x^2}p(x, t), \tag{3.8}$$

with D the diffusion coefficient. This equation can be solved using the Green-function for the one-dimensional diffusion equation:

$$p(x, t) = \int_0^t \int_{-\infty}^\infty \frac{\exp\left[-\frac{(x-x')^2}{4D(t-t')}\right] s(x', t')}{\sqrt{4\pi D(t - t')}} dx' dt', \tag{3.9}$$

where $s(x, t)$ stands for the source term, which is equal to the proton flux into the oxide from the accumulation layer. This source term can be obtained by differentiating Eqn. (3.7) with respect to time and using Eqn. (3.8):

$$
\begin{aligned}
s(x, t) &= -2D\frac{\partial p(x, t)}{\partial x}\bigg|_{x=0} \delta(x), \\
&= -2\frac{dh_0(t)}{dt}\delta(x), \tag{3.10}
\end{aligned}
$$

where the factor 2 is related to the fact that we consider a diffusion problem in a half-space $x \geq 0$. Using the equilibrium condition $p(0, t) = \alpha h_0(t)$ and the above expression for the source term, we can calculate the proton density in the oxide at the interface as

$$p(0, t) = \int_0^t \frac{1}{\sqrt{4\pi D(t - t')}} \left(-\frac{2}{\alpha} \frac{dp(0, t')}{dt'} \right) dt'. \tag{3.11}$$

On applying partial integration and replacing $p(0, t)$ with $\alpha h_0(t)$, we obtain the following equation for the hole density in the accumulation layer:

$$h_0(t) = \frac{1}{2} \int_0^t \frac{t_0^{1/2}}{(t - t')^{3/2}} (h_0(t') - h_0(t)) dt' - \left(\frac{t_0}{t} \right)^{1/2} (h_0(t) - c_0), \tag{3.12}$$

where the characteristic time t_0 is given by

$$t_0 \equiv \frac{1}{\pi \alpha^2 D}. \tag{3.13}$$

We note that, unlike the relaxation time τ in the stretched-exponential fits to the threshold-voltage shifts discussed in Section 3.2, this characteristic time is related to physical parameters.

Eqn. (3.12) can be solved for $h_0(t)$ by iterative numerical techniques. The threshold voltage is finally obtained as

$$V_{\text{th}}(t) = \frac{e}{C}(c_0 - h_0(t)). \tag{3.14}$$

The application of the model to the threshold-voltage dynamics during stressing discussed in Section 3.2 leads to the dotted green line in Fig. 3.2 for the case that only proton diffusion in the oxide is taken into account. For this case the dynamics of the threshold-voltage shift is described by a universal curve with t_0 as the only parameter. This fact is in agreement with the experimental observation that the dynamics of the bias-stress effect is virtually independent of the value of the applied gate voltage.[10] For the present case, we are able to obtain a good fit up to $t \approx 10^4$ s and extract $t_0 = 4.2 \times 10^3$ s.

The deviation from predictions of the diffusion model observed in Fig. 3.2 for longer times should be attributed to proton drift in the oxide. In order to take into account drift we must solve the full drift-diffusion equation for the motion of the protons. In order to do so, we need to estimate the diffusion constant and α individually. The drift component of the proton flux into the oxide can be written as $J_{\text{drift}}(t) = \mu p(0, t) E(0, t)$, where μ is the mobility of the protons and $E(0, t)$ is the electric field at the interface. On expressing $p(0, t)$ and $E(0, t)$ in terms of V_{G0} and $V_{\text{th}}(t)$, we get

$$J_{\text{drift}}(t) = \mu \alpha \frac{C(V_{\text{G0}} - V_{\text{th}}(t))^2}{eL_{\text{ox}}}, \tag{3.15}$$

where L_{ox} is the thickness of the oxide layer. In our model, the diffusive component of the flux is given by

$$\begin{aligned} J_{\text{diff}}(t) &= -D \frac{\partial}{\partial x} p(x, t)|_{x=0}, \\ &= -\frac{d}{dt} h_0(t) = \frac{C}{e} \frac{d}{dt} V_{\text{th}}(t). \end{aligned} \tag{3.16}$$

Deviations from our model predictions occur when the drift component becomes comparable to the diffusive component. Assuming that this happens from $t = t_{\text{dev}}$ onwards, we obtain by equating Eqns. (3.15) and (3.16) at $t = t_{\text{dev}}$:

$$\mu\alpha = \frac{L_{\text{ox}}}{(V_{G0} - V_{\text{th}}(t_{\text{dev}}))^2} \frac{d}{dt} V_{\text{th}}(t)|_{t=t_{\text{dev}}}. \tag{3.17}$$

Using Einstein's relation, $D/\mu = k_B T/e$, Eqn. (3.17), and the definition of t_0, Eqn. (3.13), we find

$$\alpha = \frac{e}{k_B T} \frac{(V_{G0} - V_{\text{th}}(t_{\text{dev}}))^2}{\pi t_0 L_{\text{ox}} \frac{d}{dt} V_{\text{th}}(t)|_{t=t_{\text{dev}}}}, \tag{3.18}$$

$$D = \left(\frac{k_B T}{e}\right)^2 \frac{\pi t_0 L_{\text{ox}}^2}{(V_{G0} - V_{\text{th}}(t_{\text{dev}}))^4} \left(\frac{d}{dt} V_{\text{th}}(t)|_{t=t_{\text{dev}}}\right)^2. \tag{3.19}$$

By taking $t_{\text{dev}} \approx 10^4$ s and the experimentally determined $V_{\text{th}}(t = t_{\text{dev}})$ and $\frac{d}{dt} V_{\text{th}}(t)|_{t=t_{\text{dev}}}$, we obtain $\alpha \approx 2$ nm^{-1} and $D \approx 10^{-19}$ cm^2/s. We are not aware of any measurements of the diffusion coefficient of protons in our gate dielectric consisting of dry amorphous thermally grown SiO$_2$, but the value we find is very close to the diffusion coefficient for protons in Si$_3$N$_4$.[36]

We also directly numerically solved the drift-diffusion equation for protons in the oxide:

$$\frac{\partial}{\partial t} p(x, t) = \mu p(x, t) E(x, t) - D \frac{\partial}{\partial x} p(x, t). \tag{3.20}$$

The threshold voltage can be calculated using:

$$V_{\text{th}}(t) = \frac{e}{\epsilon} \int_0^{L_{\text{ox}}} (L_{\text{ox}} - x) p(x, t) dx, \tag{3.21}$$

where ϵ is the dielectric constant of the oxide. The electric field at any point in the oxide can be obtained using Poisson's equation:

$$\begin{aligned} E(x, t) &= E(0, t) + \frac{e}{\epsilon} \int_0^x p(x, t) dx, \\ &= \frac{V_{G0} - V_{\text{th}}(t)}{L_{\text{ox}}} + \frac{e}{\epsilon} \int_0^x p(x, t) dx. \end{aligned} \tag{3.22}$$

The normalized version of the equations shown above is described in Appendix A. As shown by the solid red line in Fig. 3.2, an excellent fit to the experimentally determined time dependence of the threshold voltage is obtained when the drift-diffusion problem is solved with $D = 1.6 \times 10^{-19}$ cm^2/s and $\alpha = 2.2$ nm^{-1}. For these values of D and α, we show the proton density profile in the gate oxide for different times in Fig. 3.4a. The penetration depth of the protons into the oxide is about 30 nm at the end of stressing in Fig. 3.1 ($t = 100$ hours $\approx 4 \times 10^5$ s). This is much smaller than the oxide thickness of 200 nm and hence consistent with our assumption that the protons do not penetrate deep into the oxide. The results displayed in Fig. 3.2 show
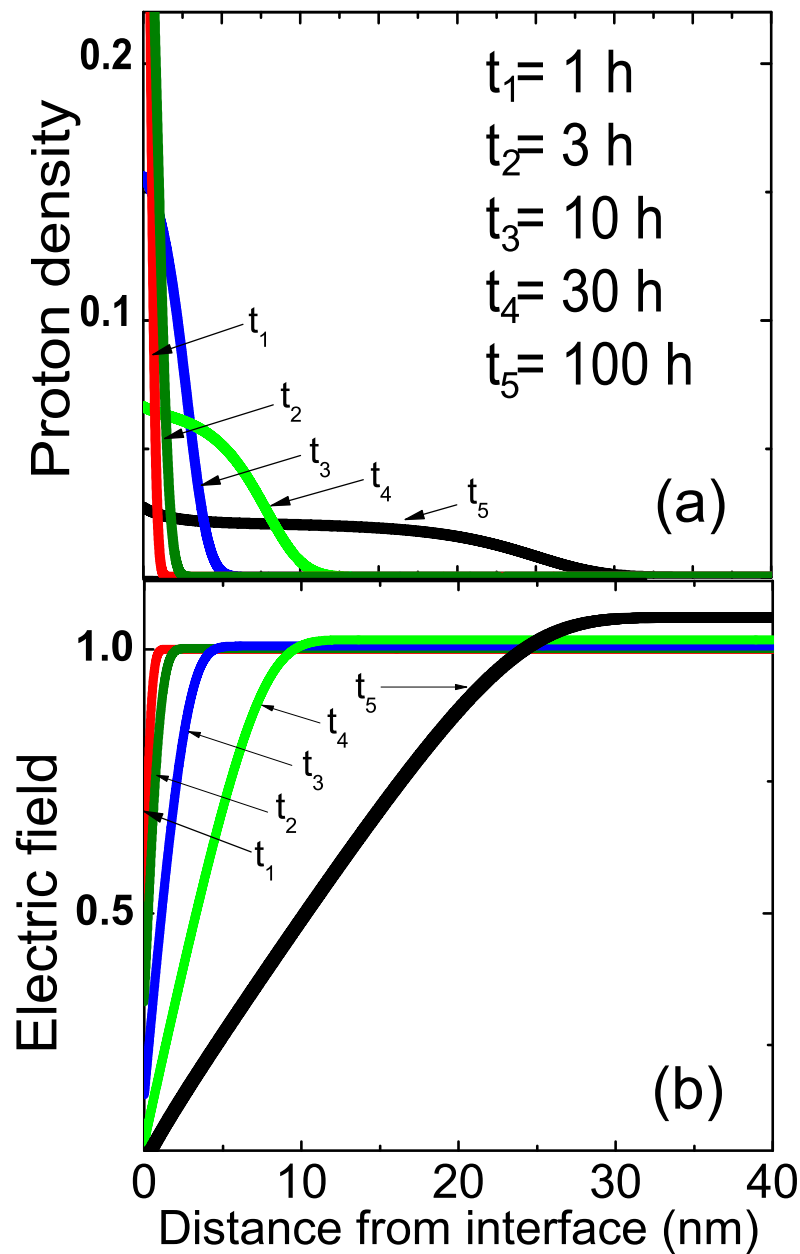
Figure 3.4: (a) Proton density profile $p(x, t)/p(0, 0)$ and (b) electric field profile $E(x, t)/E(0, 0)$ in the oxide at different times after the start of stressing, for a numerical solution of the drift-diffusion problem related to the proton migration mechanism.

that the diffusive flux of protons into the oxide dominates over the drift flux of protons till $t \approx 10^4$ s. We show in Fig. 3.4b the electric field profile in the oxide for different times. Since most of the proton charge stays close to the interface between the organic semiconductor and the oxide, the electric field varies strongly with distance near the interface, whereas there is practically no change in its value far from the interface.

The proton-migration mechanism described in this chapter is developed specifically for *p*-type organic field-effect transistors with silicon-dioxide as gate dielectric and a polymer as the organic semiconductor. *n*-type OFETs are also known to exhibit the bias-stress effect.[37] The bias-stress effect is also observed in OFETs with a gate dielectric different than silicon-dioxide,[18] in single-crystal OFETs with silicon-dioxide as the gate dielectric[38] as well as in amorphous silicon thin-film transistors.[39–41] In this thesis, we have not addressed these cases. However, it should be possible to extend the proton migration mechanism to these cases as well.

3.5 Summary and conclusions

We developed a model for operational instabilities involving threshold-voltage shifts in *p*-type organic field-effect transistors with silicon-dioxide as gate dielectric based on a proton migration mechanism. The model is based on the assumption that an equilibrium exists in the accumulation layer of the organic semiconductor between holes and protons, because of reactions taking place involving these species and water, and on the assumption that protons can migrate into the oxide, leading to a shielding of the gate electric field.

The model can very accurately describe the bias-stress effect in these transistors, which is manifested as a shift of the threshold voltage towards a constant stressing gate voltage. Because of the large proton density gradient in the oxide, the diffusion contribution of the protons dominates over the drift contribution. In the case that the drift contribution is neglected, the dependence of the threshold voltage on time follows a universal curve, with a characteristic time as the only parameter. This universal curve is very close to a stretched-exponential function, which explains the success of the description of the shift of the threshold voltage with time in terms of such a function. The model explains the role of water and the observation that the activation energy of the bias-stress effect is virtually independent of the organic semiconductor. The magnitude of the activation energy agrees with a calculated value for transport of protons in the silicon-dioxide.

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Chapter 4

Recovery of stressed organic field-effect transistors

Organic field-effect transistors exhibit operational instabilities involving a shift of the threshold gate voltage when a gate bias is applied. For a constant gate bias the threshold voltage shifts towards the applied gate bias voltage, an effect known as the bias-stress effect. On applying a zero gate bias to a device that has been exposed to stress, the threshold voltage shifts back to its original value prior to stressing. This phenomenon is known as recovery. We associate both the bias-stress effect and recovery with a reversible reaction in the organic semiconductor in which holes are converted into protons in the presence of water, and a reversible migration of these protons into the gate dielectric. We show how a shorter period of application of a gate bias leads to a faster backward shift of the threshold voltage when the gate bias is removed.*

4.1 Introduction

Organic field-effect transistors (OFETs) exhibit an operational instability known as the bias-stress effect, which involves a shift of the threshold voltage towards the applied gate bias.[1–14] This instability is a severe bottleneck in their commercial introduction. In the previous chapter, we proposed a mechanism for the bias-stress effect in OFETs. The model is based on the production of protons in the accumulation layer of the transistor from holes and water, and the subsequent migration of these protons into the gate dielectric.[12] We showed that the resulting model quantitatively explains the observed stretched-exponential dependence of the threshold-voltage shift with time. The model also explains various other aspects of the bias-stress effect, such as the activation energy of about 0.6 eV, independent of the semiconductor,[7] and the influence of water.[2,5,9,10,15–17] An interesting aspects of the bias-stress effect is that it is reversible: on applying a zero gate bias after stressing, the threshold voltage shifts back towards its original value, an effect usually referred to as "recovery". While the bias-stress effect has been thoroughly investigated, recovery has received little attention. It has been established that the dynamics of the threshold-voltage shift for recovery is different from that for stress,[7] but an explanation for this observation is still lacking. We present in this chapter a detailed study of recovery. In particular, we investigate the effect of the extent of stressing on the recovery dynamics. We find that the recovery rate strongly depends on the extent of stressing: when the transistor has been stressed to the extent that the threshold voltage has been shifted almost completely to the stressing gate bias, the time scale for recovery is much longer than when the transistor has only partially been stressed. In this chapter, we will show that recovery can be consistently explained within the framework of the model proposed for the bias-stress effect. The main ingredients of the model are:[12]

1. In the accumulation layer there is a thermodynamic equilibrium between holes and protons, where in the presence of water, holes are converted into protons and oxygen. Protons are converted into holes in the reverse reaction.

2. There is thermodynamic equilibrium between protons in the accumulation layer and protons in the SiO_2 close to the interface with the semiconductor.

3. Protons move in the SiO_2 by diffusion and drift and this motion is the rate-limiting process. The combination of 1 and 2 leads to an equilibrium between the surface density $[OS^+]$ of holes in the accumulation layer of the organic semiconductor and the volume density $[H^+]$ of protons in the SiO_2 at the interface with the semiconductor, which can be expressed as:

$$[H^+] = \alpha[OS^+], \tag{4.1}$$

   where the parameter α is determined by the reaction constants and the amount of water present at the semiconductor interface with the dielectric. The motion of protons in the SiO_2 is quantified by a diffusion constant D.

This chapter is organized as follows. In Section 4.2, we present measurements of transfer curves for a *p*-type OFET during recovery and discuss the main experimental features of the
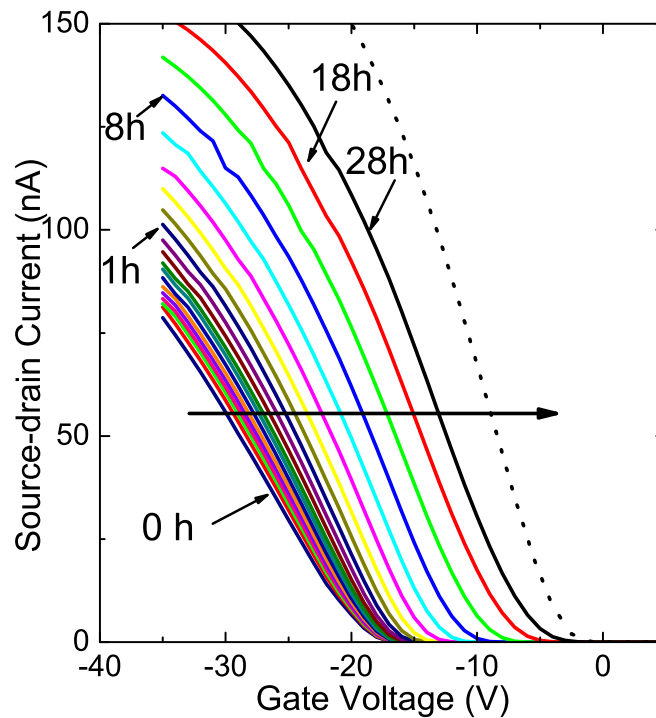
Figure 4.1: Transfer curves of a polytriarylamine (PTAA) transistor during recovery with grounded electrodes, for different recovery times indicated in hours (h). The source-drain voltage while measuring the transfer curves was $V_{SD} = -3$ V. The horizontal arrow shows the shift of the transfer curves with time. Measurements were performed in ambient atmosphere at a temperature of 30 °C. The dotted line shows the transfer curve prior to stressing.

recovery effect. In Section 4.3, we demonstrate how the proton migration mechanism can explain measurements on stress-recovery cycles with different extents of stressing. Finally, Section 4.4 contains a summary and the conclusions.

4.2 Recovery: experimental

We used the same transistor as in the previous chapter for studying recovery. First, a constant gate voltage $V_{G0} = -20$ V was applied for a certain stressing period during which the shift in the transfer curves was measured. At the end of the stressing period, zero gate bias was applied to the transistor for a total period of 28 hours. We show in Fig. 4.1 the development in time of the transfer curves during recovery of an OFET that has previously undergone stress for a stressing period of 25 hours.

The transfer curves were measured by interrupting the zero gate bias for brief periods of

time, during which a source-drain voltage of $V_{SD} = -3$ V was applied and the gate voltage was swept. As is clearly observed, the transfer curves shift back towards the original transfer curve prior to stressing.

The symbols in Fig. 4.2b labeled by A represent the threshold-voltage shift as a function of time for the transfer curves in Fig. 4.1. The shift can be fitted very well with the function $\Delta V_{th}(t) = V_1 \exp\left[-(t/\tau)^\beta\right]$, with the fit parameters $\tau = 7.7 \times 10^4$ s, $\beta = 0.58$, and $V_1 = 15.7$ V. The symbols in Fig. 4.2b labeled by B and C have been obtained by starting the recovery after 10^4 and 2×10^3 s of stressing, respectively. For these recovery curves we obtain stretched-exponential fits with $\tau = 6.5 \times 10^3$ s, $\beta = 0.3$, and $V_1 = 11.7$ V (B), and $\tau = 2 \times 10^3$ s, $\beta = 0.28$, and $V_1 = 8.4$ V. We will extensively discuss these different recovery experiments in Section 4.3.
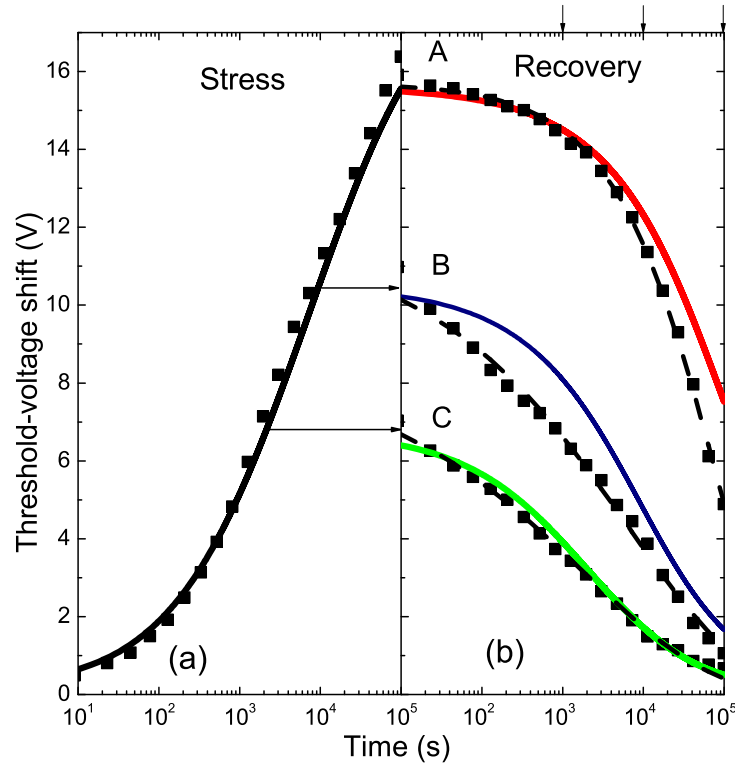
Figure 4.2: Symbols: experimentally obtained threshold-voltage shift $\Delta V_{th}(t)$ as a function of time t. (a) During stress with a gate voltage of $V_{G0} = -20$ V. (b) During recovery after three different stressing periods: 10^5 s (A, obtained from Fig. 4.1), 10^4 s (B) and 2×10^3 s (C). The dashed lines correspond to stretched-exponential fits. The thick lines correspond to the results of the proton migration mechanism. The times at which the proton density profiles are plotted in Fig. 4.4 during recovery are indicated at the upper axis in (b).

4.3   Recovery: theory

The different recovery experiments labeled by A, B and C in Fig. 4.2b discussed in Section 4.2 have been performed in order to investigate if the extent of stressing has an influence on the dynamics of the recovery. The results clearly indicate that this is the case. The fits to a stretched-exponential function yield values for the relaxation time τ of 7.7×10^4 s (A, stressing for 10^5 s), 6.5×10^3 s (B, stressing for 10^4 s), and 2×10^3 s (C, stressing for 2×10^3 s), while the relaxation time for stress is $\tau = 10^4$ s. The conclusion is that the dynamics for recovery is different from that for stress and that the relaxation times decrease with decreasing stressing time. We checked that during each stressing period the curve in Fig. 4.2a is followed, which means that the dynamics during stress remains unchanged.

The observation that the dynamics of recovery is influenced by the extent of stressing can be explained within the proton migration mechanism as follows. At the end of the stressing period, there is a density profile of protons extending into the oxide; See Fig. 3.3 of chapter 3. During recovery, when the gate bias is zero, the density of holes in the accumulation layer vanishes. Because of the equilibrium condition Eqn. (4.1) the density of protons at the interface between oxide and semiconductor also vanishes. This leads to a back-diffusion of protons from the oxide towards the semiconductor. Protons reaching the semiconductor will be converted into holes, which are carried away to the source and drain electrodes. The consequence of this is that the further away protons have diffused into the oxide during stressing, the longer it will take for these protons to diffuse back to the semiconductor. Since the depth of penetration of protons into the oxide depends on the extent of stressing (See Fig. 3.3 of chapter 3), this rationalizes the observation that the time scale for recovery decreases with decreasing stressing period.

In order to describe the recovery dynamics quantitatively, we numerically solved the time-dependent proton diffusion problem for all three stress-recovery cycles A-C. We note that we take into account only the diffusion contribution to the motion of the protons. Assuming that the device is being stressed for a total time t_{stress} before grounding the gate electrode we can write the gate voltage as a function of time in the following way:

$$V_{\text{G}}(t) = V_{\text{G0}}\theta(t) - V_{\text{G0}}\theta(t - t_{\text{stress}}). \tag{4.2}$$

In this expression, the first term can be interpreted as uninterrupted stressing of the transistor with the gate voltage V_{G0}. The contribution of this term to the proton density at the interface can be calculated by taking into account a positive source term that is injecting protons in the oxide. The second term ensures that at $t = t_{\text{stress}}$ the gate bias becomes zero, such that for $t > t_{\text{stress}}$ the hole density in the channel goes to zero. The contribution of this term to the proton density at the interface can be calculated by taking into account a negative source term corresponding to extraction of protons out of the oxide. We sketch this idea in Fig. 4.3.

We can now write for the proton density $\tilde{p}(0, t)$ at the interface as:

$$\tilde{p}(0, t) = \int_0^t \frac{1}{\sqrt{4\pi D(t - t')}} \left[s(t') - s_{\text{rec}}(t')\theta(t - t_{\text{stress}}) \right] dt', \tag{4.3}$$

where $s(t) = -(2/\alpha)dp(0, t)/dt$ and $p(0, t)$ is the density of protons at the interface for the case that the transistor is under continuous stress with the gate voltage V_{G0}. $s_{\text{rec}}(t)$ represents
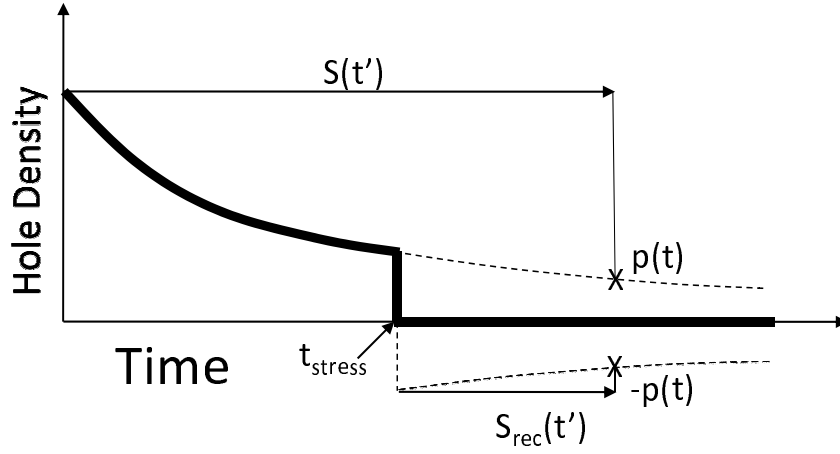
Figure 4.3: Thick black line: hole density in the accumulation layer of the transistor as a function of time. The transistor is stressed for a stressing period t_{stress}, after which the gate bias is set to zero. For $t > t_{stress}$, the hole density in the channel is zero. If the stressing would continue after t_{stress}, the hole density would follow the dotted line above the time axis. If we reflect this dotted line with respect to time axis, we get the dotted line shown below the time axis. The sum of these two dotted lines leads to a zero hole density for $t > t_{stress}$. The cross marked on the top dotted line represents the hole density when the device is continuously stressed till time t ($t > t_{stress}$). The cross marked on the dotted line below the time axis represents the negative hole density produced by the action of a sink s_{rec} acting over time $(t - t_{stress})$.

the source term that accounts for the second term in Eqn. (4.2). For $t > t_{stress}$, $\tilde{p}(0, t) \equiv 0$ and therefore we can write:

$$\int_0^t \frac{1}{\sqrt{4\pi D(t - t')}} s(t')dt' = \int_{t_{stress}}^t \frac{1}{\sqrt{4\pi D(t - t')}} s_{rec}(t')dt'. \qquad (4.4)$$

Writing $t = t_{stress} + \tilde{t}$ and using Eqn. (3.11), we can write the above equation as

$$\int_{t_{stress}}^{t_{stress} + \tilde{t}} \frac{1}{\sqrt{4\pi D(t_{stress} + \tilde{t} - t')}} s_{rec}(t')dt' = p(0, t_{stress} + \tilde{t}). \qquad (4.5)$$

Using Eqn. (4.1), we can write $p(0, t) = \alpha h_0(t)$, where $h_0(t)$ is the corresponding hole density in the channel for the case that the transistor is under constant stress with the gate voltage V_{G0}. Writing $s_{rec}(t) = 2r(t)/\sqrt{t}$ in the equation above, we can derive the following equation for $r(t)$:

$$r(t) = \frac{2}{\pi} h_0(t_{stress} + t) - \frac{1}{\pi} h_0(t_{stress}) + \frac{2}{\pi} \int_0^t \sin^{-1}\left(\frac{2t'}{t} - 1\right) \frac{dr(t')}{dt'} dt'. \qquad (4.6)$$
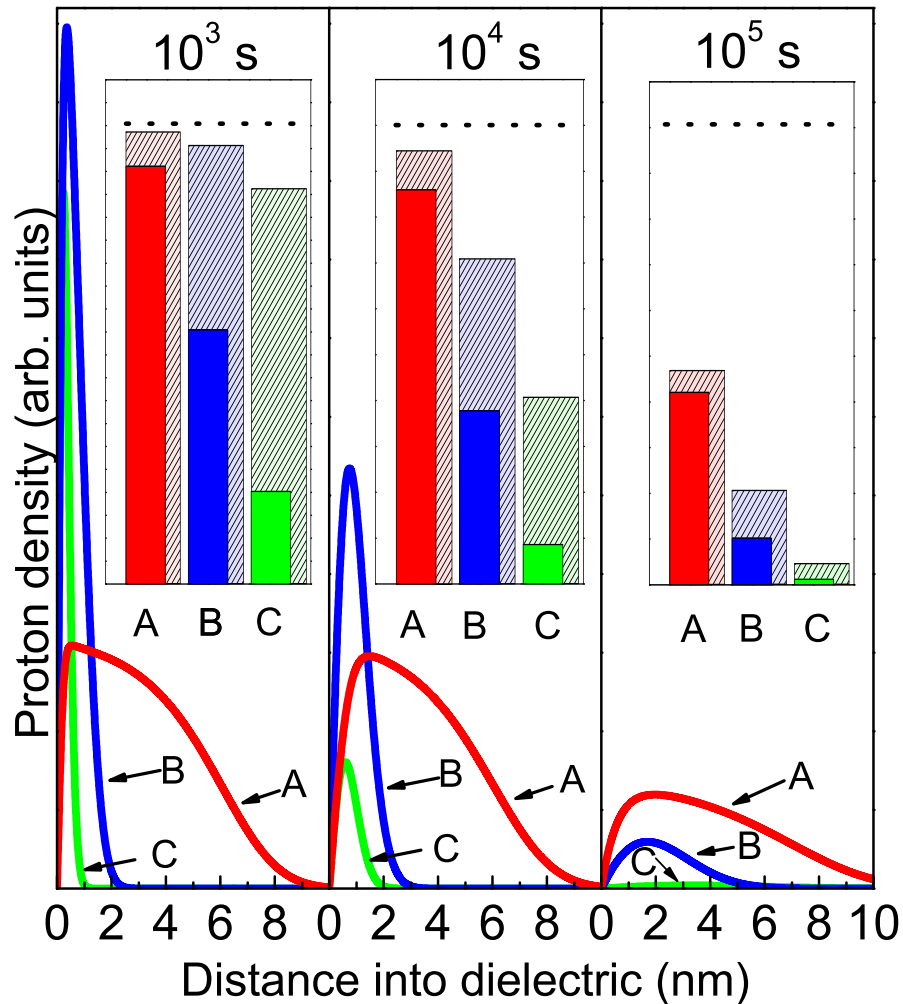
Figure 4.4: Modeled proton density profiles in the oxide during recovery after recovery times of 10^3, 10^4, and 10^5 s (left to right). A, B, and C refer to the same stressing periods as in Fig. 4.2b. Inset: bar diagrams representing the total charge (filled bars) in the oxide calculated from the model and the total charge normalized to that at the start of recovery (hatched bars). The dotted line represents the initial normalized charge at the start of recovery.

This equation can be solved for $r(t)$ using iterative numerical techniques. The threshold voltage during recovery can then be calculated as

$$V_{\text{th}}(t) = \frac{e}{C} \left(c_0 - h_0(t_{\text{stress}} + t) - \int_0^t \frac{r(t')}{\sqrt{t - t'}} dt' \right). \qquad (4.7)$$

The results for the recovery curves A-C are given by the thick lines in Fig. 4.2b, using exactly the same value $t_0 = 4.2 \times 10^3$ s as found in the previous chapter. The agreement with the measured data is surprisingly good. Apparently, the proton migration mechanism captures the dynamics of the threshold voltage for stress as well as recovery.

In Fig. 4.4 we show the proton density profiles in the oxide with proceeding recovery, calculated with the parameters $D = 1.6 \times 10^{-19}$ cm^{2}s^{-1} and $\alpha = 2.2$ nm^{-1} found in Section 3.4, for three different times after the start of recovery, indicated at the upper axis in Fig. 4.2b: 10^3, 10^4, and 10^5 s. The profiles labeled by A, B, and C correspond to the same stressing periods as in Fig. 4.2b. We clearly see that with a shorter stressing period the protons are removed much quicker from the oxide during recovery than with a longer stressing period. To emphasize this point further, we indicate the total proton charge contained in the oxide by filled bars in the insets of Fig. 4.4. The hatched bars indicate the total proton charge normalized to the total amount of charge just before recovery, making clear that the *relative* recovery rate is faster in the case of a shorter stressing period. If the recovery dynamics would not depend on the stressing period, the normalized total proton charge would be the same for the situations A-C.

4.4 Summary and conclusions

We developed a model for operational instabilities involving threshold-voltage shifts in *p*-type organic field-effect transistors with silicon-dioxide as gate dielectric based on a proton migration mechanism. The model is based on the assumption that an equilibrium exists in the accumulation layer of the organic semiconductor between holes and protons, because of reactions taking place involving these species and water, and on the assumption that protons can reversibly move in and out of the gate dielectric.

The recovery of a transistor that has been exposed to bias stress can also be described with the model. In recovery, protons that have migrated into the oxide during stressing diffuse back to the semiconductor, where they are converted back into holes that are carried away by the source and drain electrodes. This leads to a shift of the threshold voltage back to its original value. The model predicts that the extent of stressing has a large influence on the dynamics of the recovery. A transistor that has been almost fully stressed recovers relatively much slower than a transistor that has been only partially stressed. Therefore, the recovery curves for the threshold-voltage shift cannot be described by a single stretched-exponential function. The measured time dependence of the threshold voltage during recovery quite accurately follows the model predictions, obtained using parameters from the modeling of the threshold-voltage shift for stress. These results have an important technological implication for the operation of organic transistors: an optimal operational time can be obtained by alternating short periods of operation with short periods of recovery.

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Chapter 5

Anomalous current transients in organic field-effect transistors

The proton migration mechanism for the bias-stress effect in organic p-type transistors is based on water-mediated exchange between holes in the semiconductor and protons in the gate dielectric. We show that the model predicts that anomalous current transients should occur for a non-constant gate bias: applying a strongly negative gate bias followed by a less negative bias, while ensuring accumulation, should lead to a back-transfer of protons to holes and an increase of the current. We verify this counterintuitive behavior experimentally and can quantitatively model the transients with the same parameters as the bias-stress effect.*

5.1   Introduction

In the previous chapters, we studied the bias-stress effect and recovery in organic field-effect transistors (OFETs). We proposed a mechanism for the bias-stress effect based on the production of protons in the accumulation layer of the transistor from holes and water and the subsequent migration of these protons into the gate dielectric.[1] We also showed that during recovery of a stressed OFET, protons accumulated in the gate dielectric during stressing migrate back to the semiconductor. The main ingredients of the model are:[1]

1. In the accumulation layer there is a thermodynamic equilibrium between holes and protons, where in the presence of water, holes are converted into protons and oxygen. Protons are converted into holes in the reverse reaction.

2. There is thermodynamic equilibrium between protons in the accumulation layer and protons in the SiO_2 close to the interface with the semiconductor.

3. Protons move in the SiO_2 by diffusion and drift and this motion is the rate-limiting process. The combination of 1 and 2 leads to an equilibrium between the surface density $[OS^+]$ of holes in the accumulation layer of the organic semiconductor and the volume density $[H^+]$ of protons in the SiO_2 at the interface with the semiconductor, which can be expressed as:

$$[H^+] = \alpha[OS^+], \tag{5.1}$$

    where the parameter α is determined by the reaction constants and the amount of water present at the semiconductor interface with the dielectric. The motion of protons in the SiO_2 is quantified by a diffusion constant D.

Most of the studies on the bias-stress effect and recovery have focussed on the shift in the threshold voltage under a constant applied gate bias.[1–14] In practical applications, however, transistors are not biased statically but dynamically, i.e., the applied biases are a function of time. The unique aspect of the proton migration mechanism, in comparison to other proposed mechanisms for the bias-stress effect,[2,4,5,12] is that it is not based on trapping of charges in or very near the accumulation layer, but on a build-up of charges, the protons, in the bulk of the oxide at a distance of the accumulation layer. This means that the state of the transistor is not only determined by the total number or protons in the oxide, but also by their particular density profile. In Chapter 3, we have seen that in an ordinary bias-stress experiment with a constant stressing gate voltage the shift of the threshold voltage is monotonic and that the proton density profile decays monotonically into the bulk of the oxide. With the application of a dynamic gate bias, however, it is possible to create a non-monotonic proton density profile, leading to a non-monotonic time dependence of the threshold voltage. The observation of such anomalous non-monotonic behavior is an excellent way to validate the proton migration mechanism.

The chapter is organized as follows. In Section 5.2, we show how the proposed mechanism predicts anomalous current transients in an OFET under a dynamic gate bias. In Section 5.3, we quantitatively describe the anomalous behavior in the light of the proton migration model. Finally, Section 5.4 contains a summary and the conclusions.
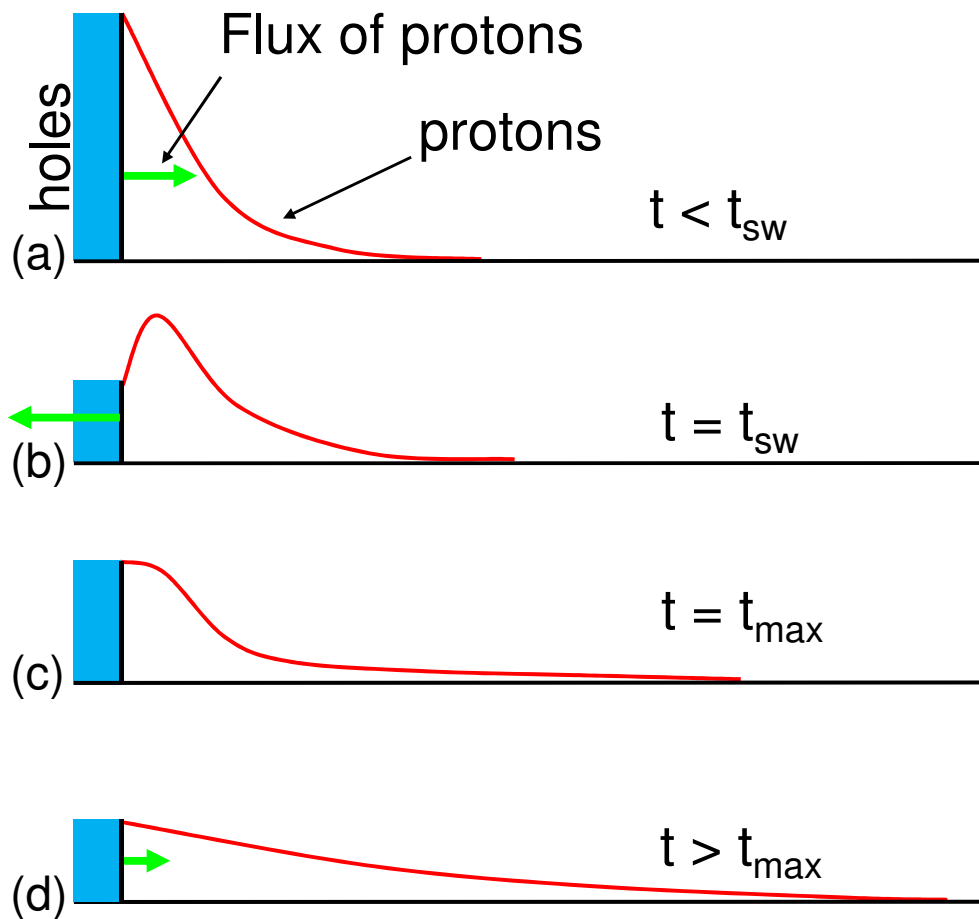
Figure 5.1: Sketch of the mechanism behind the anomalous current transients. Blue bars: hole density in the accumulation layer. Red lines: proton density in the dielectric, scaled such that the lines connect continuously to the blue bars at the interface. Green arrows: proton flux from the semiconductor into the dielectric, or vice versa. (a) Applying a strongly negative gate bias V_{G0} creates a decaying proton concentration profile. There is a proton flux into the dielectric and the source-drain current decreases with time. (b) Immediately after switching to a less negative gate voltage V_{G1} at time t_{sw} the proton concentration at the interface decreases. Excess protons in the bulk of the dielectric diffuse back towards the semiconductor and convert back into holes, leading to an increasing current. (c) At a certain time t_{max}, the flux of protons is zero and the current reaches a maximum. (d) The proton flux is again directed into the dielectric. The source-drain current continues to decrease with time.

5.2   Anomalous transients: qualitative

We investigate a dynamic gate biasing scheme in which the transistor is first stressed with a strongly negative gate voltage V_{G0} and then, after time $t = t_{sw}$, stressed with a less negative gate voltage V_{G1}, which is chosen such that the transistor remains in accumulation throughout the stressing period. During the stressing, a constant small source-drain voltage V_{SD} is applied, leading to a source-drain current I_{SD} that is measured.

According to the proton migration mechanism the following should happen, as pictorially sketched in Fig. 5.1. After applying the initial gate voltage V_{G0}, protons are generated in the accumulation layer in an equilibrium with holes. With time, these protons diffuse into the oxide, causing a build-up of a distribution of protons in the oxide at the cost of the hole density in the accumulation layer; see Fig. 5.1a. Hence, the source-drain current should decrease. This decrease is as expected for the usual bias-stress effect. At time $t = t_{sw}$, the gate voltage is switched to the less negative voltage V_{G1}, causing the hole density in the accumulation layer to decrease. The proton density at the oxide interface should correspondingly decrease, because of the fast equilibration between protons in the oxide at the interface and holes in the accumulation layer (Eqn. (5.1)). Due to the excess protons in the bulk of the oxide, the distribution of protons will acquire the shape indicated in Fig. 5.1b. As a result, there will be a diffusive flow of protons towards the accumulation layer, where they are converted back into holes. This should lead to an increase of the hole density in the accumulation layer and an increase of the source-drain current. It is important to note at this point that with the gate bias V_{G1} the transistor is still in accumulation and therefore under stressing conditions, so that other mechanisms for the bias-stress effect would predict a continuing decrease of the current. The proton migration mechanism predicts that the source-drain current will increase until a maximum is reached; see Fig. 5.1c. After that, the flow of protons should reverse sign again: protons diffuse into the oxide and the source-drain current should continue to decrease; see Fig. 5.1d.

We checked the above prediction by applying such a gate biasing scheme to the same transistor as studied in the previous chapters and operated under the same conditions. The biasing scheme is shown in the upper panel of Fig. 5.2: a pre-stressing gate voltage $V_{G0} = -20$ V is followed by a step to a voltage $V_{G1} = -10$ V after a pre-stressing time $t_{sw} = 900$ s. The lower panel of Fig. 5.2 shows the resulting source-drain current, which exactly shows the predicted behavior. The indicated points a-d correspond in the same order to Figs. 5.1(a)-(d). Importantly, we made sure that the transistor remains well into accumulation mode during the whole experiment. We remark that the occurrence of a non-monotonic current transient is not predicted by other models for the bias-stress effect that we know of.[1] Other models would rather predict a current transient indicated by the dashed line in Fig. 5.2. The non-monotonic nature of the transient shows that the OFET has a "memory" of its biasing history. This is clearly demonstrated by the fact that at the points b and d in Fig. 5.2 the source-drain current is the same, whereas the future development of the current is not. This memory effect is caused by the "storage" of protons in the gate dielectric, which is a unique feature of the present model.

In principle one can construct a specific model based on competition between trapping and detrapping of mobile carriers in the accumulation layer that will give rise to similar transients on switching the gate bias. On applying such model to the bias-stress effect under constant gate

bias, it would predict a steady-state situation in which there is a balance between trapping and detrapping. However, such model would predict a saturation of the threshold voltage, which is in contrast to the observation that the threshold voltage shifts all the way to the applied gate voltage under constant stress.

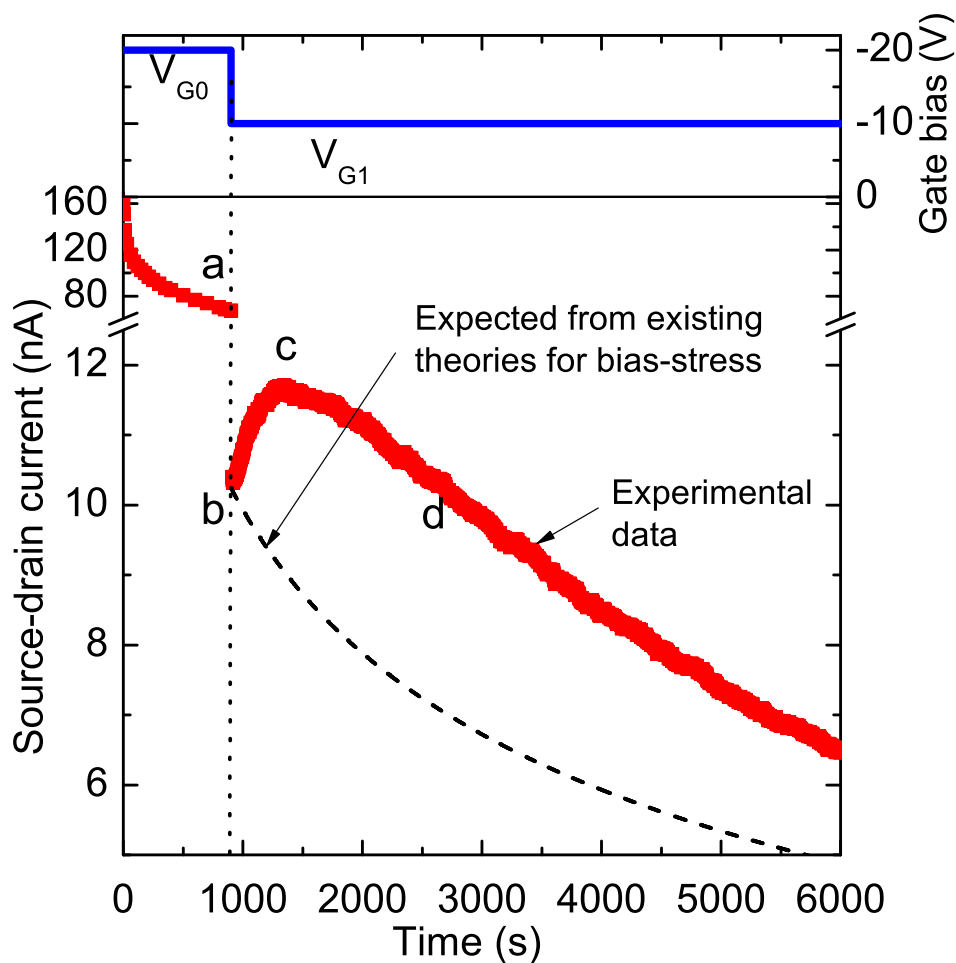**Figure 5.2:** Upper panel: dynamic switching scheme of the gate bias voltage. Lower panel: source-drain current I_{SD} vs. time t for a source-drain voltage $V_{SD} = -3$ V. The dotted line indicates the switching time $t_{sw} = 900$ s. The dashed line indicates the transient as predicted by existing models for the bias-stress effect. The points indicated by a-d correspond to (a)-(d) in Fig. 5.1.

5.3   Anomalous transients: quantitative

The scenario explaining the anomalous transient currents can be made quantitative in the following way. The dynamic gate voltage applied to the gate electrode can be written as the sum of two step functions:

$$V_{\mathrm{G}}(t) = V_{\mathrm{G0}}\theta(t) - (V_{\mathrm{G0}} - V_{\mathrm{G1}})\theta(t - t_{\mathrm{sw}}), \tag{5.2}$$

where $\theta(t)$ is the unit step function. The experiments on the anomalous current transients are conducted on a time scale where the motion of protons in the oxide is primarily dominated by their diffusion. The following analysis is analogous to the one presented in Section 4.3 of Chapter 4.

By virtue of the linearity of the diffusion equation, the solution for the surface density of holes $h(t)$ can be obtained as the linear combination

$$h(t) = h_0(t) - \left(1 - \frac{V_{\mathrm{G1}}}{V_{\mathrm{G0}}}\right) h_0(t - t_{\mathrm{sw}}), \quad (t > t_{\mathrm{sw}}), \tag{5.3}$$

where $h_0(t)$ is the solution for the bias-stress effect given by the equation derived in Chapter 3:

$$h_0(t) = \frac{1}{2} \int_0^t \frac{t_0^{1/2}}{(t - t')^{3/2}}(h_0(t') - h_0(t))dt' - \left(\frac{t_0}{t}\right)^{1/2}(h_0(t) - c_0), \tag{5.4}$$

where the characteristic time t_0 is given by

$$t_0 \equiv \frac{1}{\pi\alpha^2 D}. \tag{5.5}$$

with $c_0 \equiv CV_{\mathrm{G0}}/e$, where C is the capacitance of the oxide per unit area, and e is the elementary charge. The threshold voltage is obtained as

$$V_{\mathrm{th}}(t) = \frac{e}{C}(c - h(t)), \quad (t > t_{\mathrm{sw}}), \tag{5.6}$$

with $c \equiv CV_{\mathrm{G1}}/e$.

We show in Fig. 5.3 the measured and predicted current transients for different values of the pre-stressing time t_{sw} and the gate voltage V_{G1} after the pre-stressing time. In the calculations we have used $t_0 = 4.2 \times 10^3$ s, which is obtained from the fit of the theoretical to the measured time-dependence of the threshold-voltage shift in Chapter 3. Once we have obtained the threshold voltage as a function of time after switching of the gate voltage, we obtain the predicted current transients using the transfer curves from Section 3.2. We note that in this procedure the lateral inhomogeneity of the hole density in the accumulation layer due to the finite source-drain voltage $V_{\mathrm{SD}} = -3$ V is neglected.

In Fig. 5.3(a) a gate bias $V_{\mathrm{G0}} = -20$ V is applied for a fixed pre-stressing time $t_{\mathrm{sw}} = 900$ s, after which the gate bias is stepped to three different values of V_{G1}, while in Fig. 5.3(b) the initial gate bias $V_{\mathrm{G0}} = -20$ V and the final gate bias $V_{\mathrm{G1}} = -10$ V are kept fixed and
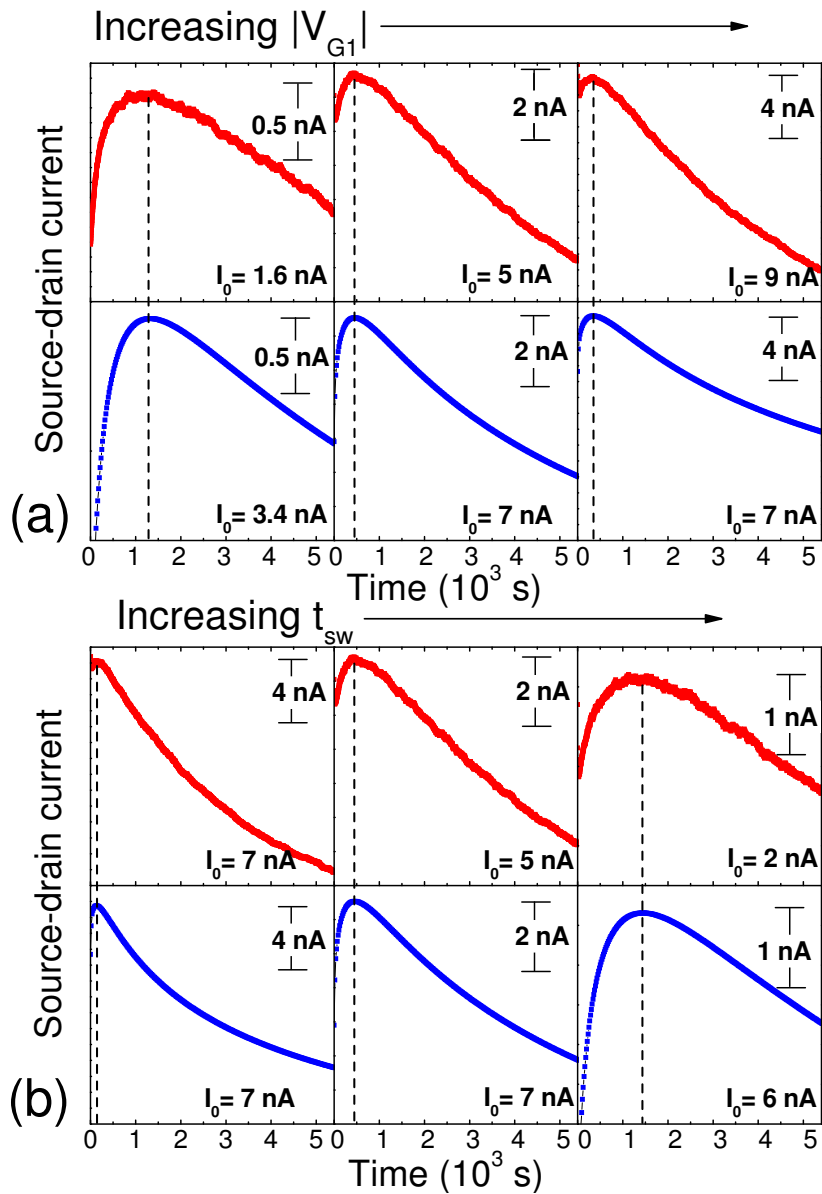
Figure 5.3: Upper (red) curves: measured source-drain current I_{SD} for $V_{SD} = -3$ as a function of time $t - t_{sw}$ after switching. The initial gate bias is $V_{G0} = -20$ V. Lower (blue) curves: model predictions using $t_0 = 4.2 \times 10^3$ s. Vertical dashed lines: time t_{max} for which the model predicts maximal current. Bars: current scale. The transients are displayed with an offset current I_0 that is indicated in the figures. (a) Constant switching time $t_{sw} = 900$ s and varying gate bias V_{G1} after switching: -7, -10, and -12 V (left to right). (b) Constant $V_{G1} = -10$ V and varying t_1: 300, 900, and 1800 s. The experimental curves in the middle panels of (a) and (b) are the same as in Fig. 5.2 for $t > t_{sw}$.

three different values of the pre-stressing time t_{sw} are taken. The agreement between the experimental and predicted transients is striking. We show the experimental and theoretical transients with different offset currents I_0, which roughly compensates for the above mentioned neglect of inhomogeneity. We checked that the times t_{max} at which the peaks appear are highly insensitive to the particular value of V_{SD}. The agreement between the experimental values of t_{max} and the theoretical predictions is excellent.

5.4   Summary and conclusions

Summarizing, we predicted the occurrence of anomalous non-monotonic current transients in p-type organic field-effect transistors with a silicon-oxide gate dielectric for a time-varying gate bias, where after pre-stressing with a strongly negative gate bias the bias is stepped to a less negative voltage. During pre-stressing, protons produced in the semiconductor from holes and water diffuse into the gate dielectric. After the step in the bias, these protons diffuse back to the semiconductor, where they are reconverted into holes. This leads to a temporal increase in the number of holes and the transistor current. The occurrence of the resulting non-monotonic current transients was verified experimentally. The measured current transients accurately follow the model predictions, obtained using parameters from the modeling of the bias-stress effect. We consider the quantitative prediction and the experimental verification of these quite unexpected results as an important step forward in the understanding of the operational instabilities occurring in organic transistors.

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Chapter 6

Locating trapped charges in a self-assembled organic monolayer field-effect transistor

We study the time evolution of the transfer curve of a self-assembled organic monolayer field-effect transistor to which a prolonged gate bias is applied. The gradual shift of this curve towards the applied bias points at an ongoing trapping of mobile charges. We show that the subtle change in the shape of the transfer curve can be used to identify the location of the trapped charges. Simulations of the charge transport in the Coulomb field of the trapped charges cannot reproduce this subtle change if the trapped charges are located in or close to the monolayer. Agreement is only found for a finite penetration depth of the trapped charges into the dielectric. The conclusion that charge trapping takes place in the bulk of the dielectric is in line with the proton migration mechanism for the bias-stress effect in organic field-effect transistors.**

6.1   Introduction

Studies of the bias-stress effect in organic field-effect transistors have indicated that the effect is due to a gradual trapping of mobile charges.[1–9] If the location of the trapped charges could be determined, this could be used to distinguish between the different proposed mechanisms for the bias-stress effect. The proton migration mechanism investigated in this thesis is the only proposed mechanism that predicts that the trapped charges are located in the gate dielectric. The Coulomb scattering by the trapped charges is expected to have a major effect on the mobility of the mobile charges in the transistor channel. The effect should be reflected in the electrical characteristics of the OFET. The precise location of the trapped charges plays a crucial role in the following way. If the trapped charges are located in the transistor channel a large influence on the mobility is expected, whereas if the trapped charges are located at a distance from the channel the Coulomb scattering should be much reduced. Recently, an experimental study was performed which strongly indicated that traps are not located in the channel.[10] In the experimental study, a series of PTAA (polytriarylamine) transistors was stressed for specific periods. At the end of the stressing, transfer curves were measured and the semiconductor was peeled off. Subsequently the surface potential of the exposed gate dielectric was probed with SKPM with all electrodes grounded. It was observed that after stressing, the surface potential profile obtained with or without the organic semiconductor was exactly the same. This unambiguously demonstrated that the charges are not trapped in the organic semiconductor but in the gate dielectric. In another experiment, a transistor with a self-standing semiconducting film as active layer was fabricated. The transistor was stressed for a specific time. After stressing, transfer curve was measured and the semiconductor was removed immediately after and a pristinie new film of organic semiconductor was then applied on the same source-drain electrodes. The transfer curve measured on this device with the new pristine film was nearly identical to the original stressed transfer curve.[10] Although these experiments clearly showed that traps are not located in the channel, they did not precisely determine the location of the traps as to whether they are at the surface of the dielectric or in the bulk of the dielectric. Determining the location of the traps is an important step in unraveling the mechanism behind the bias-stress effect. As far as we know, the Coulomb scattering effect of trapped charges on the mobility in OFETs has not been investigated theoretically.

An interesting analogy can be drawn with the Coulomb scattering of mobile electrons by ionized donors in inorganic semiconductors. With homogeneous doping of the semiconductor the electron mobility significantly decreases with increasing donor concentration, because the electrons and donors are located in the same region of space.[11] However, in III-V semiconductor heterostructures a situation can be created where the electrons are located in a quasi two-dimensional region that is spatially separated from the ionized donors. This spatial separation of electrons and donors is called "modulation doping". It leads to a much reduced Coulomb scattering and an improved mobility of the two-dimensional electron gas.[11] In the present chapter we will show that in OFETs an effect occurs that is based on exactly the same physics.

A problem that hinders the analysis of the effect of trapped charges on the electrical characteristics of OFETs is the complex morphology of the organic semiconductors that are commonly used. These semiconductors often consist of well-ordered regions separated by less ordered
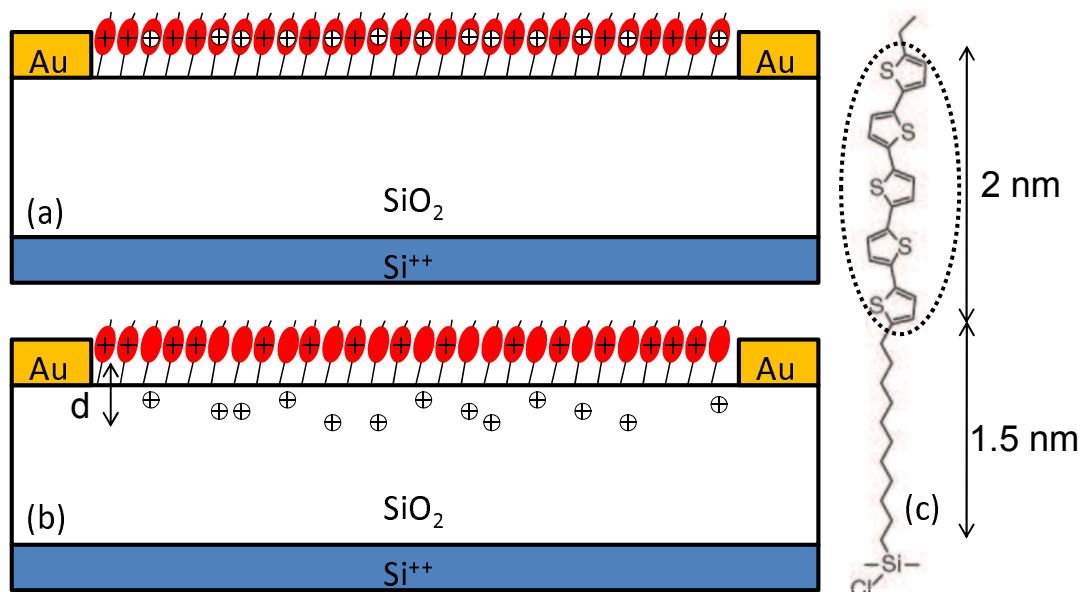
Figure 6.1: (a) and (b) Schematic of the SAMFET. In (a) the trapped charges (circles) are lying in the monolayer. In (b) they are distributed in the gate dielectric to a depth d. (c) Chemical structure of the self-assembling molecule.

regions. Charge trapping in the less ordered regions may be enhanced with respect to the well-ordered regions.[8,12] Another problem is the large thickness (typically of the order of 100 nm) of the commonly used organic layers, as compared to the thickness of the accumulation layer of the transistor (typically of the order of 1 nm). This leads to a large volume of the organic layer that does not take part in charge transport, but that could contain many traps.[13]

In order to avoid these problems we investigate in this chapter the effects of trapped charges on the electrical characteristics of a field-effect transistor consisting of a quinquethiophene-based self-assembled organic monolayer (SAMFET); see Fig. 6.1. The self-assembled monolayer (SAM) in this system is very homogeneous and has a high degree of order. Furthermore, contrary to conventional OFETs, the entire volume of the organic layer participates in charge transport, so that there are no inactive regions where charge trapping can take place. Another important advantage of this system is that the charge transport is truly two-dimensional. This facilitates the modeling of the charge transport in this system enormously. In particular, it allows the evaluation of the effects of the static Coulomb field of trapped charges on the transport of the mobile charges.

The chapter is organized as follows. In Section 6.2, we present measurements of transfer curves for a p-type SAMFET during stressing and discuss the main experimental features of the effect, in particular the change in mobility during the stressing period. In Section 6.3, we describe the two-dimensional model of the SAMFET and the Monte-Carlo approach for determining the current in the channel. This Monte-Carlo approach includes the Coulomb

interaction between the charges. Finally, Section 6.4 contains a summary and the conclusions.

6.2 Effect of Coulomb interaction on the mobility: experiment

The SAMFET was prepared on a heavily doped silicon wafer (acting as the gate) covered with a 200 nm layer of thermally grown SiO_2.[14] The gold source and drain contacts were defined by conventional photolithography and wet etchant chemistry. Titanium (10 nm) was used as an adhesion layer. The liquid-crystalline active molecule comprised a mesogenic quinquethiophene core, end-capped with an ethyl group to enhance stability and solubility. To bind the molecule to the SiO_2 gate dielectric, a monochlorosilane anchoring group was attached via an undecane spacer. The chemical structure of the self-assembling molecule, chloro [11-(5''''-ethyl-2,2':5',2'':5'',2 ''':5''',2''''-quinquethien-5-yl)undecyl]-dimethylsilane is shown in Fig. 6.1c. To induce self-assembly of the molecules, the SiO_2 gate dielectric was activated by an oxygen plasma treatment followed by acid hydrolysis. The SAM was then formed by submerging the substrate in a dry toluene solution of the semiconducting molecule for two days, resulting in a smooth dense layer. The length and width of the SAMFET channel are $L = 10$ μm and $W = 2500$ μm, respectively. The electrical characterizations were carried out at a temperature $T = 30°$ C in vacuum of 10^{-6} mbar. Fig. 6.2a shows the time evolution during 15 days of the transfer curve of the SAMFET while a voltage of $V_{G0} = -30$ V was applied to the gate. The transfer curves were measured by brief interruptions with a gate sweep, while applying a source-drain voltage of $V_{SD} = -2$ V. Fig. 6.2b shows the time evolution during an ensuing period of 15 days in which the gate was grounded.

Several important conclusions can be drawn from Fig. 6.2:

1. During the bias stress the transfer curve shifts towards the applied gate voltage. This shift is generally understood as a result of trapping of mobile charges.[2,7,8,10,12] When an increasing number of the charges induced by the gate field is being trapped, the transistor switches on at a larger magnitude of the gate voltage.

2. During the bias stress there is a subtle change in the shape of the transfer curve. In particular, the slope of the linear part of the transfer curve shows a slight but significant decrease. Such behavior is also observed in more typical OFETs[15–17] and very likely has the same origin.

3. Although after the recovery period (which is equally long as the stressing period) the transfer curve has not completely returned to the initial transfer curve, the shape of the transfer curve at the end of the experiment is exactly the same as that of the initial transfer curve. This shows that the change in shape of the transfer curve during stressing is a reversible effect that should be attributed to the presence of the trapped charges.

Our explanation for the change in the shape of the transfer curve during stressing is the effect of Coulomb interactions between the trapped and mobile charges on the charge transport
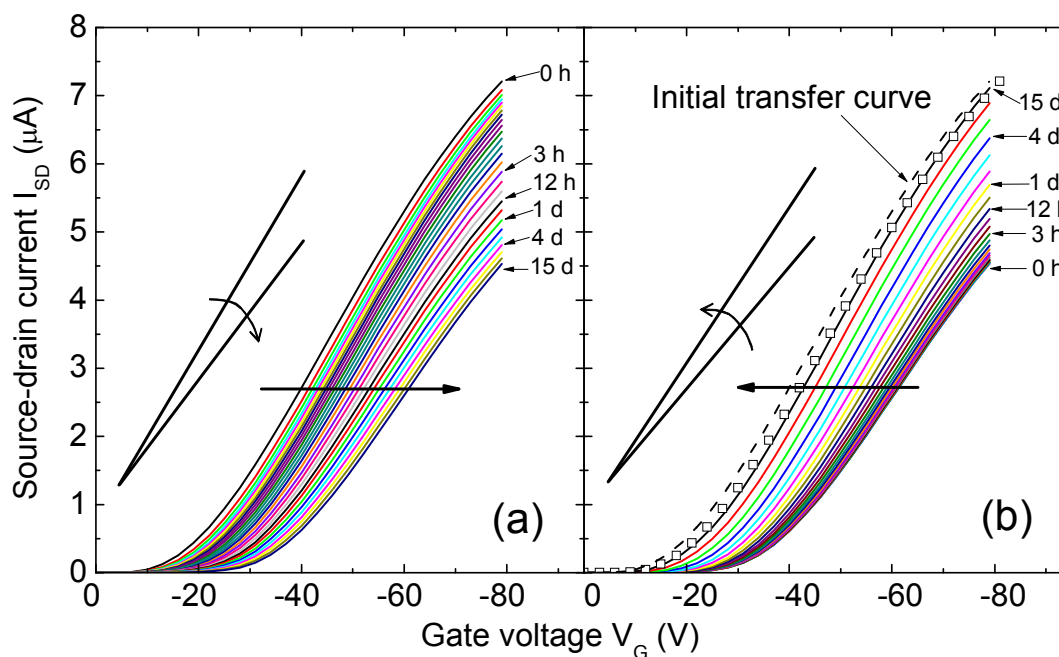
Figure 6.2: (a) Transfer curves of the investigated SAMFET during stressing for 15 days in vacuum at temperature $T = 30°$ C. The gate bias voltage during stressing was $V_{G0} = -30$ V and the source-drain bias during measurement of a transfer curve was $V_{SD} = -2$ V. (b) Transfer curves during recovery. The gate bias voltage during recovery was $V_{G0} = 0$ V. Dashed line: original transfer curve before stressing. Squares: original transfer curve shifted by -2 V. The horizontal arrows in (a) and (b) indicate the direction of the shift. The tilted lines indicate the slope of the linear part of the initial and final transfer curve and the curved arrows indicate the change in slope.

in the SAMFET. In the next section we will make a quantitative analysis of this effect. We will show that that the effect can be used to obtain information about the location of the trapped charges.

6.3   Effect of Coulomb interaction on mobility: theory

The monolayer self-assembles in a herringbone pattern with lattice constants of 5.49 and 7.69 Å and with a slight tilt angle of the molecules of $20°$ with respect to the normal.[14] Because the orientation of the herringbone pattern with respect to the source and drain electrodes is unknown and because the wavefunction of a charge located at a molecule is known to spread also to the neighboring molecules, we model the monolayer for simplicity as a square lattice of sites with lattice constant a. The relatively low mobility and the thermally activated behavior of the SAMFET[14] indicate that charge transport occurs by phonon-assisted hopping of charges between molecules. For the case of coupling to acoustical phonons this process is appropriately

described by the Miller-Abrahams hopping rate[18]

$$
\begin{aligned}
W_{ij} &= \nu_0 exp\left[-2\alpha R_{ij} - \beta(E_j - E_i)\right], E_j \geq E_i, \\
&= \nu_0 exp[-2\alpha R_{ij}], \qquad\qquad E_j < E_i.
\end{aligned}
\tag{6.1}
$$

Here, $\beta = 1/k_B T$, with k_B Boltzmann's constant, ν_0 is a phonon frequency, $|\mathbf{R}_i - \mathbf{R}_j|$ is the distance between sites i and j, and E_i and E_j are the on-site energies of sites i and j. For the inverse localization length of the wave functions α we have taken $10/a$.[19] The value taken for the inverse localization length of the wave functions α only influences the prefactor of the hopping rate, as long as it is large enough to suppress further than nearest-neighbor hopping. For the value $\alpha = 10/a$ that we have taken, this is the case.[19]

The energy difference in Eqn. (6.1) contains a contribution $-eFR_{ijx}$ due to an electric field F, taken in the x direction of the lattice (e is the unit charge), and a contribution due to the Coulomb interactions with all other, mobile and immobile, charges. Since charge transport occurs in a two-dimensional surface on top of a dielectric, the Coulomb interaction has to be adapted to this geometry. The Coulomb interaction energy between two unit charges of which one is at the interface between vacuum and a dielectric with relative dielectric constant ϵ_r (3.9 for SiO_2) while the other is at an arbitrary position at a distance R, is[20]

$$
V_{ij} = \frac{2e^2}{4\pi\epsilon_0(\epsilon_r + 1)R},
\tag{6.2}
$$

with ϵ_0 the vacuum permittivity. This result is formally derived in Appendix B. Finally, the on-site energies E_i contain a random contribution $E_{rand,i}$ that we will draw from a Gaussian density of states (DOS):

$$
g(E) = \frac{1}{\sqrt{2\pi}\sigma a^2} \exp\left[-\frac{E^2}{2\sigma^2}\right],
\tag{6.3}
$$

with σ the standard deviation of the DOS. We note that the combination of Miller-Abrahams hopping and Gaussian disorder has been very successful in describing charge transport in various organic semiconductors.[19,21]

We performed Monte-Carlo simulations for the charge transport in two-dimensional square lattices of 100×100 sites in the following way. We start with an empty lattice and fill it with a prescribed number of holes determined by the applied gate bias and the transistor capacitance. For a gate voltage V_G the surface density of charges is given by $n = C|V_G|/(eWL)$, where $C = 4.35$ pF is the transistor capacitance. This corresponds to an increase of the filling of the lattice of about 1% for every -10 V in V_G. After that, hops of holes are chosen with weights determined by the hopping rates Eqn. (6.1). A hopping time is chosen from an exponential distribution with an inverse decay time equal to the sum of all possible hopping rates. An applied electric field of $F = 0.1\sigma/ea$ was taken in the simulations, which is well within the linear regime of the charge transport. After about 10 million simulation steps, a stationary situation was obtained and the current was determined. An average over the currents for 10 disorder configurations of the on-site energies was taken until the error in the average current was smaller than 5%. At the beginning of the experiment ($t = 0$) all charges are assumed

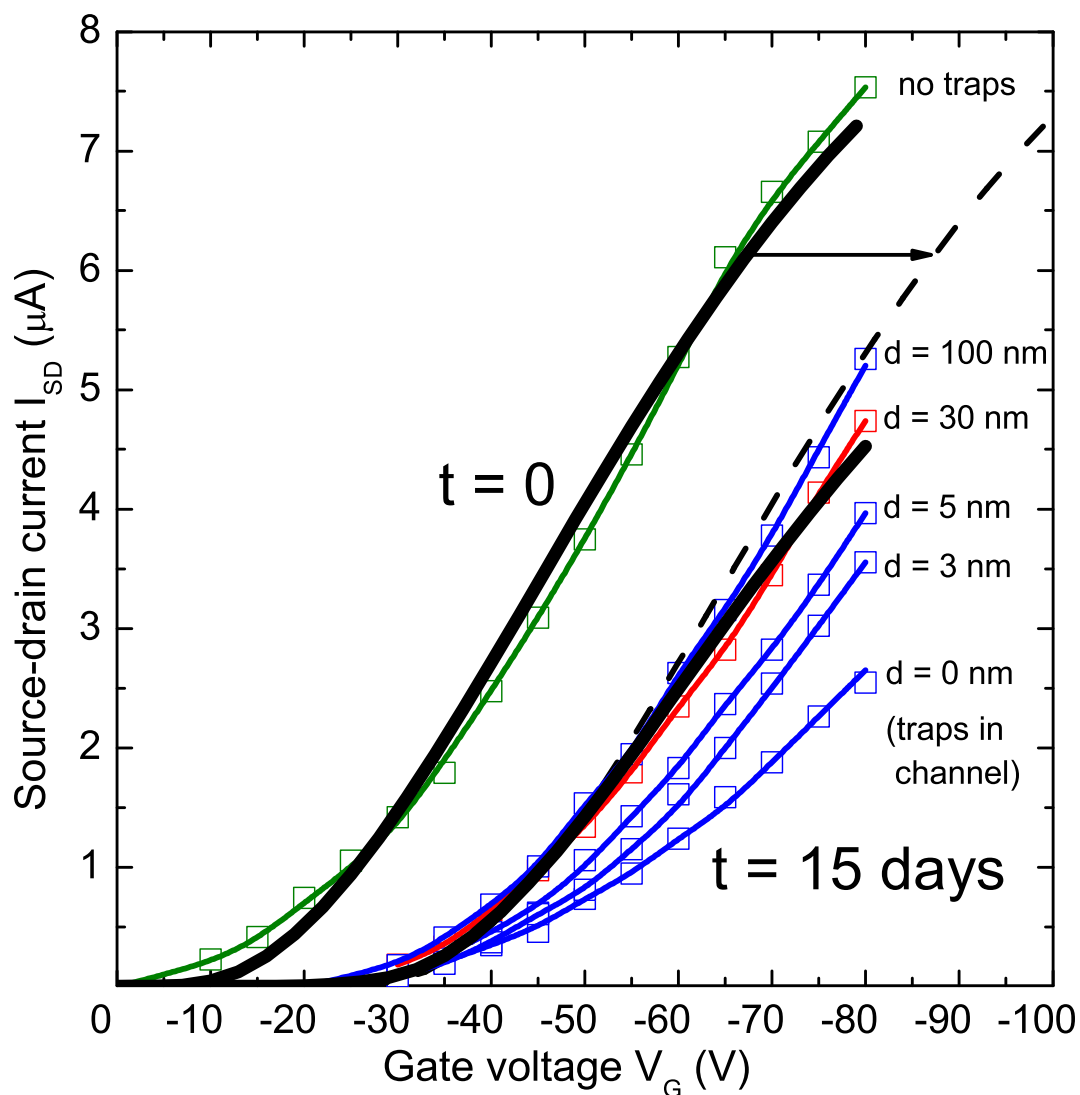**Figure 6.3:** Thick solid lines: measured transfer curves from Fig. 6.2a at the start of the experiment and after 15 days of applying a gate voltage of $V_G = -30$ V. Dashed line: initial transfer curve shifted by -20 V. Thin lines and symbols: simulated transfer curves without trapped charges and for a uniform trapped charge distribution with a surface density of 2×10^{12} cm^{-2} in a layer of thickness d.

to be mobile. We obtain a very good fit to the experimental transfer curve at $t = 0$ with a standard deviation of the Gaussian DOS of $\sigma = 0.13$ eV and a lattice constant of $a = 1$ nm; see Fig. 6.3. The value for σ is quite typical for organic semiconductors. The fact that a is larger than the shortest packing distance of 0.47 nm between the molecules[14] could account for a certain amount of correlation between the random energies of neighboring molecules. A free numerical prefactor in the simulated current was used in the fitting of the initial transfer curve and kept constant for all following calculations.

We note that the experimental transfer curve at $t = 0$ appears to have a non-zero threshold voltage. However, since the transfer curve can be reproduced by our simulations without assuming trapped charges at $t = 0$, we conclude that the apparent non-zero threshold voltage is not related to any initial trapped charges being present in the SAMFET. Also, for the channel length considered here (10 μm) contact effects are negligible.[14] Instead, the apparent initial threshold voltage offset is related to the filling of energetically low-lying states in the tail of the DOS. The difference between the simulated and experimental transfer curve at low gate voltage could be due to deviations from a Gaussian in the tail of the DOS.

Using exactly the same parameters, simulations were performed for the case that a fixed amount of charges induced by the gate field is trapped. After 15 days of application of the gate voltage of $V_G = -30$ V, the shift of the transfer curve of about $V_{shift} = -20$ V corresponds to a trapped charge density of about 2×10^{12} cm^{-2}. For the case that these trapped charges are randomly distributed in the transistor channel, i.e., in the monolayer, the predicted transfer curve lies significantly below the measured curve; see Fig. 6.3. We also display in Fig. 6.3 the results for the case that the trapped charges are randomly distributed in a layer with thickness d of 3, 5, 30, and 100 nm. Since the length of the spacer in the self-assembling molecule is about 1.5 nm, see Fig. 6.1c, for $d = 3$ nm about half of the trapped charges would be located in the gate dielectric. For both $d = 3$ and $d = 5$ nm the predicted transfer curves lie above the transfer curve for trapped charges located in the channel but still significantly below the experimental transfer curve. We obtain a good fit to the experimental data for $d = 30$ nm. For $d = 100$ nm, the trapped charges interact only very weakly with the mobile charges in the transistor channel. As a result, the shape of the transfer curve is almost indistinguishable from the initial transfer curve and now lies above the measured curve.

In Fig. 6.4a we plot the simulated mobilities as a function of $V_G - V_{shift}$ for the different values of d. The increase of the mobility with gate voltage is a well-known effect of state filling.[19,22] We clearly see the influence of d on the mobility. The further away the trapped charges are from the monolayer, the weaker is the effect of the Coulomb scattering. In Fig. 6.4b we show the effective DOS for the different values of d. This effective DOS is obtained by adding to the random energy of each site in the lattice the Coulomb interaction energy with all the trapped charges. The effective DOS is significantly narrower for the case that the trapped charges have penetrated deep into the gate dielectric as compared to when they are in the monolayer. This then leads to a much higher mobility. The effect is completely analogous to the modulation doping in III-V semiconductor heterostructures, where the spatial separation of donors from the mobile carriers reduces the effect of Coulomb scattering. The interesting additional aspects of the present work are that the effect is tunable and reversible; see Fig 6.2.

Our conclusion that trapped charges in the SAMFET are located in the dielectric is compat-
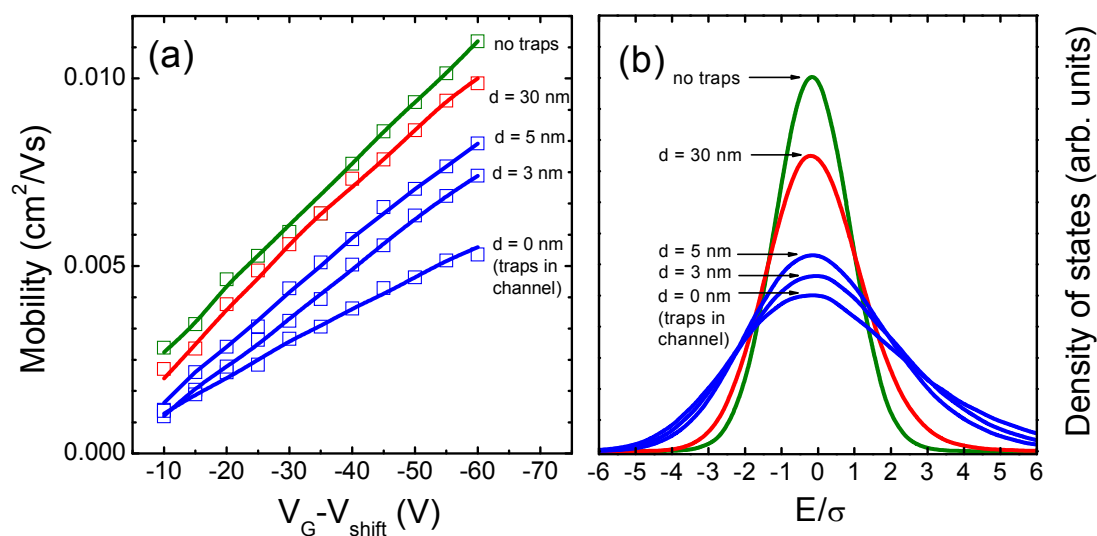
Figure 6.4: (a) Lines and symbols: simulated mobilities as a function of $V_G - V_{shift}$, corresponding to the results in Fig. 6.3. (b) Corresponding effective densities of states.

ible with a recent experiment in which the semiconducting organic layer of an OFET that had undergone bias stress was removed from the SiO_2 dielectric.[10] By using scanning Kelvin probe microscopy it was shown that after removal of the semiconductor the dielectric was carrying charge with a magnitude in agreement with the measured bias-stress effect before removal. That experiment was not able to distinguish charge trapping on the surface of the dielectric from charge trapping in the bulk of the dielectric. Our present analysis shows that in fact charge trapping takes place in the bulk of the dielectric.

The conclusion that charge trapping takes place in the bulk of the dielectric is in line with the proton-migration mechanism proposed in this thesis. This mechanism is based on hole-assisted production of protons in the accumulation layer of the semiconductor in an electrolytic reaction involving water and the subsequent migration of these protons into the gate dielectric. During recovery, the protons move back to the accumulation layer and get reconverted into holes. The observation that after a recovery period that is equal to the stress period the transfer curve has not fully returned to the initial transfer curve (see Fig. 6.2b) is in agreement with the predictions following from this mechanism; see Chapter 4. We note that the approximation of a uniform distribution of trapped charges up to a penetration depth d made in the present chapter is in fair agreement with the calculated proton profiles following from this mechanism for a long stress period; see Fig. 3.3. If this mechanism is also responsible for the bias-stress effect in the SAMFET investigated in this work it means that there should be residual water present in the SAMFET even under the vacuum conditions under which the bias-stress effect is investigated. Apparently, the vacuum conditions slow down the bias-stress effect as compared to ambient conditions,[15,23] but cannot eliminate it. This is an important conclusion for the development of techniques to control instabilities in OFETs caused by this effect.

6.4   Summary and conclusions

We investigated trapping of charges in a well-defined self-assembled monolayer field-effect transistor by studying the time evolution of the transfer curve while exposing the transistor to gate bias stress. Prolonged application of gate bias is used to tune the number of trapped charges. We performed two-dimensional Monte-Carlo simulations of the charge transport in this transistor in which the static random Coulomb field of the trapped charges is taken into account. This random Coulomb field leads to reduction of the current. The simulations show that the subtle change of the transfer curve after a long period of bias stress cannot be reproduced if the trapped charges are assumed to be located in or very close to the transistor channel. The change in the transfer curve can be reproduced if the trapped charges are assumed to be distributed in a layer with a thickness of several nanometers underneath the monolayer. We therefore conclude that the trapped charges are located in the gate dielectric. We stress that our results are applicable to organic field-effect transistors in general, because at typical gate biases the thickness of the accumulation layer in conventional thin-film organic field-effect transistors is very comparable to the height of the semiconducting core of the molecule in the self-assembled organic monolayer.

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Chapter 7

Bias-stress effect and HOMO energy of the semiconductor

The mechanism for the bias-stress effect in organic field-effect transistors presented in this thesis is based on hole-assisted production of protons in the accumulation layer and their subsequent migration into the gate dielectric. For a given organic semiconductor the time scale of the effect is determined by the diffusion of protons in the gate dielectric. On the other hand, the production of protons in the accumulation layer of the transistor strongly depends on the energy of the highest occupied molecular orbital (HOMO) of the semiconductor and should therefore influence the dynamics of the bias-stress effect. We derive an expression for the dependence of the characteristic time of the bias-stress effect on the HOMO energy of the semiconductor. We show that the time scale of the bias-stress effect decreases exponentially with increasing HOMO energy of the organic semiconductor.**

7.1   Introduction

In previous chapters, we studied the bias-stress effect, recovery, and the occurrence of anomalous current transients in organic field-effect transistors (OFETs) in the light of the proton migration mechanism. This mechanism is based on an equilibrium between holes and protons existing in the accumulation layer and the reversible motion of protons from the accumulation layer into the gate dielectric and back. In the presence of water, holes in the organic semiconductor, indicated below by OS^+, can be converted into protons in the electrolytic reaction

$$2H_2O + 4OS^+ \rightleftharpoons 4H^+ + O_2(g) + 4OS, \tag{7.1}$$
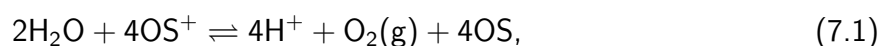
where OS refers to electrically neutral sites in the organic semiconductor. A similar charge transfer reaction occurs in carbon nanotube field-effect transistors, where electron transfer takes place from the nanotube to the oxygen dissolved in water.[1] From the equation above it is evident that an increase of the energy of the highest occupied molecular orbital, E_{HOMO}, should facilitate the electrolytic production of protons from holes, since an increase of E_{HOMO} makes the positively charged oxidized state of the organic semiconductor (OS^+) less stable. In other words, the equilibrium described by the above reaction equation will be shifted to the right with increasing E_{HOMO}. Under the assumption that there is thermodynamic equilibrium between protons in the accumulation layer and protons in the SiO_2 close to the interface with the semiconductor, we also proposed the following relation between the surface density $[OS^+]$ of holes in the accumulation layer and the volume density $[H^+]$ of protons in the SiO_2 at the interface with the semiconductor:

$$[H^+]_{interface} = \alpha [OS^+]_{accumulation layer}. \tag{7.2}$$

The parameter α in this equation determines the time scale at which the bias-stress effect occurs. In Section 7.2, we derive an expression for the dependence of α on E_{HOMO}. We will further highlight the strong dependence of α on ambient conditions. Finally, Section 7.3 contains a summary and the conclusions, as well as a discussion of the results.

7.2   Influence of HOMO energy on bias-stress dynamics

The forward reaction in Eqn. (7.1) shows that water is oxidized by the holes in the accumulation layer of the transistor producing protons. In fact, there are two reactions occurring in the accumulation layer of the transistor: the oxidation of water and the reduction of holes. The oxidation of water involves the reaction:

$$2H_2O \rightleftharpoons O_2 + 4H^+ + 4e^-. \tag{7.3}$$
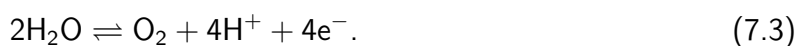
The redox potential for oxidation of water at a pH of 7 amounts to -0.57 V versus the standard calomel electrode (SCE).[2] The other redox reaction that we are interested in is

$$4OS^+ + 4e^- \rightleftharpoons 4OS, \tag{7.4}$$

showing the reduction of the positively charged oxidized state of the semiconductor. If we combine reactions Eqns. (7.3) and (7.4) we get reaction Eqn. (7.1), with a redox potential of $(E_{OS} - 0.57)$ V versus SCE, where E_{OS} is the oxidation potential of the semiconductor versus SCE. The total free energy change associated with the combined reaction Eqn. (7.1) is given by

$$\Delta G_{total} = -nF(E_{OS} - 0.57), \tag{7.5}$$

where n is the number of electrons transferred in the reaction and F is the Faraday constant (the charge of a mole of electrons).

The forward reaction in Eqn. (7.1) proceeds when ΔG_{total} is negative, implying that $E_{OS} > 0.57$ V. The work function of the semiconductor is equal to the electrochemical potential at which the semiconductor can be oxidized (versus SCE) plus 4.4 V.[2] E_{HOMO} is obtained by multiplying the work function by the elementary charge e. Therefore, production of protons in Eqn. (7.1) will proceed only if $E_{HOMO} > (0.57 + 4.4) = 4.97$ eV.

We can infer from the simple analysis above that with increasing E_{HOMO} the production of protons from water becomes increasingly favorable. This finding suggests that to eliminate the bias-stress effect in organic transistors, an organic semiconductor with a low E_{HOMO} should be chosen. Unfortunately, upon decreasing E_{HOMO}, the semiconductor becomes environmentally instable due to oxidation.

We can write the equilibrium constant K_{eq} for the reaction Eqn. (7.1) as

$$K_{eq} = \frac{[OS]^4[O_2][H^+]^4}{[H_2O]^2[OS^+]^4}, \tag{7.6}$$

where we have replaced the activity of the components by their concentrations. Here, the concentrations refer to the number of moles of the respective components per unit volume of the accumulation layer. In equilibrium at temperature T, $\Delta G = \Delta G_{total} + RT \log K_{eq} = 0$, where R is the Gas constant. In the following analysis we take for simplicity $[OS] = 1$. Combining Eqns. (7.2), (7.5), (7.6), and using the relation $R = N_A k_B$, where N_A is the avogadro number and k_B is the Boltzmann constant, we get

$$\alpha = \frac{[H^+]_{interface}}{[OS^+]_{accumulationlayer}} \propto \frac{[H^+]}{[OS^+]} = \frac{[H_2O]^{1/2}}{[O_2]^{1/4}} \exp\left[-\frac{\Delta G_{total}}{4k_B T}\right] \tag{7.7}$$

$$\propto \frac{[H_2O]^{1/2}}{[O_2]^{1/4}} \exp\left[\frac{E_{HOMO}}{4k_B T}\right]. \tag{7.8}$$

In Chapter 3, we obtained the characteristic time of the bias-stress effect $t_0 \equiv \frac{1}{\pi \alpha^2 D}$, where D is the diffusion coefficient of protons in the silicon-oxide. Inserting the above dependence of α on E_{HOMO} in the expression for this characteristic time, we obtain

$$t_0 = \frac{C}{\pi D} \frac{[O_2]^{1/2}}{[H_2O]} \exp\left[-\frac{E_{HOMO}}{2k_B T}\right], \tag{7.9}$$

where C is a constant.
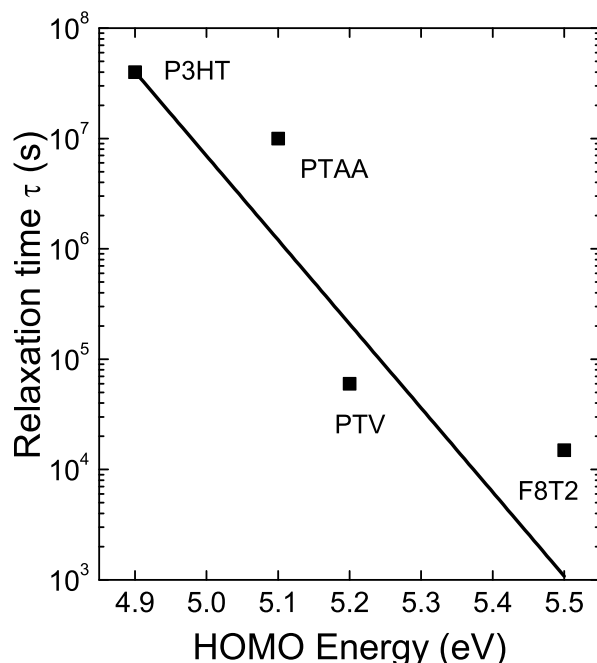
Figure 7.1: Relaxation times τ obtained from measurements under identical conditions of the bias-stress effect of OFETs[3] at temperature $T = 25\ °C$ as a function of the energy of the highest occupied molecular orbital for four different polymeric semiconductors: poly-3-hexylthiophene (P3HT), polytriarylamine (PTAA), poly-thienylene-vinylene (PTV), and poly-dioctyl-fluorene-co-bithiophene (F8T2). The line shows the fit according to the Eqn. (7.9) at $T = 25\ °C$.

We note that in the derivation above we have assumed that $[H^+]_{interface}/[OS^+]_{accumulationlayer}$ is proportional to $[H^+]/[OS^+]$. The replacement of $[OS^+]_{accumulationlayer}$ by $[OS^+]$ involves a replacement of a surface concentration by a volume concentration and should therefore be accompanied by a multiplication by a factor with the dimensions of a length, which should be of the order of the thickness of the accumulation layer. The replacement of $[H^+]_{interface}$ by $[H^+]$ should be accompanied by a dimensionless factor accounting for the continuity of the chemical potential of the protons at the interface between the semiconductor and the silicon-oxide.

It is clear from the Eqn (7.9) that increasing values of E_{HOMO} lead to an exponential decrease in the characteristic time of the bias-stress effect. The characteristic time also depends on the concentration of oxygen and water at the interface in the accumulation layer. The concentration of oxygen and water can be replaced by their respective partial vapor pressures. As a consequence, the characteristic time of the bias-stress effect is highly sensitive to the partial pressure of oxygen. In order to perform a fit of the Eqn (7.9) to experimental data, we consider the relaxation time τ in the stretched-exponential fits to bias-stress measurements of OFETs based on different organic semiconductors.[3] This relaxation time τ is proportional to the characteristic time t_0. It should then be ensured that the measurements are performed

under exactly the same conditions, i.e., the concentration of water and oxygen should be fixed for all experiments. In Fig. 7.1, the relaxation time τ for four different semiconductors, P3HT, PTAA, PTV, and F8T2, is shown as a function of E_{HOMO} of these polymers.[3] The value of E_{HOMO} for the different semiconductors was determined by cyclic voltammetry measurements. It is difficult to judge if the data follow the exponential dependence Eqn. (7.9). Although the experiments were done under nominally identical conditions, there could still be uncertainties in the amount of water and the partial pressure of oxygen in these experiments. Moreover, even if the ambient conditions would be completely identical, the water and oxygen uptake of the different polymers will be different. Nevertheless, we can definitely say that the trend is correct.

7.3 Summary and conclusions

In this chapter we presented an analysis of the influence of the energy of the highest molecular orbital (HOMO) of organic semiconductors on the dynamics of the bias-stress effect in organic field-effect transistors. The analysis was carried out within the framework of the proton migration mechanism, in which holes in the accumulation layer are in equilibrium with protons and can move into and out of the silicon-oxide gate dielectric. In the reaction between holes and water holes act as the oxidizing agent, reacting with water to produce molecular oxygen and protons. We have shown that with increasing HOMO energy of the organic semiconductor, the proton production is increasingly favored, leading to an exponential decrease of the characteristic time of the bias-stress effect. Due to uncertainties in the concentration of water and the partial pressure in measurements of the bias-stress effects of a sequence of organic semiconductors we were not able to obtain a quantitative fit with experiments. However, the predicted trend of a decreasing relaxation time with increasing HOMO energy is in agreement with what is experimentally observed.

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Chapter 8

Charge transport in organic field-effect transistors

Application of a gate bias to an organic field-effect transistor leads to the accumulation of charges in the organic semiconductor in a thin region near the gate dielectric. We study the layered distribution of charges in the organic semiconductor as a function of the thickness of the organic semiconductor and the applied gate voltage. We show that for low energetic disorder, the source-drain current increases with the thickness of the organic semiconductor. On the other hand, for high energetic disorder, the source-drain current first increases and then decreases with the thickness of the organic semiconductor. We rationalize the obtained results in the light of the Coulomb interaction between charges and the state-filling effect. The obtained results prompt for a new description of charge transport in organic field-effect transistors. Moreover, we show that the layered distribution of charge carriers has strong implications for the bias-stress effect as well.

8.1　Introduction

In organic field-effect transistors (OFETs), the application of a gate voltage leads to the formation of a conducting channel in the organic semiconductor extending from the source to the drain electrode. This channel is commonly referred to as the accumulation layer. Several studies carried out on OFETs with conjugated molecules and oligomers as organic semiconductors have established that charge transport in OFETs is quasi two-dimensional.[1] Charge transport in p-type OFETs, on application of negative gate bias, is confined within a few molecular layers on top of the gate dielectric. Experiments on sexithiophene FETs demonstrated that the first two monolayers sustain the whole source-drain current in the transistor.[2] OFETs with dihexylquaterthienyl as the organic semiconductor exhibit maxima in the hole mobility at one and two monolayers.[3] Recently, an experimental study was performed by Shehu *et al.* that strongly indicated a non-two-dimensional nature of the charge transport in the channel of an OFET.[4] In this study, the authors monitored the source-drain current *in situ* and in real time during the deposition of pentacene on the gate dielectric (silicon-dioxide). They claimed that the source-drain current in the transistor starts flowing when percolation of the first monolayer occurs and, depending on the deposition rate, saturates at a coverage in the range of 2-7 monolayers. The authors also claimed that the number of active layers contributing to the current and the spatial distribution of the charge carriers is modulated by the growth method.

In the other experimental study mentioned above it was shown that the thickness of the accumulation layer is in general larger than the thickness of the region where charge transport occurs.[2] Continuum models based on semi-infinite and structureless semiconductors cannot explain these experimental findings. According to continuum models, the screening depth of the gate electric field penetrating the organic semiconductor is of the order of a nanometer,[5,6] implying that the accumulation layer is confined to the first monolayer of the organic transistor.

A theoretical study based on Monte-Carlo simulations of the charge-carrier mobility in OFETs, taking energetic disorder and Coulomb interactions between the charges into account, showed that the charge carriers are confined in a conducting channel in the organic semiconductor with a thickness of about 5-6 nm.[7] It was shown that most of the charges reside in the first monolayer and that the distribution of charges decays rapidly with increasing distance into the organic semiconductor. The authors showed that with increasing gate voltage the most significant increase occurs in the first monolayer, although the charge carrier distribution changes throughout the organic semiconductor. The increased carrier density in the first monolayer, together with the well-known mobility-increasing state-filling effect,[8,9] was used to explain the observed increase in mobility with increasing gate voltage. The authors also claimed that, despite the fact that the accumulation layer extends a few nanometers into the semiconductor, the gate electric field makes the charge transport essentially two-dimensional, implying that only the first monolayer or maybe the first two monolayers contribute to the charge transport in OFETs. In this chapter we will argue that the latter view on charge transport in OFETs is not entirely correct. We will show that the dimensionality of the charge transport in the channel of an OFET is strongly dependent on the energetic disorder in the organic semiconductor. We will show that even for high gate voltages the transport can be non-two-dimensional. Our approach is based on Monte-Carlo simulations of charge transport in a regular lattice. To systematically

investigate the effect of energetic disorder and gate voltage on charge transport in OFETs, we will start with a purely two-dimensional structure of one monolayer and subsequently add monolayers to it. For each thickness of the semiconductor we will calculate the charge-carrier distribution as well as the current for different applied gate voltages. This approach is motivated by the experimental study of Shehu *et al.*[4]

The chapter is organized as follows. In Section 8.2, we discuss how Coulomb interactions between charges and the state-filling effect influence charge transport in the channel of an OFET. In Section 8.3, we describe the model of the OFET and the Monte-Carlo approach for determining the current in the channel. We demonstrate that for low energetic disorder, the source-drain current monotonically increases with the thickness of the organic semiconductor. On the other hand, for high energetic disorder, the source-drain current first increases and then decreases with the thickness of the organic semiconductor. Finally, Section 8.4 contains a summary and the conclusions.

8.2   The effect of Coulomb interactions and state filling

We first consider a two-dimensional lattice similar to that in Chapter 6. This corresponds to an OFET with a single monolayer of organic semiconductor, as shown in Fig. 8.1a. It is known that an increasing charge-carrier density leads to a higher carrier mobility in a disordered organic semiconductor, because of the state-filling effect.[8,10] At low carrier density, the average distance between charge carriers is so large that one carrier's motion is not affected by the presence of other carriers. The charge carriers occupy the low-lying states of the Gaussian density of states (DOS) and the energy barriers for charge transport are substantial, which results in a low mobility. Above a certain critical density,[11] the average energy of the charges increases substantially with increasing density, as the lowest-energy states are already filled. The activation energy for transport decreases, resulting in a higher mobility. Since in a single-monolayer OFET the charges are confined to the two-dimensional surface of the lattice, the Coulomb interactions between the charges increase as well. Due to the increased Coulomb fields of the randomly distributed charges, the effective density of states becomes broader, leading to a decrease in the mobility; see Chapter 6. These two competing effects determine the effective charge-carrier mobility in the lattice. In other words, the increase in mobility with increasing carrier density is less than what is expected from the state-filling effect alone.

Now consider the situation that another two-dimensional lattice is added on top of the first lattice as shown in Fig. 8.1b. This corresponds to an OFET with two monolayers of the organic semiconductor. To understand charge transport in this structure, the following should be considered:

1. State-filling effect: Since the charges now occupy a larger volume, the average carrier density decreases. The decrease in carrier density is expected to lead to a decrease in the carrier mobility.

2. Coulomb interaction: Since the charges now occupy a larger volume, the Coulomb interaction between the charges is reduced and this is expected to lead to an increase in the
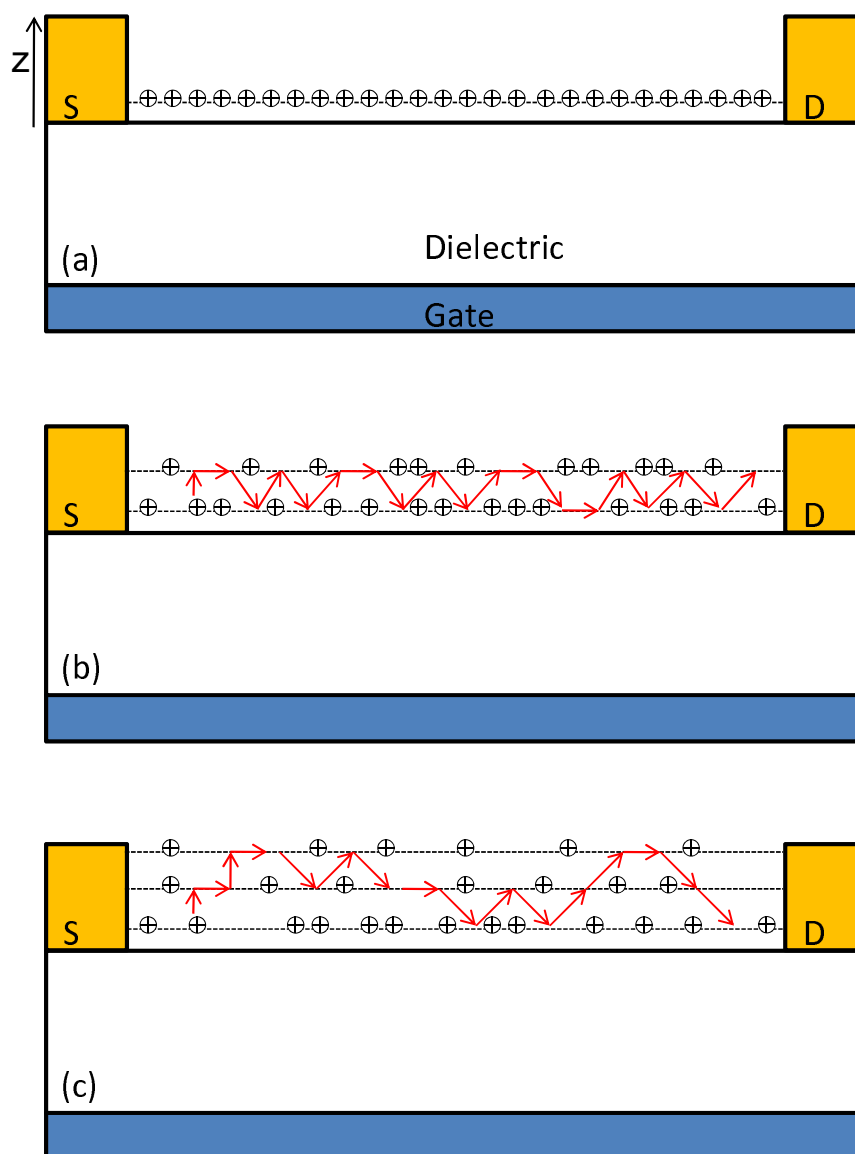
Figure 8.1: (a) Schematic of an OFET with a single monolayer. S and D denote the source and drain electrode, respectively. The monolayer is shown as a dotted line. Circles with a plus sign represent charge carriers (holes). In a single-monolayer OFET, all the charge carriers are confined to move in the two-dimensional surface $z = 0$. (b) OFET with two monolayers. The total number of charge carriers is the same as in (a). Some of the charges move from the first monolayer to the second one. (c) OFET with three monolayers. The total number of charge carriers is the same as in (a) and (b). Charges are now distributed in the three monolayers. Red arrows represent an imaginary trajectory a carrier may follow from the source to the drain electrode.

carrier mobility.

3. Availability of new paths: The trajectory of a charge moving from the source to the drain the electrode can be considered as a path taken by the charge during charge transport process. When a second monolayer is added to an OFET, new paths become available in the second monolayer in addition to the paths in the first monolayer. Moreover, many other new paths traversing both the first and the second monolayer also become available.

We already discussed the influence of the state-filling effect and Coulomb interaction between charges on the mobility of charge carriers. We now consider the effect of availability of new paths on addition of the second monolayer. Unlike the single monolayer OFET, in this structure charges can move on a non-two-dimensional trajectory. In this structure with two monolayers, charges can move from the first monolayer to the second one as shown in Fig. 8.1b. By adding the second monolayer to the OFET, charges which were earlier confined to the first monolayer and were not able to contribute to the current can now contribute to the total current. They can do so by finding an optimal path (with a net drift in the direction of the lateral electric field) utilizing both the first and the second monolayer. Whether the charge mobility increases or decreases with the addition of the second monolayer depends on which of the above mentioned effect(s) is dominant. If state-filling effect dominates over the other two, the charge carrier mobility will decrease on addition of the second monolayer. On the other hand, if the joint effect of reduced Coulomb interaction and the availability of new paths is dominant, the charge carrier mobility will increase on addition of the second monolayer.

Next, we consider further addition of monolayers and the effect of the size of the energetic disorder on the carrier mobility. On adding a third monolayer to an OFET for a given gate voltage, charges can further reduce their Coulomb interaction by moving to the third monolayer as shown in Fig. 8.1c. The average carrier density decreases, but the effect of this on the mobility will depend on the size σ of the energetic disorder in the organic semiconductor. We discuss two cases: very low energetic disorder ($\sigma \sim k_\mathrm{B}T$-$2k_\mathrm{B}T$) and high energetic disorder ($\sigma \geq 4k_\mathrm{B}T$), where k_B is the Boltzmann constant and T is the temperature. If many energetically low-lying states become available with the addition of the third monolayer, charges can move from the lower-lying monolayers to the third monolayer and become effectively trapped. This corresponds to an organic semiconductor with a high energetic disorder. In this case, the state-filling effect has a relatively larger influence on the mobility than the Coulomb interactions between the charges. Correspondingly, the charge-carrier mobility is expected to decrease with an increasing number of monolayers. On the other hand, if the energetic disorder is low, the state-filling effect has a smaller influence on the mobility than the Coulomb interactions between the charges. In this case, the charge carrier mobility is expected to increase with an increasing number of monolayers.

In the next section, we check the above by performing Monte-Carlo simulations of charge transport on lattices representing OFETs with a varying number of monolayers.

8.3 Monte-Carlo simulation of charge transport

We model the organic semiconductor as a set of N_z monolayers stacked on top of each other to to form a regular three-dimensional lattice. We model each monolayer as a square lattice of sites with lattice constant a. The vertical distance between the monolayers is also taken as a. The simulation box then has $N_x N_y N_z$ lattice sites, where N_x and N_y are the number of sites in the x and y direction, respectively. We assume that the charge transport occurs by phonon-assisted hopping of charges between sites. For the case of coupling to acoustical phonons this process is appropriately described by the Miller-Abrahams hopping rate[12]

$$
\begin{aligned}
W_{ij} &= \nu_0 exp\left[-2\alpha R_{ij} - \beta(E_j - E_i)\right], E_j \geq E_i, \\
&= \nu_0 exp[-2\alpha R_{ij}], \qquad\qquad\quad E_j < E_i.
\end{aligned}
\tag{8.1}
$$

Here, $\beta = 1/k_B T$, with k_B Boltzmann's constant, ν_0 is a phonon frequency, $R_{ij} \equiv |\mathbf{R}_i - \mathbf{R}_j|$ is the distance between sites i and j, and E_i and E_j are the on-site energies of sites i and j. For the inverse localization length of the wave functions α we have taken $10/a$.[8] The value taken for the inverse localization length of the wave functions α only influences the prefactor of the hopping rate, as long as it is large enough to suppress further than nearest-neighbor hopping. For the value $\alpha = 10/a$ that we have taken, this is the case.[8]

The on-site energies E_i contain a random contribution $E_{rand,i}$ that we will draw from the Gaussian DOS:

$$
g(E) = \frac{1}{\sqrt{2\pi}\sigma a^3} \exp\left[-\frac{E^2}{2\sigma^2}\right],
\tag{8.2}
$$

with σ the standard deviation of the DOS. We note that the combination of Miller-Abrahams hopping and Gaussian disorder has been very successful in describing charge transport in various organic semiconductors.[8,13]

Apart from this random contribution, the energy difference in Eqn. (8.1) contains two contributions:

1. The Coulomb interaction energy with all other charges, including the gate charge.

2. An electrostatic contribution $-eFR_{ijx}$ due to an electric field F, taken in the x direction of the lattice (e is the unit charge), due to a source-drain bias.

The Coulomb interaction of a charge will the other charges is taken into account in the following way. We split the total Coulomb interaction of a charge with all the other charges into three contributions.[14] (i) First, we take into account a short-range contribution, in which the Coulomb interaction energy with the charges within a sphere of radius R_c is taken into account explicitly. (ii) Next, we add a layer-averaged contribution, in which the Coulomb interaction energy with the other charges as well as that due to the applied gate electric field is taken into account in a layer-averaged way. Because this contribution also takes into account the layer-averaged Coulomb energy of charges in the disc-shape parts of the layers within the sphere, a double counting occurs. (iii) Therefore, we subtract a contribution due to these disc-shape parts to correct for this double counting. With increasing R_c, Coulomb interactions are taken into

account in an increasingly exact way, with full exactness for $R_c = \infty$. For a well-chosen finite value of R_c we can obtain a good compromise between accuracy and simulation speed. For the device simulations discussed later on, we have taken $R_c = 15a$.

Since charge transport occurs in a confined geometry, the Coulomb interaction between charges has to be adapted to this geometry. For simplicity, we assume that the gate dielectric and the organic semiconductor have the same relative dielectric constant ϵ_r. The surface of the gate dielectric is taken to be the $z = 0$ plane, with the z axis pointing into the organic semiconductor as shown in Fig. 8.1a. The electric potential due to a charge e at (x_e, y_e, z_e) at an arbitrary point $(x, y, z < N_z a)$ is

$$\frac{1}{4\pi\epsilon_0} \left(\frac{e/\epsilon_r}{\sqrt{(x - x_e)^2 + (y - y_e)^2 + (z - z_e)^2}} + \frac{e_t}{\sqrt{(x - x_e)^2 + (y - y_e)^2 + (z - z_{e,\text{img}})^2}} \right),$$

(8.3)

where $z_{e,\text{img}} = (2(N_z - 1)a - z_e)$ is the z-coordinate of the image of charge e, ϵ_0 is the vacuum permittivity, and $e_t = \left(\frac{\epsilon_r - 1}{\epsilon_r + 1} \right) \frac{e}{\epsilon_r}$ is the total bound charge induced by e at the interface between the semiconductor and vacuum. This result is formally derived in Appendix B.

We performed Monte-Carlo simulations for the charge transport in three-dimensional square lattices of $100 \times 100 \times N_z$ sites for different values of N_z in the following way. The relative dielectric constant of the gate dielectric as well as that of the semiconductors is taken to be $\epsilon_r = 3.9$, which corresponds to that of SiO_2, and the thickness of the gate dielectric is taken to be 200 nm. For all the calculations, we assumed a lattice constant $a = 1$ nm and temperature $T = 30°$ C. These parameters are the same as for the self-assembled monolayer field-effect transistor studied in Chapter 6.

We start with an empty lattice and fill it with a prescribed number of holes determined by the applied gate bias. After that, hops of holes are chosen with weights determined by the hopping rates Eqn. (8.1). A hopping time is chosen from an exponential distribution with an inverse decay time equal to the sum of all possible hopping rates. An applied electric field of $F = 0.1\sigma/ea$ was taken in the simulations, which is well within the linear regime of the charge transport. After about 10 million simulation steps, a stationary situation was obtained and the current was determined. An average over the currents for 15 disorder configurations of the on-site energies was taken until the error in the average current was smaller than 5%.

We show in Fig. 8.2 the simulated current as a function of the applied gate voltage for different numbers of monolayers N_z. These curves were calculated for four different values of the energetic disorder σ, indicated in the figure. It is clear from Fig. 8.2 that in the case of a low disorder, $\sigma = 2k_B T = 0.052$ eV, for all values of the gate voltage the current increases with increasing thickness of the semiconductor. On the other hand, in the case of a high energetic disorder, $\sigma = 5k_B T = 0.13$ eV, the current does not increase monotonically with increasing thickness of the semiconductor. When the thickness of the semiconductor increases from one monolayer to two monolayers, the current increases for all values of the applied gate voltage. With further increase in the thickness of the semiconductor, the current decreases for all values of the applied gate voltage. In the case of $\sigma = 3k_B T = 0.078$ eV, when the thickness of the semiconductor increases from one monolayer to two monolayers, the current increases for all
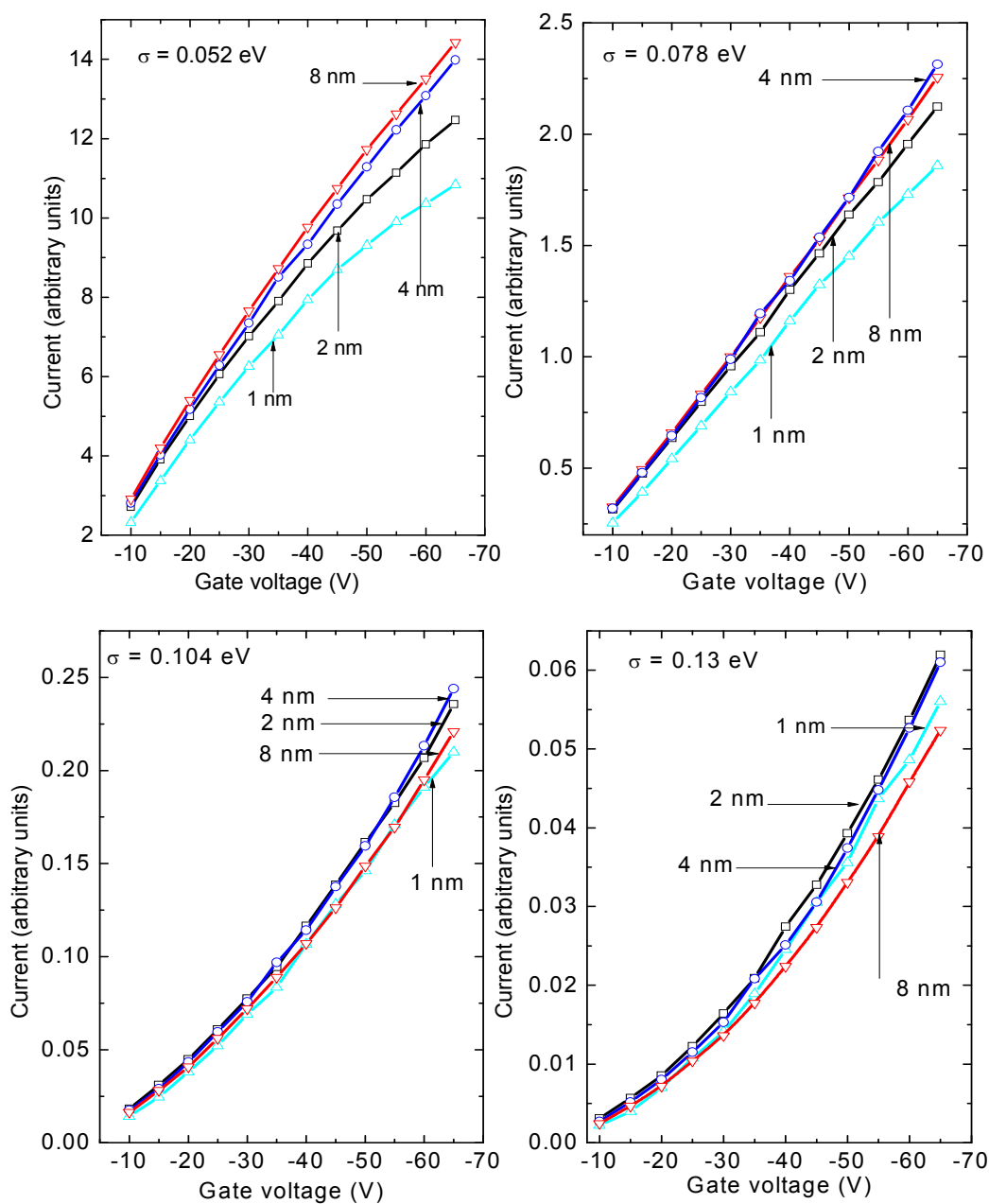
Figure 8.2: Current versus applied gate voltage for different number of monolayers of the semiconductor. The relative dielectric constant of the gate dielectric and the semiconductors is $\epsilon_r = 3.9$, which corresponds to that of SiO_2, and the thickness of the gate dielectric is 200 nm. The lattice constant is $a = 1$ nm and the temperature $T = 30°$ C. These parameters are the same as for the self-assembled monolayer field-effect transistor studied in Chapter 6.
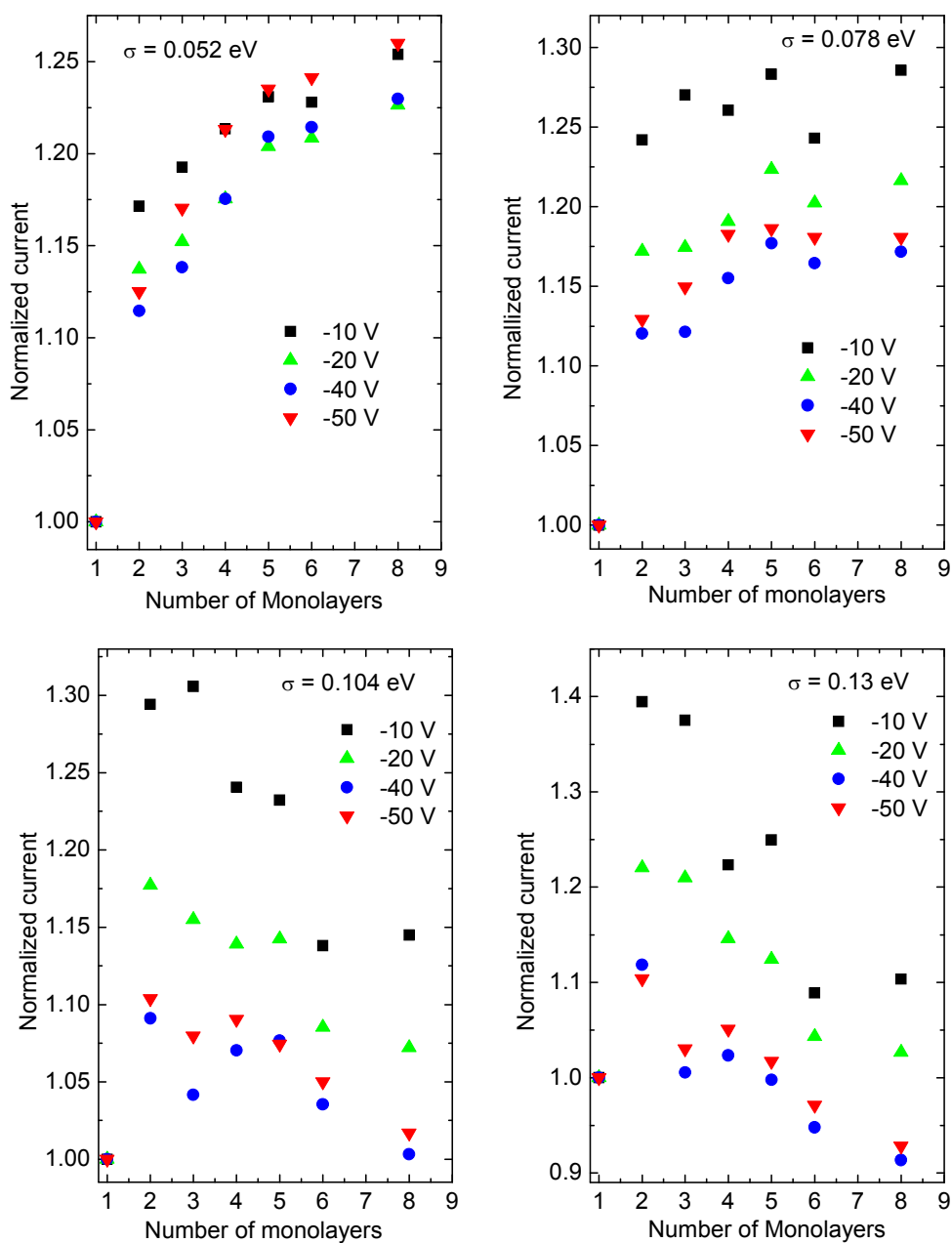
Figure 8.3: Normalized current versus number of monolayers for different applied gate voltages. Square: $V_G = -10V$, Triangle: $V_G = -20V$, Circle: $V_G = -40V$, and Inverted triangle: $V_G = -50V$. For $\sigma = 2k_B T = 0.052$ eV, current increases with thickness of the semiconductor. For $\sigma = 3k_B T = 0.078$, current increases when thickness of semiconductor increases from one monolayer to two. For thickness larger than two monolayers current shows a weak dependence on the thickness of semiconductor. For $\sigma = 4k_B T = 0.104$ and $\sigma = 5k_B T = 0.13$, current increases when thickness of semiconductor increases from one monolayer to two. For thickness larger than two monolayers current decreases with the thickness of the semiconductor.

values of the applied gate voltage. With further increase in the thickness of the semiconductor, the current shows a very weak dependence on the thickness. This can be clearly seen in Fig. 8.3, where we plot the current, normalized to the current for one monolayer, as a function of the thickness of the semiconductor for different values of the applied gate voltage.

The results above indicate the change in the nature of charge transport with addition of monolayers to the OFET. In the case of low energetic disorder ($\sigma = 2k_B T$), the increase in current with increasing number of monolayers clearly shows that the state-filling effect is not the dominant effect that influences the charge carrier mobility. The increase in the current is due to the joint effect of the reduced Coulomb interaction and the increase in number of available paths. It still needs to be investigated which of the two, reduced Coulomb interaction and the increase in the number of available paths, is the dominant effect that determines the increase in charge carrier mobility in the case of low energetic-disorder. The results are also indicative of the charge transport becoming three-dimensional with an increasing number of monolayers. In the case of high energetic disorder ($\sigma \geq 4k_B T$), the current increases on addition of the second monolayer. This suggests that similar to the low energetic disorder case, state-filling effect is not dominant when the number of monolayers is increased from one to two. On adding more monolayers, the current starts decreasing indicating that state-filling effect becomes dominant for $N_z \geq 3$. Even though the current starts decreasing, it still remains higher than that for a single monolayer OFET. It is only for relatively large values of N_z that the current is less than that for a single monolayer OFET. Although the decrease in current after two monolayers is due to the state-filling effect, it is not clear from the results above whether charges from the first and second monolayer follow a three-dimensional trajectory using the higher-lying monolayers. In other words, based on the current-voltage simulation results presented above, we cannot conclusively determine whether the charge transport becomes three-dimensional with an increasing number of monolayers. To unequivocally determine the dimensionality of charge transport, we need to investigate the path of current through different monolayers for different thicknesses of the semiconductor.

In Fig. 8.4, we plot the fraction of the total number of charges in each monolayer for different values of the applied gate voltage. Fig. 8.4a and Fig. 8.4b correspond to three and eight monolayers, respectively. As shown in Fig. 8.4a, at low gate voltage $V_G = -10$ V, the first monolayer contains only about half of the total number of charges for both low and high energetic disorder. With increasing gate voltage, the fraction of charges in the first monolayer increases. On increasing the thickness of the semiconductor, the fraction of charges in each of the monolayer decreases as shown in Fig. 8.4b for both low and high energetic disorder. The distribution profiles of charges in Fig. 8.4b does not decay all the way up to the last monolayer. From the fifth monolayer onwards, they start increasing again. The reason for the upturn of the profiles at higher lying monolayers is the following. The first 3-4 monolayers contain about 80% of the total number of charges which screen the applied gate electric field. If the electric field beyond these monolayers denoted by E_z becomes so weak that $E_z < \frac{\sigma}{ea}$, the interaction between charges lying in the region $N_z \geq 3$ is dominated by the short-range Coulomb interaction. In order to minimize this interaction, charges move as far away from each other as possible. Since the charges are confined within the semiconductor, charges accumulate near the boundary of the semiconductor. If the thickness of the semiconductor is increased further ($N_z \geq 8$), such
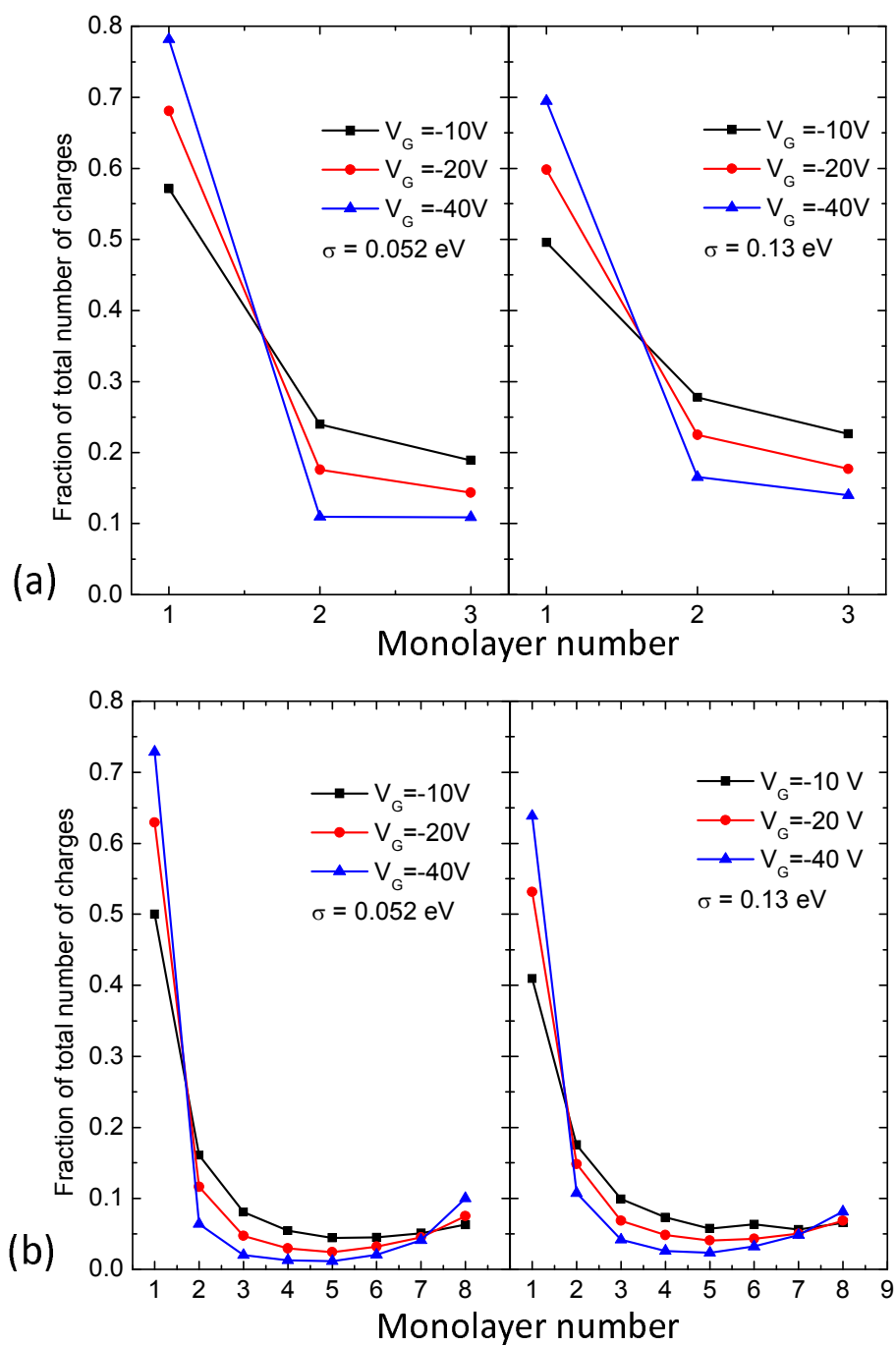
Figure 8.4: Fraction of total number of charges in each monolayer for different values of the applied gate bias. The thickness of the organic semiconductor is (a) 3 monolayers, and (b) 8 monolayers. The energetic disorder is indicated in the figures.

an upturn of the density profile would become less pronounced.

Our simulation results above show that the distribution of holes in the organic semiconductor depends on the number of monolayers and the applied gate bias. These findings have implications for the modeling of the proton migration mechanism for the bias-stress effect presented in Chapter 3. According to the mechanism, water present at the interface between SiO_2 and the organic semiconductor is oxidized by the holes in the accumulation layer. In the modeling, we considered only the surface concentration of holes and did not consider the distribution of holes perpendicular to the interface. The simulation results presented here clearly show that for low gate voltages this distribution penetrates rather far into the semiconductor. Moreover, the results also indicate that the thickness of the organic semiconductor layer in an OFET should influence the dynamics of the bias-stress effect. The threshold-voltage shift in an OFET with a thick organic semiconductor layer is expected to be slower than that in an OFET with a thin organic layer, because the holes are on average further away from the interface with the dielectric.

8.4   Summary and conclusions

In this chapter we investigated the effects of energetic disorder and gate voltage on charge transport in organic field-effect transistors. For different thicknesses of the organic semiconductor we calculated the charge-carrier distribution and current as a function of applied gate voltages by Monte-Carlo simulations of the hopping of the charges on a cubic grid of sites, taking into account Coulomb interactions between the charges. We showed that for low energetic disorder the lateral (source-drain) current increases with the thickness of the organic semiconductor. In the case of a high energetic disorder, the current increases when the thickness increases from one monolayer to two monolayers and then decreases with the addition of more monolayers. The initial increase is due to a reduction of the effects of Coulomb interactions between the charges and the availability of new paths traversing both monolayers. Beyond two monolayers, the mobility decreases for high energetic disorder, because the mobility-decreasing state-filling effect becomes more important. The simulations show that at low gate voltages, the distribution of charges extends a few monolayers into the semiconductor. We conclude that due to this penetration of charges into the semiconductor the threshold-voltage shift during bias stress of an organic transistor with a thick layer of organic semiconductor is expected to be slower than that of one with a thin layer.

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Chapter 9

Conclusions and outlook

The main goal of the work described in this thesis was to acquire an understanding of bias-induced changes of the electrical characteristics of organic field-effect transistors (OFETs). The work described is the theoretical part of a joint experimental-theoretical effort. On the experimental side, OFETs made from a p-type organic semiconductor (polytriarylamine, PTAA) on a silicon-dioxide (SiO_2) gate dielectric served as our main model system. The focus was primarily on the bias-stress effect, in which a prolonged application of a gate bias results in a monotonous shift of the threshold voltage towards the applied gate voltage. Prior to this work, the bias-stress effect was modeled only empirically by fitting the experimentally obtained threshold-voltage shift $\Delta V_{th}(t)$ as a function of time t with a stretched exponential function, $\Delta V_{th}(t) = V_0 \left(1 - \exp[-(t/\tau)^{\beta}] \right)$. Apart from a prefactor V_0 - which is found to be close to the applied gate bias - this fitting procedure involves two independent parameters: an exponent β and a relaxation time τ. Despite the practical use of this fitting procedure, at the beginning of this thesis work there was no mechanistic description of the effect that is in agreement with all the experimental observations (Chapter 2). Most of the proposed mechanisms only address the immobilization of charge during the bias stress. Other features, like the reversibility, the dependence on humidity, and the semiconductor-independent activation energy, did not receive much attention. In this work, we presented for the first time a mechanism that consistently explains all the main known features of the bias-stress effect.

In Chapter 3, we conclude that hole-assisted production of protons from water in the accumulation layer and their subsequent migration into the gate dielectric is the underlying mechanism of the bias-stress effect in p-type OFETs with SiO_2 as the gate dielectric. The dynamics of the bias-stress effect is determined solely by the motion of protons in the SiO_2 and can be modeled by taking only diffusion of protons into account. The presented model can very accurately describe the evolution of the threshold voltage as a function of time in these transistors. Since the time scale of the bias-stress effect is determined by the diffusion of protons in the gate oxide, the activation energy of the bias-stress effect is independent of the organic semiconductor. The magnitude of the activation energy agrees with a calculated value for transport of protons in the SiO_2.

In Chapter 4, we conclude that recovery of a transistor that has been exposed to bias stress is associated with the back-diffusion of protons from the SiO_2 to the organic semiconductor.

The extent of stressing determines the distance to which protons migrate during stressing. A partially stressed transistor recovers relatively faster than a transistor that has been almost fully stressed. We conclude that the recovery curves for the threshold-voltage shift cannot be described by a single stretched-exponential function. The measured time dependence of the threshold voltage during recovery quite accurately follows the model predictions, obtained using parameters from the modeling of the threshold-voltage shift for stress. An important conclusion for the application of OFETs is that an optimal operational time can be obtained by alternating short periods of operation with short periods of recovery.

In Chapter 5, we conclude that in order to describe the state of the transistor, the threshold voltage at any given moment as well as the biasing history of the transistor must be known. The biasing history of the transistor determines the density profile of protons in the bulk of the gate oxide. We conclude that different density profiles of protons can lead to the same threshold voltage, but that the further evolution of the electrical characteristics of the transistor depends on the particular profile. Consequently, anomalous non-monotonic current transients should occur in organic transistors during application of a time-varying gate bias, where after pre-stressing with a strongly negative gate bias the bias is stepped to a less negative voltage. During pre-stressing, protons produced in the semiconductor from holes and water diffuse into the SiO_2. After the step in the bias, these protons diffuse back to the semiconductor, where they are reconverted into holes. This should lead to a temporal increase in the number of holes and hence the transistor current. The measured current transients do indeed show the predicted anomalous behavior and accurately follow the model predictions, obtained using parameters from the modeling of the bias-stress effect. The conclusion is that the proton migration mechanism is able to predict this peculiar effect quantitatively.

According to the proton migration mechanism, a build-up of charges in the form of protons occurs in the bulk of SiO_2 away from the channel of the transistor. Other proposed mechanisms have focussed on trapping of holes in or very near the channel of the transistor. In Chapter 6, we conclude that the subtle change of the transfer curve (source-drain current as a function of gate voltage for a given source-drain bias) after a long period of bias stress cannot be reproduced if the trapped charges are assumed to be located in or very close to the transistor channel. The change in the transfer curve can only be reproduced if the trapped charges are assumed to be distributed in a layer with a thickness of several nanometers underneath the monolayer. Coulomb scattering from charges trapped in the transistor channel has a large influence on the mobility whereas for charges trapped at a distance from the channel, the Coulomb scattering is highly reduced. We hence conclude that the subtle change in the transfer curve is in agreement with the proton migration mechanism.

In Chapter 7, we conclude that the timescale of the bias-stress effect should decrease exponentially with increasing energy E_{HOMO} of the highest occupied molecular orbital of the organic semiconductor. Increasing E_{HOMO} facilitates the electrolytic production of protons from holes. Due to uncertainties in the concentration of water and the partial pressure in measurements of the bias-stress effects of a sequence of organic semiconductors we could not obtain a quantitative fit with experiments, but we conclude that the observed trend is in agreement with the prediction of the proton migration mechanism.

In Chapter 8, we conclude that the dimensionality of charge transport in an organic field-

effect transistor depends on the energetic disorder in the semiconductor and the applied gate voltage. Due to the distribution of charges extending into the semiconductor, during stressing the threshold voltage shift in an organic transistor with several monolayers of the organic semiconductor is expected to be slower than that in a single monolayer organic transistor.

Our final conclusion is that the goal to acquire an understanding of bias-induced changes of the electrical characteristics of organic field-effect transistor has been reached to a large extent. However, even though our model for bias-stress effect explains many aspects of this effect in p-type organic field-effect transistors with silicon-oxide as gate dielectric, several interesting questions still need to be addressed. We propose research in the following directions:

1. Calculations within the framework of density-functional theory show that water at the Si-SiO$_2$ interface undergoes oxidation to produce protons in the presence of holes. In our model for the bias-stress effect it has been assumed that the same reaction takes place at the interface between an organic semiconductor and SiO$_2$. We suggest that this assumption can be theoretically tested by doing similar density-functional calculations on an interface between an organic semiconductor and SiO$_2$.

2. In the proton migration model for the bias-stress effect, the volume concentration of protons in the SiO$_2$ gate-dielectric at the interface with the semiconductor is assumed to be proportional to the surface concentration of holes in the accumulation layer. We assumed here that the charge transport in the channel of transistor is predominantly two-dimensional. This assumption is justified for high gate fields. However, with time the threshold voltage shifts towards the applied gate bias, leading to a decrease of the gate field. For low gate fields, the holes will be distributed across several nanometers in the organic semiconductor. At the same time, most of the water will not reside in the bulk of the semiconductor but at the surface of the SiO$_2$. It should be possible to extend the model to describe the situation at the interface between the SiO$_2$ and the semiconductor better.

3. We showed that the relaxation time τ of the bias-stress effect should decrease exponentially with increasing HOMO energy of the organic semiconductor, $\tau \sim \exp(-E_{\mathrm{HOMO}}/2k_{\mathrm{B}}T)$. However, we did not obtain good quantitative agreement with the experimental data. Although we attributed this to the uncertainties in the concentration of water and the partial pressure of oxygen, our analysis could be too simplistic. In deriving the relation between α (defined as the ratio of the volume density of protons in the gate dielectric to the surface density of holes in the accumulation layer) and the HOMO energy of the semiconductor, we have neglected a possible coordination shell of water molecules surrounding the protons. Moreover, we have not considered the different affinities for water and oxygen that different organic semiconductors may have. The derivation of τ can be generalized to include these effects, possibly leading to a better agreement.

4. We showed that the relaxation time of the bias-stress effect depends on the concentration of oxygen in the accumulation layer. According to the model prediction, the bias-stress

effect should slow down with increasing partial pressure of oxygen. We suggest an experimental study in which the dynamics of the bias-stress effect is studied by varying the partial pressure of oxygen.

5. We investigated only transistors with p-type organic semiconductors and SiO_2 as the gate dielectric. The proton migration mechanism was developed for such transistors. Experiments have shown that the bias-stress effect also occurs in transistors with gate-dielectrics different than SiO_2. It has also been shown that transistors with a crystalline organic semiconductor on a SiO_2 gate dielectric also show the bias-stress effect. Moreover, even n-type organic transistors show a similar bias-stress effect. It is known that a charge transfer reaction takes place in the channel of n-type organic transistors as well, in which the organic semiconductor is oxidized by oxygen dissolved in water. The proton migration mechanism can possibly be extended to include these cases as well.

6. The bias-stress effect is also observed in thin-film amorphous-silicon transistors with silicon nitride as the gate dielectric. Trapping of charges in the gate dielectric has been suggested as the mechanism of the effect. The dynamics of the effect is similar to that observed in the OFETs. To test whether the proton migration mechanism is applicable to amorphous-silicon transistors as well, it would be interesting to calculate the activation energy of diffusion of protons in silicon nitride and to compare it with the known activation energy of $\sim$0.97 eV.

With our understanding of the bias-stress effect, we suggest the following measures to ensure a better operational stability of organic field-effect transistors:

1. Prevent water from reaching the accumulation layer. A way to achieve this is by using a hydrophobic dielectric surface, e.g., by treatment of the dielectric surface with hexamethyldisilazane prior to deposition of organic semiconductor. Another way to achieve this is by encapsulation of the transistor.

2. Use a dielectric in which protons cannot penetrate. If the presence of water cannot be prevented, electrolytic production of protons in the accumulation layer will occur. However, if the protons cannot penetrate into the gate dielectric the bias-stress effect can be avoided. At present, we do not know of any such dielectric used in Organic field-effect transistors.

3. Pulsed operation of the transistors. Although the bias-stress effect is detrimental, it is reversible by recovery when the electrodes are grounded. Recovery takes a relatively longer time with a longer operation period of the transistor. However, if the transistor is operated for a short period, it needs a relatively short period of time to recover. An optimal sustained operation can therefore be obtained by alternating short periods of operation with short periods of recovery.

Appendix A

Solution of the drift-diffusion equation

In Chapter 3, the motion of protons in the silicon-dioxide was modeled using the following drift-diffusion equation:

$$\frac{\partial}{\partial t}p(x,t) = \mu p(x,t)E(x,t) - D\frac{\partial}{\partial x}p(x,t). \tag{A.1}$$

D and μ refer to the diffusion coefficient and mobility of protons in the silicon-dioxide, respectively, and the Einstein's relation $D/\mu = k_{\mathrm{B}}T/e$ is assumed valid. This equation can be written in the dimensionless form by defining dimensionless distance into the oxide, proton density, Electric field, and time,

$$
\begin{aligned}
\tilde{x} &= \frac{x}{L_{\mathrm{ox}}}, \\
\tilde{p}(\tilde{x},\tilde{t}) &= \frac{p(x,t)}{\alpha h_0(t=0)}, \\
\tilde{E}(\tilde{x},\tilde{t}) &= \frac{L_{\mathrm{ox}}}{V_{\mathrm{G0}}}E(x,t), \\
\tilde{t} &= \frac{\mu V_{\mathrm{G0}}}{L_{\mathrm{ox}}^2}t.
\end{aligned}
\tag{A.2}
$$

Here, L_{ox} is the oxide thickness, V_{G0} is the applied gate bias, and $h_0(t=0)$ is the surface-density of holes in the accumulation layer at time $t=0$. As defined in Chapter 3, α is the proportionality constant having dimensions of inverse length, relating the surface-density of holes in the accumulation layer to the volume density of holes in the gate dielectric at the interface by $p(0,t) = \alpha h_0(t)$.

We define another quantity,

$$F(\tilde{x},\tilde{t}) = \int_{\tilde{x}}^{1} p(\tilde{x},\tilde{t})d\tilde{x}. \tag{A.3}$$

Under the assumption that protons do not reach the gate electrode during the stressing

period, the dimensionless form of the drift-diffusion equation can now be written as:

$$\frac{\partial}{\partial \tilde{t}} F(\tilde{x}, \tilde{t}) = \tilde{p}(\tilde{x}, \tilde{t}) \tilde{E}(\tilde{x}, \tilde{t}) - \gamma \frac{\partial}{\partial \tilde{x}} \tilde{p}(\tilde{x}, \tilde{t}), \tag{A.4}$$

where $\gamma = k_B T / e V_{G0}$. The electric field in the oxide can be written as,

$$\tilde{E}(\tilde{x}, \tilde{t}) = 1 - \alpha L_{ox} F(\tilde{x}, \tilde{t}) + \alpha L_{ox} \int_0^1 \tilde{x} \tilde{p}(\tilde{x}, \tilde{t}) d\tilde{x}, \tag{A.5}$$

The Eqns. (A.3), (A.4), and (A.5) can be solved numerically by advancing time in small steps to obtain $\tilde{p}(0, \tilde{t})$ from which the hole density in the channel can be obtained as $h_0(\tilde{t}) = \tilde{p}(0, \tilde{t}) h_0(t = 0)$. The threshold voltage $V_{th}(t)$ is obtained from $V_{th}(t) = \frac{e}{C}(c_0 - h_0(t))$.

Appendix B

Dielectric discontinuity

Consider the situation shown in the Fig. B.1 below. Charge q is placed at position $x = 0, y = 0, z = d$ in a dielectric medium of susceptibility χ_1. The permittivity of the medium is $\epsilon_1 = (1 + \chi_1)$. The half-space $z < 0$ is filled with a dielectric of susceptibility χ_2. We wish to calculate the potential in the half-space $z \geq 0$ due to the charge q, the polarization charge surrounding q, and the induced surface-charge at the interface between the two dielectrics.
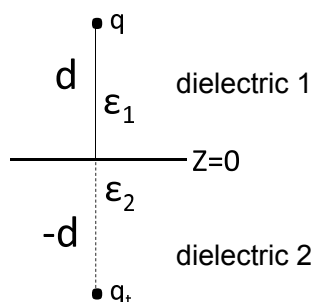

Figure B.1: Charge q is positioned at a distance d above a dielectric of permittivity ϵ_2. The charge is lying in a medium of permittivity ϵ_1. The total bound surface-charge induced by q is denoted by q_t. To get the potential in the half-space $z \geq 0$, the original problem should be replaced with the following: Remove both dielectrics. Keep q at its original position and include the polarization charge q_p surrounding it. Place q_t at a distance of d below $z = 0$. The potential at any point (x, y, z) with $z \geq 0$ is given by the sum of potentials due to q, q_p, and q_t.

The polarization charge q_p surrounding q is given by,

$$q_p = -\frac{\chi_1}{\chi_1 + 1} q. \tag{B.1}$$

This implies that the total charge at $x = 0, y = 0, z = d$ is $q + q_p = q/\epsilon_1$. Let's assume that the surface-charge density on the lower surface of dielectric 1 is σ_1 and on the upper surface of

dielectric 2 is σ_2. The z-component of electric field at any point P_1 $(x, y, z = 0^+)$ just above the interface in the dielectric 1 can be written as,

$$E_{z1} = -\frac{1}{4\pi\epsilon_0}\frac{qd/\epsilon_1}{(r^2 + d^2)^{3/2}} + \frac{\sigma_1}{2\epsilon_0} + \frac{\sigma_2}{2\epsilon_0}, \tag{B.2}$$

where r is the distance between $(x = 0, y = 0, z = 0)$ and P_1. Similarly, the z-component of electric field at any point P_2 $(x, y, z = 0^-)$ just below the interface in the dielectric 2 can be written as,

$$E_{z2} = -\frac{1}{4\pi\epsilon_0}\frac{qd/\epsilon_1}{(r^2 + d^2)^{3/2}} - \frac{\sigma_1}{2\epsilon_0} - \frac{\sigma_2}{2\epsilon_0}, \tag{B.3}$$

where r is the distance between $(x = 0, y = 0, z = 0)$ and P_2. The surface-charge density can be obtained as,

$$\sigma_1 = -\epsilon_0\chi_1 E_{z1}, \tag{B.4}$$

$$= \frac{1}{4\pi}\frac{qd}{(r^2 + d^2)^{3/2}}\frac{\epsilon_2\chi_1/\epsilon_1}{[1 + (\chi_1 + \chi_2)/2]} \tag{B.5}$$

$$\sigma_2 = \epsilon_0\chi_2 E_{z2} \tag{B.6}$$

$$= -\frac{1}{4\pi}\frac{qd}{(r^2 + d^2)^{3/2}}\frac{\chi_2}{[1 + (\chi_1 + \chi_2)/2]}. \tag{B.7}$$

The total bound surface-charge density is,

$$\sigma_t = \sigma_1 + \sigma_2 \tag{B.8}$$

$$= \frac{1}{4\pi}\frac{qd}{(r^2 + d^2)^{3/2}}\frac{\chi_1 - \chi_2}{\epsilon_1[1 + (\chi_1 + \chi_2)/2]}. \tag{B.9}$$

The total bound surface-charge q_t is obtained as,

$$q_t = \int_0^\infty \sigma_t 2\pi r\, dr = \left(\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2}\right)\frac{q}{\epsilon_1}. \tag{B.10}$$

This charge q_t is shown in the Fig. B.1 above lying at $-d$ in the dielectric 2. The potential at any point $(x, y, z \geq 0)$ can be written as,

$$\frac{1}{4\pi\epsilon_0}\left(\frac{q/\epsilon_1}{\sqrt{x^2 + y^2 + (z - d)^2}} + \frac{q_t}{\sqrt{x^2 + y^2 + (z + d)^2}}\right). \tag{B.11}$$

In the Eqn. (B.11), if we substitute $z = 0$, $\epsilon_1 = \epsilon_{SiO_2}$, and $\epsilon_2 = 1$, we get,

$$V(x, y, 0) = \frac{2q}{4\pi\epsilon_0(\epsilon_{SiO_2} + 1)R}, \tag{B.12}$$

where $R = \sqrt{x^2 + y^2 + d^2}$.

Summary

Modeling of bias-induced changes of organic field-effect transistor characteristics

Organic semiconductors offer exciting possibilities in developing new types of solar cells, photodetectors, light emitting diodes and field-effect transistors. Important advantages of organic semiconducting materials over their inorganic counterparts are their chemical tunability, their low weight, their relative low cost and the ease in which they can be processed. Many organic semiconductors can be processed from solution by using relatively cheap techniques like ink-jet printing or spin-coating, whereas ultra-clean high-vacuum conditions and high temperatures are required for inorganic semiconductors. Organic-based semiconductors in thin-film form are projected to be active elements in plastic-based circuits. In particular, using organic field-effect transistors as switching or logic elements opens up a wide range of possibilities into developing applications. However, organic field-effect transistors exhibit an operational instability. On applying a gate bias to a transistor, the on-current slowly decreases with time eventually going to zero, which is caused by a shift of the threshold voltage. This phenomenon is known as the bias-stress effect and severely hampers the application of organic transistors. For example, in an active matrix display, where light emission from each pixel is proportional to the current supplied by the driving transistor, any change in source-drain current with time is going to impact the brightness of the pixel. The main goal of the work described in this thesis has been to understand and model bias-induced changes of the electrical characteristics of organic field-effect transistors. The work described is the theoretical part of a joint experimental-theoretical effort.

In Chapter 2, the bias-stress effect is presented and its main aspects are highlighted. Some of the previously reported mechanisms for the bias-stress effect are briefly discussed, namely trapping mechanisms, a mechanism based on bipolarons, a mechanism based on water-induced polaron formation, and a contact degradation mechanism. However, there are many aspects of the bias-stress effect that cannot be consistently explained within the framework of these mechanisms. In particular, the fact that the bias-stress effect is thermally activated with an activation energy of about 0.6 eV, independent of the organic semiconductor used, cannot be explained by any of the mechanisms listed above. Experimental studies have established that water is the primary agent causing the bias-stress effect. An increase in humidity accelerates the bias-stress effect, whereas operating the device in vacuum practically eliminates the effect.

In Chapter 3, a new mechanism for the bias-stress effect is presented. Reversible proton

migration into the gate oxide is proposed as the main cause of the bias-stress effect in p-type organic transistors with silicon-dioxide (SiO_2) as the gate dielectric. Protons are produced in an electrolytic redox reaction between holes and water in the accumulation layer of the transistor. In this reaction, water is oxidized by holes producing protons and oxygen. This reaction essentially establishes an equilibrium between holes and protons in the accumulation layer. The protons produced in the accumulation layer subsequently migrate into the SiO_2. It is assumed that, independent of the organic semiconductor, the dynamics of the bias-stress effect is determined solely by the motion of protons in SiO_2. The model is called the proton-migration model. The motion of protons away from the accumulation layer into the SiO_2 has two consequences: (i) more holes are converted into protons in the accumulation layer, and (ii) the protons in the SiO_2 screen the gate field, giving rise to the observed threshold-voltage shift. Taking only diffusion into account a model is developed that has only one parameter: a characteristic time. The predicted threshold-voltage shift is very close to a stretched-exponential function, which has often been used as an empirical fit. The model explains the role of water as the source of protons. Since the time scale of the bias-stress effect is determined by the motion of protons in the SiO_2, the activation energy of the bias-stress effect is independent of the organic semiconductor. The activation energy of the effect indeed corresponds to that for transport of protons in the silicon-dioxide.

In Chapter 4, the recovery of a transistor that has been exposed to bias stress is described within the proton-migration model. Recovery is associated with the backward shift of the threshold voltage of an organic transistor that has been exposed to stressing. During stressing protons migrate into the SiO_2. The depth of penetration depends on the extent of stressing. At the end of stressing, the threshold voltage has shifted to the applied gate voltage and the transistor is in the off state. Applying zero gate bias to the transistor results in a backward shift of the threshold-voltage. Protons that have migrated into the oxide during stressing diffuse back to the semiconductor, where they are converted back into holes. Since the applied gate bias is zero, these holes are carried away by the source and drain electrodes. Recovery is modeled quantitatively within the proton-migration mechanism. The model predicts that the extent of stressing has a large influence on the dynamics of the recovery, which is in agreement with experiments. Experimentally obtained threshold-voltage shifts during recovery for different values of stressing periods clearly show that the dynamics of recovery is not governed by a single relaxation time. The measured time dependence of the threshold voltage during recovery quite accurately follows the model predictions, obtained using parameters from the modeling of the threshold-voltage shift for stress.

In Chapter 5, the predictions of the proton-migration model for a dynamic, time dependent, gate bias are tested. The model makes the following prediction: stressing the transistor with a highly negative gate voltage for a certain period of time and thereafter switching the gate voltage to a less negative value leads to a temporary recovery of the transistor, despite the fact that the transistor is under monotonous stressing. This temporary recovery is experimentally observed as an anomalous increase in the current. The occurrence of the resulting non-monotonic current transients was verified experimentally. The measured current transients accurately follow the model predictions, obtained using parameters from the modeling of the bias-stress effect in Chapter 3.

In Chapter 6, the effect of Coulomb scattering on the mobility of the charge carriers in the channel of the transistor is investigated. It is shown that Coulomb scattering from charges trapped in the channel of the transistor has a major effect on the mobility of the mobile charges in the transistor channel. The number of trapped charges is tuned by a prolonged application of the gate bias. Two cases are considered: (i) charges trapped in the channel, and (ii) charges trapped in the gate dielectric beneath the organic semiconductor. The distance over which the trapped charges are spread out in the gate dielectric is varied from 1 nm to 100 nm. Two-dimensional Monte-Carlo simulations of the charge transport in this transistor are performed in which the static random Coulomb field of the trapped charges is taken into account. The simulations show that the change in mobility of charge carriers in the channel of the transistor is substantially reduced if the trapped charges are assumed to be located in or very close to the transistor channel. The experimentally observed decrease in mobility is much smaller than that obtained from these simulations. The decrease in mobility is accurately obtained if in the simulations the trapped charges are assumed to be distributed in a layer with a thickness of a few tens of nanometer underneath the monolayer. This finding provides strong evidence for the proton migration mechanism.

In Chapter 7, the dependence of the time scale of the bias-stress effect on the organic semiconductor is investigated. The model predicts that this time scale should decrease exponentially with increasing energy of the highest occupied molecular orbital of the organic semiconductor. This was tested by comparing the relaxation times of organic field-effect transistors of organic semiconductors with different HOMO energies. The observed trend is correct, but the exponential dependence could not be quantitatively verified, because of uncertainties in the water and oxygen uptake of the semiconductors.

In Chapter 8, the effect of energetic disorder and gate voltage on charge transport in organic field-effect transistors is investigated. Simulations show that for low energetic disorder, the source-drain current increases with the thickness of the organic semiconductor. For high energetic disorder, the source-drain current first increases and then decreases with the thickness of the organic semiconductor. The observed behavior of current versus thickness of organic semiconductor is due to the joint effect of coulomb interactions between charges and the state-filling effect. For low energetic disorder, state-filling effect has relatively less influence on the mobility than the Coulomb interaction. In this case, the charge carrier mobility therefore increases with increasing number of monolayers. For high energetic disorder, state-filling effect has relatively larger influence on the mobility than the Coulomb interaction. Correspondingly, the charge carrier mobility decreases with increasing number of monolayers.

In summary, we can say that the proton-migration model has been able to describe all the main features of bias-induced changes of p-type organic field-effect transistors with silicon-dioxide as gate dielectric. The model has even triggered new experiments, which have verified the theoretical predictions. We conclude that the objective of this thesis work, to understand and model the electrical characteristics of organic field-effect transistors and identify the mechanism of the bias-stress effect, has been fully achieved.

List of publications

1. *Effect of Coulomb scattering from trapped charges on the mobility in an organic field-effect transistor*
   A. Sharma, N. M. A. Janssen, S. G. J. Mathijssen, D. M. de Leeuw, M. Kemerink, P. A. Bobbert
   Physical Review B **2011**, *83*, 125310.

2. *Proton migration mechanism for operational instabilities in organic field-effect transistors*
   A. Sharma, S. G. J. Mathijssen, E. C. P. Smits, M. Kemerink, D. M. de Leeuw, P. A. Bobbert
   Physical Review B **2010**, *82*, 075322.

3. *Bias stress effect and recovery in organic field effect transistors: proton migration mechanism*
   A. Sharma, S. G. J. Mathijssen, M. Kemerink, D. M. de Leeuw, P. A. Bobbert
   SPIE Proceedings **2010**, *7778*, 77780q.

4. *Anomalous current transients in organic field-effect transistors*
   A. Sharma, S. G. J. Mathijssen, T. Cramer, M. Kemerink, D. M. de Leeuw, P. A. Bobbert
   Applied Physics Letters **2010**, *96*, 103306.

5. *Proton migration mechanism for the instability of organic field-effect transistors*
   A. Sharma, S. G. J. Mathijssen, M. Kemerink, D. M. de Leeuw, P. A. Bobbert
   Applied Physics Letters **2009**, *95*, 253305.

6. *Charge trapping at the dielectric of organic transistors visualized in real time and space*
   S. G. J. Mathijssen, M. Kemerink, A. Sharma, M. Cölle, P. A. Bobbert, R. A. J. Janssen, D. M. de Leeuw
   Advanced Materials **2008**, *20*, 975-979.

7. *Scalable General High Voltage MOSFET Model inlcuding Quasi-Saturation and Self-Heating effect*
   Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. Baguenier Desormeaux, <u>A. Sharma</u>, M. Declercq, A. M. Ionescu
   Solid State Electronics **2006**, *50*, 1801-1813.

Manuscripts in preparation

1. *Distribution and transport of charges in organic field-effect transistors*
   <u>A. Sharma</u>, D. M. de Leeuw, M. Kemerink, P. A. Bobbert

2. *Influence of HOMO energy on the dynamics of the bias-stress effect in organic field-effect transistors*
   <u>A. Sharma</u>, S. G. J. Mathijssen, M. Kemerink, P. A. Bobbert, D. M. de Leeuw

Curriculum Vitae

Abhinav Sharma was born on October 21st 1983 in Moradabad, India. After finishing secondary school at the Meerut Public School, Meerut, India, he started in 2001 the study Electrical Engineering at the Indian Institute of Technology-Kanpur (I.I.T-K). During his studies he carried out an internship in the Processor Architecture Laboratory, École Polytechnique Fédérale de Lausanne, Switzerland under supervision of prof.dr. E. Charbon in which he implemented a Time-to-digital converter used in Single-photon diode-array on FPGA (Field-programmable gate-array). His M.Sc. research work was carried out in the Microelectronics group under supervision of prof.dr. B. Mazhari at the Indian Institute of Technology-Kanpur which concerned a theoretical investigation of contact-resistance in top-contact organic field-effect transistors. In June 2006, he worked at Nano-electronics Device Laboratory, École Polytechnique Fédérale de Lausanne, Switzerland under supervision of dr. A. Ionescu on modeling of mobility in disordered organic semiconductors. From September 2006 till April 2007, he worked at Texas Instruments, Bangalore, India as Design Engineer in the Advanced Embedded Controls group. In June 2007, he started with his Ph.D. research under supervision of dr. P. A. Bobbert and prof.dr. M. A. J. Michels in the Theory of Polymers and Soft Matter group at the faculty of Applied Physics, TU/e. During his PhD., he guided one student for his bachelor project. He is the recipient of best instructor award for second year physics lab course in the year 2008 and best instructor award for third year computational physics course in the year 2009. The most important results of this Ph.D. research are presented in this thesis.

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Abhinav