Picosecond Femtojoule Resistive Switching in Nanoscale VO$_2$ Memristors

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ABSTRACT: Beyond-Moore computing technologies are expected to provide a sustainable alternative to the von Neumann approach not only due to their down-scaling potential but also via exploiting device-level functional complexity at the lowest possible energy consumption. The dynamics of the Mott transition in correlated electron oxides, such as vanadium dioxide, has been identified as a rich and reliable source of such functional complexity. However, its full potential in high-speed and low-power operation has been largely unexplored. We fabricated nanoscale VO$_2$ devices embedded in a broadband test circuit to study the speed and energy limitations of their resistive switching operation. Our picosecond time-resolution, real-time resistive switching experiments and numerical simulations demonstrate that tunable low-resistance states can be set by the application of 20 ps long, <1.7 V amplitude voltage pulses at 15 ps incubation times and switching energies starting from a few femtojoule. Moreover, we demonstrate that at nanometer-scale device sizes not only the electric field induced insulator-to-metal transition but also the thermal conduction limited metal-to-insulator transition can take place at time scales of 100s of picoseconds. These orders of magnitude breakthroughs can be utilized to design high-speed and low-power dynamical circuits for a plethora of neuromorphic computing applications from pattern recognition to numerical optimization.

KEYWORDS: *vanadium dioxide, Mott transition, picosecond, femtojoule, memristor, resistive switching*
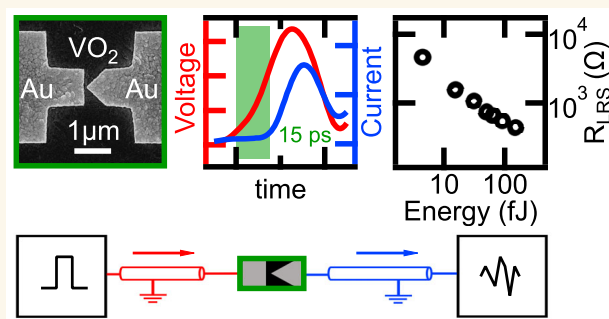
Few-component analog circuits exploiting the dynamical complexity of memristors enable increased functional complexity at a minimized footprint. Moreover, they can energy-efficiently replace extensive digital circuits designed to facilitate demanding algorithms.[1,2] Meanwhile reconfigurability, a great asset of digital platforms, has been put forward also in the analog domain by the concept of memristive field-programmable analog arrays.[3] In particular, second order dynamical complexity arising from the Mott-type insulator-to-metal transition (IMT)[4−10] in NbO$_2$ has been utilized to realize relaxation oscillators and chaotic dynamics for accelerating probabilistic optimization in transistor-less circuits.[11,12] Passively coupled VO$_2$ Mott-memristors have been used to mimic the fundamental adaptability of the biological nervous system to various input streams and even faithfully reproduce a spectrum of biorealistic neural response patterns.[13] The phase information in coupled VO$_2$ oscillator networks has been identified as a state variable and exploited in neural network operation.[14−17] The discovery of short and longer enduring metallic domains enabled subthreshold operation, short-term and long-term memory functionalities extending

the toolkit for neuromorphic data storage and processing.[18,19] The potential for high-speed and low-energy operation relying on the IMT in VO$_2$ based devices has been predicted by theoretical considerations[5] and simulations.[13] Experiments carried out in the optical and THz domain[20−26] have demonstrated that due to its predominantly electronic origin, the IMT can indeed be completed at subpicosecond time-scales. However, the more scalable electrical domain applications could so far only exploit ≥300 ps set and ≫1 ns reset switching times at ≥100 fJ energy costs.[18,19,27]

Here we demonstrate that the resistive switching response of VO$_2$ memristors to purely electrical stimuli can be as fast as 15 ps for the set transition, in agreement with finite element
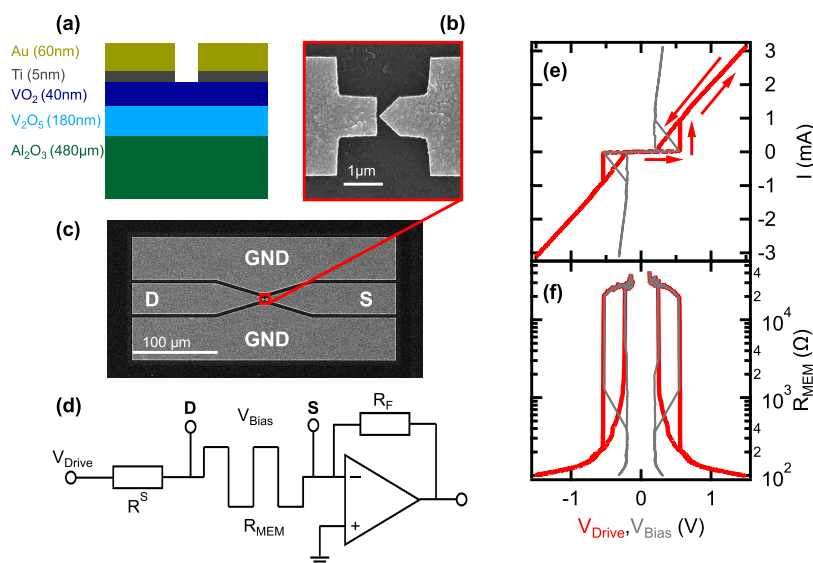
Figure 1. Device structure and DC characterization of the resistive switching. (a) Schematic (not to scale) vertical cross-section of the VO_2 memristors. (b) Magnified top-view of the planar device. The Au terminals are separated by a $\approx$ 30 nm gap at the tip of the triangular electrode. (c) Scanning electron microscope image of the coplanar waveguide (CPW) hosting the device for the high-speed resistive switching experiments (S: source, D: drain, GND: ground). The separation of the ground terminals is 4 μm. (d) The DC $I(V)$ measurement setup includes a series resistor R^S, the memristor device and a current amplifier. The V_{Drive} voltage signal is sourced from a data acquisition card whereas the V_{Bias} voltage drop on the memristor is calculated as $V_{Bias} = V_{Drive} - I \cdot R^S$. (e-f) Low-frequency ($f_{Drive}$ = 1 Hz) $I(V)$ traces and the calculated resistance, respectively, as a function of V_{Drive} (red) and V_{Bias} (gray). R^S = 380 Ω. The red arrows indicate the direction of the hysteresis.

simulations based on a two-dimensional resistor network model. The evaluation of the current acquired during the applied 20 ps long voltage pulses reveals that the IMT is triggered by the injection of as little Joule heat as a few femtojoule. Furthermore, a dedicated V-shaped electrode arrangement is utilized to focus the electric field and, thus, the device operation to a nanometer-scale active volume. Consequently, the thermal relaxation time to the insulating state of VO_2 can be greatly reduced to the 100 ps time-scale, enabling low-power dynamical memristor circuits for ultrafast neuromorphic computing applications.

RESULTS AND DISCUSSION

Our report is organized as follows. First, the device structure and the DC characterization of the resistive switching cycles are presented. Next, the transmission spectroscopy of subnanosecond voltage pulses is explained. Using this method, we demonstrate the analog tunability of the volatile low resistance states, set switching times down to 15 ps and switching energies in the femtojoule regime. We show that these results can be quantitatively understood in terms of a two-dimensional resistor network of nanometer-scale VO_2 domains, where the resistance of each domain is determined by the local temperature and electric field. Finally, we use a pump−probe scheme utilizing 20 ps long voltage pulses to monitor the complete recovery of the high resistance state in the subnanosecond time-domain.

Device Structure and DC Characterization. The individual layer thicknesses of the sample are labeled in the schematic vertical cross-section in Figure 1a. The magnified top view of the planar device is exhibited in Figure 1b. The two, asymmetrically shaped Au electrodes were evaporated on the top of a VO_2/V_2O_5 film, which was created by the thermal oxidation of a V layer evaporated on top of a sapphire substrate.[10,28] The planar gap between the two electrodes was

around 30 nm. The latter, together with the flat (triangular) shape of the source (drain) electrode, facilitate low-voltage resistive switching in a single, nanometer-scale volume of the underlying VO_2 layer. Further details on sample fabrication and characterization are provided in the Methods and Experimental Section and in ref 10. Figure 1c shows the electrode layout of the devices. The source (S), drain (D) and the two ground (GND) electrodes made of 50 nm thick Au form a coplanar waveguide (CPW). The CPW ensures the suitable termination of the two-terminal $Au/VO_2/Au$ devices for the short-duration voltage pulses of the high-speed resistive switching experiments.

The DC characterization of the current−voltage $[I(V)]$ traces were carried out in a setup consisting of a series resistor, the memristor device, a current amplifier and a data acquisition card which was also utilized as a programmable voltage source, as illustrated in Figure 1d and explained in detail in the Methods and Experimental Section. In our nomenclature the V_{Drive} voltage is applied on the device and the current limiting series resistor R^S whereas the voltage drop on the memristor device only is denoted as V_{Bias}. Positive voltage corresponds to higher potential on the drain electrode.

A representative, hysteretic $I(V)$ trace exhibiting unipolar, volatile resistive switching is shown in Figure 1e both as a function of V_{Drive} (red) and V_{Bias} (gray). The resistance, calculated as V_{Bias}/I is plotted in Figure 1f. Resistive switching reproducibly occurs between typical high resistance states (HRS) of $R_{HRS} \approx$ 30 kΩ and tunable low resistance states (LRS) in the $10^2 - 10^3$ regime at set (reset) voltages around 550 mV (250 mV). The actual R_{LRS} value can be fine-tuned by the choice of R^S and the power of the driving voltage signal. The reproducibility and endurance of the resistive switching cycles benefit from the well-defined, few 10 nm scale, presumably single-domain volume of the IMT.[10]

Picosecond Time-Scale Set Switching. The speed limit and energy consumption of resistive switching in VO$_2$ memristors was investigated by the real-time monitoring of the devices' resistive response to voltage pulses as short as 20 ps full width at half-maximum (fwhm). Resistive switching taking place within 20 ps due to the injection of 1−5 fJ energy was demonstrated. The corresponding experimental setup is shown in Figure 2c and described in the Methods and

Figure 2. Experimental demonstration of picosecond time-scale resistive switching. (a) Incoming voltage signal V_{In} (left axis, red) consisting of a 2 ns long, low-voltage read-out offset and a higher amplitude, 20 ps fwhm set voltage pulse. The corresponding transmitted voltage V_{Trans} evidence that resistive switching takes place during the set voltage pulse, as shown in blue (right axis). Note the different scales of the vertical axes. The inset magnifies the shaded regime at the onset of the read-out pulse. The negligible capacitive response during the 20 ps rise time of the V_{In} step demonstrates the low, ≈ 2 fF parasitic capacitance of the memristor sample, in agreement with simulations (green), and indicates the dominantly resistive nature of the switching in the investigated resistance regime. (b) The time dependence of the device resistance is calculated from the V_{In} and V_{Trans} traces shown in (a), according to eq 1. (c) The schematics of the high-speed setup. The V_{In} amplified voltage pulses are sourced from an arbitrary waveform generator (AWG). The V_{Trans} transmitted voltage is measured by a digital storage oscilloscope (DSO). The DSO is triggered by the second, nonamplified output channel of the AWG. (d) The equivalent circuit of the memristor device. Z_{MEM} consists of a series resistance R_S taking the lead and probe contact resistances into account, the device resistance R_{MEM} and the parasitic device capacitance C_{MEM}.

Experimental Section. The measurement technique and the data analysis followed the procedures explained in great detail in ref 29. In short, when the memristor device is exposed to fast voltage signals whose wavelength falls below the length of the utilized transmission lines, partial reflection and transmission of the V_{In} incoming voltage signal occurs due to the impedance mismatch between the Z_{MEM} device impedance and the $Z_0 = 50$ Ω wave impedance of the transmission lines. According to the solution of the telegraph equations applied to our experimental arrangement, the voltage drop on the sample equals to 2 · V_{Refl} whereas the current equals to V_{Trans}/Z_0, where V_{Refl} and V_{Trans} are the amplitudes of the reflected and transmitted harmonic waves, respectively. The impedance of the memristor can be determined through the formula

$$\frac{V_{Trans}}{V_{In}} = \frac{2Z_0}{Z_{MEM} + 2Z_0} \tag{1}$$

where, in general, harmonic V_{In} signals and a frequency dependent, complex-valued Z_{MEM} are assumed. When the memristor impedance is dominated by a frequency independent, real-valued resistive term, $Z_{MEM} \approx R_{MEM}$, eq 1 directly applies and V_{Trans} is proportional to any time dependent V_{In} signal. When a complex-valued, frequency dependent $Z_{MEM}(f)$ is concerned, the numerical deduction of the device impedance requires a model assumption on $Z_{MEM}(f)$ and a Fourier analysis based on eq 1.

A simplistic equivalent circuit accounting for the R_S lead resistance and C_{MEM} parasitic capacitance of the memristor is shown in Figure 2d. While the former contribution is usually negligible compared to the R_{MEM} device resistance, and merely plays a role in the capacitive response time through the R_S · C_{MEM} product, the frequency dependent capacitive impedance contribution arising from C_{MEM} may have a profound impact on the real time response during the applied V_{In} voltage pulses.

Figure 2a shows the measured V_{Trans} response (blue, right axis) to a V_{In} pulse sequence (red, left axis). The latter consists of a 1 ns long, low-amplitude read-out pulse, a 20 ps fwhm, 1.3 V amplitude set pulse and a second read-out pulse identical to the first one. The relative timing of V_{In} and V_{trans} are compensated for the propagation time differences in the transmission lines according to the procedures outlined in ref 29. During the first read-out pulse the device resides in its HRS and V_{Trans} stays low, consistently with eq 1 and $R_{HRS} \approx 30$ kΩ. It is important to note the absence of a dominant capacitive peak in V_{Trans} during the 20 ps rise time of the first read-out pulse, exhibited in the magnified view of the inset in Figure 2a. This observation evidence the negligible capacitive impedance of the device even in the HRS and indicates the purely resistive nature of the impedance switching. A quantitative analysis using LTspice shows a good agreement between the modeled (green) and measured (blue) V_{Trans} signal in the voltage step region by assuming $C_{MEM} = 2$ fF. In contrast, a higher C_{MEM} value would give rise to a dominant peak in response to the rising edge of V_{In}, which is definitely not the case here.

Resistive switching due to the 20 ps fwhm set voltage pulse is demonstrated by the sharp increase of V_{Trans} during the set pulse and the persistence of an increased transmission during the second, 1 ns long read-out period. In the absence of a prevailing capacitive contribution, e.g., during the constant voltage read-out periods, the device's resistive impedance can be well approximated from the V_{Trans}/V_{In} ratio based on eq 1, as shown in Figure 2b. Note, however, that the apparent rate of the such deduced resistance change within duration of the set pulse is instrumentally limited within the set pulse duration by the ≈60 GHz analog bandwidth of the detection setup. Additionally, within the duration of a short V_{In} pulse the frequency dependent capacitive contribution to Z_{MEM} can no longer be neglected which further limits the validity of the quantitative analysis on $R_{MEM}(t)$ in this time window.[29]

Next, we investigate the set switching dynamics in more detail by applying 20 ps fwhm set voltage pulses of different amplitudes and evaluating the resulting resistance change, switching times and switching energies. The applied V_{In} pulse sequence is schematically illustrated in Figure 3a. In essence, a similar pattern is utilized as discussed in the demonstrator experiment shown in Figure 2, only this time the first, 1 ns long and 0.25 V amplitude read-out pulse is shifted 100 ns away
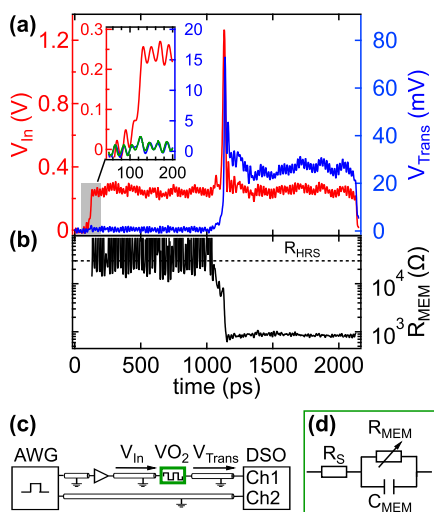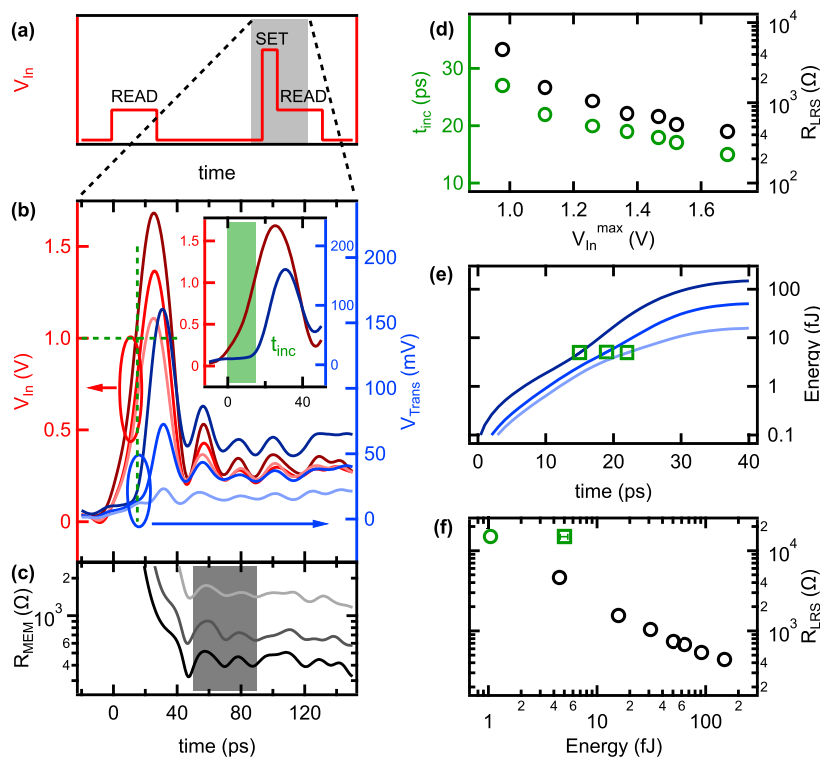
Figure 3. Analysis of the set switching. (a) Schematic illustration of the applied voltage pulse sequence. The first read pulse of 1 ns duration and 0.25 V amplitude is used to confirm the initial HRS. 100 ns later a 20 ps fwhm programming pulse of varying amplitude is applied which is directly followed by another 1 ns long, 0.25 V amplitude read pulse. Three V_{In} and V_{Trans} traces recorded in the shaded area are displayed in (b) in red (left axis) and blue colors (right axis), respectively. The horizontal green dashed line denotes $V_{In} = 1$ V whereas the corresponding vertical green dashed line highlights the onset of the switching due to the $V_{In}^{max} = 1.7$ V pulse. The inset shows the magnified view of the highest amplitude traces of the main panel. The green shaded area illustrates the definition of the t_{inc} incubation time (see text for details). (c) Time dependent resistance calculated from the data presented in (b). The gray shaded area highlights the time window where averaging was applied to evaluate R_{LRS} after the completion of the set pulse. (d) Deduced t_{inc} (green, left axis) and R_{LRS} (black, right axis) as a function of the V_{In}^{max} amplitude of the applied voltage pulses. The vertical error-bars are smaller than the corresponding symbol sizes. (e) The solid lines show the set pulse energy calculated from the time dependent voltage and current for the three traces presented in (b). The green symbols mark the corresponding incubation times. (f) R_{LRS} as a function of the set pulse energy (black dots). The green square and its horizontal error bar correspond to the average and standard deviation of the energy integrals calculated until t_{inc}, as shown in (e). The green circle is an estimated extrapolation of the energy dependence to $R_{LRS} = 15$ kΩ.

from the set pulse. As this time separation is much longer than the zero-bias relaxation time from the LRS to the HRS, a possible preconditioning of the set switching by the first read-out pulse can be unambiguously excluded.

Figure 3b exemplifies the V_{Trans} response (blue colors, right axis) to 20 ps fwhm V_{In} pulses (red colors, left axis) of three different V_{In}^{max} amplitudes. The corresponding, time dependent resistance traces assessed from the V_{In}/V_{Trans} ratio according to eq 1 are shown in Figure 3c. For further evaluation, the R_{LRS} values are deduced by averaging over the 40 ps long, gray shaded time window directly following the falling edge of the set pulse in Figure 3c. The length and the position of this time-interval is over an order of magnitude below the zero-bias thermal relaxation time. Therefore, the role of the second read pulse in maintaining the LRS is negligible in this regime and the existence of the LRS is solely attributed to the effect of the preceding set pulse. The fine analog tunability of the LRS is demonstrated in Figure 3d where a 60% increase in V_{In}^{max} results in the gradual, 1 order of magnitude decrease of R_{LRS} in the $10^2 - 10^3$ Ω regime (black dots, right axis). This behavior is consistent with the set pulse energy dependent volume of the metal–insulator transition (MIT), as will be discussed later in the framework of our set switching model.

In addition to the decreasing tendency in R_{LRS}, an apparent acceleration of the set transition is also observed at higher V_{In}^{max}. We characterize the speed of the set process by the t_{inc} incubation time which is experimentally defined here as the time interval between the 10% onset of V_{In}^{max} and reaching 15 kΩ ≈ $R_{HRS}/2$, as illustrated by the green shaded area in the inset of Figure 3b. The incubation time as a function of the applied V_{In}^{max} setting is shown in Figure 3d by the green dots (left axis). Although the Mott type IMT in VO_2 is identified to have a dominant electronic origin and, thus, can be triggered even by femtosecond laser excitation,[20] previous experiments utilizing voltage pulses have reported incubation times down to 100s of picoseconds.[19] In contrast, we demonstrate incubation times down to 15 ps. Note that the voltage pulse amplitude dependence does not show any saturation at this value, therefore t_{inc} values in the single digit picosecond regime are highly conceivable. However, the applied V_{In}^{max} pulse amplitudes were restricted to ≤1.7 V in order to protect the devices from destruction.

The data presented in Figure 3b also reveals the threshold switching nature of the set transition: the lower t_{inc} values deduced at higher V_{In}^{max} settings correspond to the same actual $V_{In} ≈ 1$ V voltage levels, as highlighted by the green dashed lines. The observed apparent V_{In}^{max} dependence of t_{inc} in Figure
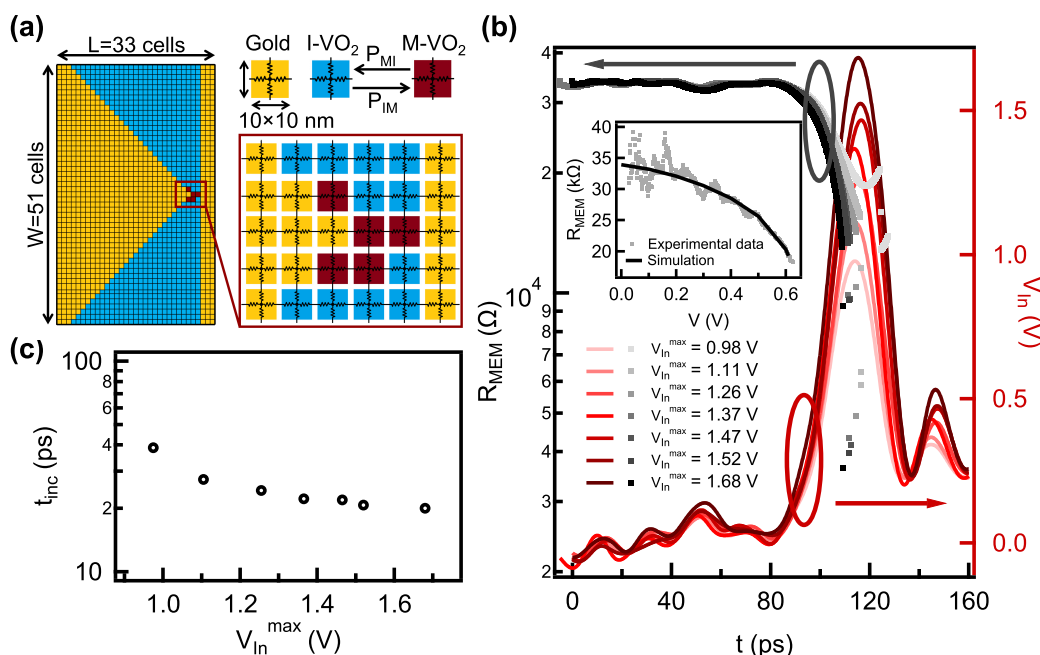
Figure 4. Two-dimensional resistor network simulation of the set switching time. (a) Illustration of the two-dimensional resistor network model applied for the experimentally realized electrode arrangement. The 40 nm thick VO_2 layer is in thermal contact with an electrically perfectly insulating substrate that is at T_0 = 300 K. The yellow, blue and red squares represent low-resistivity Au, insulating phase VO_2 and metallic phase VO_2 domains, respectively. The dynamics of the transition between the latter two phases is determined by the transition probabilities P_{IM} and P_{MI}. The width (length) of the simulated area is W = 51 (L = 33) cells. The gap between the electrodes at the narrowest spot is 2 cell wide. The resistance network connecting the nearest neighbor domains are also indicated. (b) Experimental V_{In} voltage pulses of 20 ps fwhm (red colors, right axis) and the corresponding, time-dependent calculated resistance traces (gray colors, left axis). The inset shows the $R(V)$ dependence in the HRS acquired in a DC measurement (gray dots) and its numerical fitting (black curve) which were used to extract the actual values of the thermal parameters of the model (see text). (c) Incubation times as a function of the V_{In}^{max} set voltage pulse amplitudes, as deduced from the simulated data shown in (b).

3d is quantitatively accounted for by the instrumental aspects of our pulse firing setup, where the rise time of the V_{In} voltage pulse is always 20 ps, independently of the pulse amplitude. Consequently, the same threshold voltage is established faster when a higher amplitude pulse is applied. Such a threshold switching behavior is in agreement with the models which attribute a purely electronic[4] or a mixed electronic and thermal origin[10] to the IMT in VO_2. In contrast, ionic migration driven resistive switching compounds exhibit exponentially decreasing incubation times at linearly increasing voltage levels, known as the voltage−time dilemma.[30−32] Based on the above arguments, we argue that an independent control on t_{inc} and R_{LRS} shall be possible in VO_2 devices, as the former is merely governed by the rise time of the V_{In} set pulse while the latter is determined by its amplitude and duration, i.e., the total set pulse energy, as demonstrated by the black circles in Figure 3d. Note, however, that ≤20 ps rise times at Volt-scale signal levels are facing the limitations of current state of the art electronics.

The set switching energies required to reach a specific R_{LRS} were calculated by numerically integrating the product of the 2 · V_{Refl} voltage drop on the sample and the V_{Trans}/Z_0 current as a function of time, as shown by the solid lines in Figure 3e for the three example time traces of Figure 3b. The corresponding incubation times are marked by the green squares. They highlight that the set transition is ignited after the injection of ≈5 fJ energy, independently of the specific shape of the set pulse, underpinning the role of local heating in the IMT. The Joule heating contribution is estimated to be ≈1 fJ, by taking the capacitive charging energy of $C \cdot U^2/2 \approx 4$ fJ into account, where $U \approx 2 \cdot V_{In}(t_{inc}) = 2$ V and $C = 2$ fF.

The LRS resistance values deduced from the 40 ps long time interval directly following the falling edges of the different amplitude set pulses are plotted against the total energy deposited in the device by the black circles in Figure 3f. As a reference, the average and standard deviation of the total energies calculated at t_{inc} for the three example traces of Figure 3e are also displayed in Figure 3f by the green square and its error bar, respectively. According to our definition of t_{inc}, the corresponding resistance value is 15 kΩ. Note that the energy values of the black circles naturally exclude most of the capacitive charging energy, as they involve the time integral over the entire duration of the corresponding set pulses where the contributions of charging and discharging mostly cancel out. Therefore, these energy values can be directly attributed to the Joule heating contribution. The green circle extrapolates the tendency drawn by the black symbols to R_{LRS} = 15 kΩ as an estimate of the set switching energy limitations for an ideally parasitic capacitance-free device design. In contrast, the energy value of the green square was determined at the onset of the set pulses, where the ≈4 fJ penalty of capacitive charging is not yet counteracted with the subsequent discharging. In comparison to the state of the art switching energies of 400 fJ in silicon CMOS neurons,[33] ~50 fJ in electrochemical metalization cells[34] and ~100 fJ in valence change oxide memories[29,35,36] as well as in micrometer-scale VO_2 samples,[19] this evaluation demonstrates the merits of nanoscale VO_2 devices in high-frequency electronics reaching single-digit femtojoule switching energies at kΩ range LRSs. The latter regime quantitatively corresponds to the extreme energy

efficiency of the human brain, where the energy cost of a neural spike is estimated to be 5−100 fJ.[13,37]

Modeling the Set Switching Dynamics. The plausibility of the set switching due to Volt-scale pulses of 20 ps fwhm within our thermally and electrically driven Mott transition picture[10] was confirmed by numerical simulations. The applied two-dimensional resistor network model[38,39] takes into account the electrical and thermal conductivities of the VO_2 layer confined by the Au electrodes. The active region is modeled as an array of 10×10 nm^2 cells arranged in a square lattice, as illustrated in Figure 4a. The state of each VO_2 cell is either insulating (I-VO_2, blue) or metallic (M-VO_2, red) whereas the Au cells (yellow) are always in a low-resistance metallic state. The thickness of the cells is 40 nm according to the VO_2 film thickness of our samples. Each cell consists of four identical resistors connecting to its nearest neighbors. All VO_2 cells are initialized as I-VO_2.

In our model, the phase transition of the VO_2 cells is a thermally assisted process, where the $P_{IM}(T)$ and $P_{MI}(T)$ insulator-to-metal and metal-to-insulator transition probabilities depend exponentially on the temperature. The local temperature is determined from the heat equation accounting for Joule heating and heat conduction toward the neighboring cells and the substrate. Furthermore, a boundary thermal resistance was considered between the VO_2 and Au cells. The resistance of an individual resistor in an I-VO_2 cell depends on both the local temperature and the local electric field, whereas in the metallic state of VO_2 a temperature and electric field independent resistance is assumed. The electrical and thermal material parameter values utilized by the resistor network simulation are adopted from our previous finite element simulations performed in COMSOL Multiphysics.[10] They were determined by fitting the experimental $R(V)$ trace of the device by the simulation, as shown in the inset of Figure 4b. Further details on the numerical approach are provided in the Methods and Experimental Section as well as in ref 10.

In order to extract the incubations times according to the definition used throughout the evaluation of the measured set switching data, the experimentally realized set voltage pulses were applied to the resistor network, as shown by the red curves in Figure 4b. The model was solved by using 0.1 ps long time steps. The gray curves in Figure 4b show the time evolution of device resistance. The phase transition is hallmarked by the sudden drop of the resistance which occurs during the rise time of the set pulses, in agreement with the experiment. The simulated incubation times are exhibited in Figure 4c. In spite of the crude simplifications of the applied model, they fall into the 20−40 ps regime, in good agreement with the experimentally observed values of 15 ps < t_{inc} < 30 ps. The simulated incubation time also reveals a similar voltage dependence as its experimental counterpart, demonstrating the consistence of the measured, picosecond-scale incubation times with the electro-thermal picture of the Mott transition in VO_2 nanodevices. These findings are also in agreement with the Spice simulation results of W. Yi et al.,[13] where picosecond time-scale set transitions are predicted at femtojoule switching energies for active volumes comparable to our device design.

The simulations also facilitate a qualitative understanding of the sample fabrication aspects of the voltage range and incubation time scale of the IMT. Concerning substrate effects, the simultaneous presence of the V_2O_5 and VO_2 layers is an inherent result of the thermal oxidation process of V and cannot be completely avoided. However, the thick V_2O_5 layer

beneath the VO_2 film enhances the thermal isolation of the device from the sapphire substrate, since the thermal conductivity of V_2O_5 is more than an order of magnitude lower than the one of sapphire. Consequently, electrical switching can be induced at lower voltage levels compared to a configuration where the VO_2 layer is directly on the sapphire substrate. Decreasing the gap size beyond the 30 nm limit of our fabrication technology is expected to influence the measured incubation time via proportionally decreasing both the switching threshold voltage and the low-voltage resistance of the insulating phase. As a result, the critical amount of Joule heat for the IMT will be induced at a lower and, thus, faster achievable voltage level.

Sub-Nanosecond Reset Dynamics. Finally, we demonstrate that the HRS can be restored within 600 ps from the set voltage pulse. For this purpose, the pulsing scheme shown in Figure 3a is modified by replacing the second, 1 ns long read-out pulse promptly following the set pulse by a 20 ps long, 0.2 V amplitude probe pulse. The latter is delayed by t_{delay} with respect to the set pulse, as illustrated in Figure 5a. The concept of the short probe pulse is introduced in order to minimize the
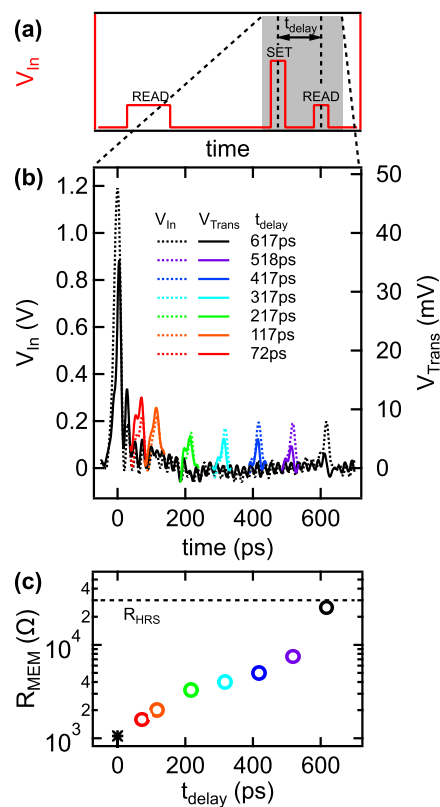

Figure 5. Analysis of the retention. (a) Schematic illustration of the applied voltage pulse sequence. Verification of the HRS and triggering the set transition are carried out identically to the scheme exhibited in Figure 3. In contrast, the second, 0.2 V amplitude read-out voltage pulse is only 20 ps long and is delayed with respect to the 20 ps long, 1.2 V amplitude programming pulse by a varying t_{delay}. (b) V_{In} (dashed lines, left axis) and V_{Trans} data (solid lines, right axis) corresponding to the shaded area in (a) at different t_{delay} times, as labeled in the figure. Note that only the second read-out pulse and its response are shown in color for better visibility. (c) Resistance as a function of the delay time, as deduced from the data shown in (b). The initial HRS resistance, indicated by the horizontal dashed line, is recovered within 600 ps.

impact of the readout pulse in maintaining the LRS. The initial $R_{HRS} \approx 30$ kΩ state is confirmed by a 1 ns long, 0.25 V amplitude read-out pulse applied 100 ns before the set pulse. The 20 ps long, 1.2 V amplitude set pulse, displayed by the black dashed line at 0 ps in Figure 5b, switches the device into an $R_{LRS} \approx 1$ kΩ state within the duration of the pulse, consistently with the data exhibited in Figure 3. In the experiment shown in Figure 5b, identical set pulses and different t_{delay} times between 0 and 600 ps were utilized, as plotted by the colored V_{In} (dashed lines) and V_{Trans} (solid lines) traces. The actual device resistance is evaluated at each t_{delay} by fitting the V_{Trans} response to the probe pulse according to eq 1 and the Z_{MEM} equivalent circuit shown in Figure 2d. This analysis reveals the decay of the LRS toward the HRS and evidence that the $R_{HRS} = 30$ kΩ state can be restored within 600 ps, as presented in Figure 5c. Note, however, that this finding does not exclude further, subtle relaxation of remnant metallic volumes, as observed by J. del Valle et al.,[18] as well as M. Nikoo et al.[19]

Previous studies utilizing micron-scale VO$_2$ devices concluded that the MIT is a predominantly thermal relaxation driven, slow process taking place at 10s or even 100s of nanoseconds,[18] where the presence of long-lived metallic domains was also evidenced.[19] In contrast, our analysis unambiguously demonstrates that the relaxation to the HRS can take place at the subnanosecond time-scale in nanoscale VO$_2$ cells, as shown in Figure 5c. We emphasize that the small device volume, granted by our special electrode arrangement, is a crucial ingredient to the improved heat transfer toward the environment which is a prerequisite to fast thermal relaxation. This finding, together with the sub-100 ps IMT enables the orders of magnitude acceleration of VO$_2$-based electronics, among them THz sensors[40] and oscillator circuits exploited for neuromorphic computing purposes.[16]

CONCLUSION

In conclusion, we monitored the resistive switching dynamics in nanoscale volumes of VO$_2$ thin films in real time at the picosecond time-scale, enabled by a special, low-capacitance and scalable electrode design. By utilizing current state of the art electronics, we demonstrated that 20 ps fwhm voltage pulses of ≤1.7 V amplitude trigger the insulator-to-metal transition with incubation times down to 15 ps, resulting in fine-tunable, analog LRS in the resistance range of $10^2 - 10^4$ Ω. These findings are supported by finite element simulations taking the combined electronic and thermal origin of the IMT into account. Our analysis of the energy consumption revealed that, depending on the targeted R_{LRS} level, the set switching requires as little energy as ≈4 fJ. By applying a pump–probe pulsing scheme we demonstrated that the HRS can be restored within 600 ps.

The picosecond-scale operation rate enables memristive technologies to set foot in the communication industries where low-power solutions become increasingly crucial at ever-rising information carrier frequencies. Furthermore, the femtojoule set switching energies not only surpass the state of the art among solid-state memristors but also comply with the extreme low-power operation of the human brain. Thus, brain-inspired spiking neural network operation at an 8 orders of magnitude faster pace compared to biological computation becomes reality. Thereby the demonstrated, orders of magnitude breakthroughs in speed and energy underline the

merits of nanoscale Mott devices in diverse electronic platforms of the Beyond-Moore Era.

METHODS AND EXPERIMENTAL SECTION

Device Fabrication. The VO$_2$ layers were formed via the postdeposition heat treatment of an Al$_2$O$_3$/V vertical stack of 480 μm Al$_2$O$_3$ and 100 nm V. During the heat treatment, the sample was exposed to 400 °C temperature and 0.1 mbar air pressure over 4.5 h. As a result, a 40 nm thick VO$_2$ film was created on top of a 180 nm thick V$_2$O$_5$ bottom layer, as confirmed by cross-sectional TEM and EELS analyses.[10] The metallic leads of 10 nm Ti and 50 nm Au were patterned by standard electron-beam lithography and deposited by electron-beam evaporation at 10^{-7} mbar base pressure at rates of 0.1 and 0.4 nm/s, respectively, followed by lift-off. After the completion of the CPW structure shown in Figure 1c, a selective etching step was carried out to remove the VO$_2$ layer in the gap regions of the GND-S and GND-D electrodes of the CPW. During this step the sample was immersed to an acidic solution of H$_2$O$_2$:H$_3$PO$_4$:CH$_3$COOH:HNO$_3$ (2:16:1:1) at 50 °C for twice 5 s. This method yielded to ∼10 MΩ parasitic resistances between the GND-S and GND-D electrodes of the CPW.

Direct Current (DC) Characterization. The schematic of the DC $I(V)$ measurement is shown in Figure 1d. A slow, typically $f_{Drive} =$ 1 Hz frequency, triangular voltage signal was applied to the device under test and the series resistor of $R^S = 0.3-1$ kΩ by an NI USB-6341 data acquisition unit (DAQ). The current was measured by a Femto DHPCA-100 current amplifier and recorded at the analog voltage input of the DAQ. The V_{Bias} voltage acting on the device was determined as $V_{Bias} = V_{Drive} - I \cdot R^S$.

Fast Switching Setup. The schematics of the fast resistive switching setup is shown in Figure 2c. The device under test was contacted by two 67 GHz bandwidth Picoprobe triple probes in a vibration-damped probe station. A Micram DAC10004 100GSa/s DAC unit served as an arbitrary waveform generator (AWG) which provided voltage pulses down to 20 ps fwhm at 20 ps rise time. The output of the AWG was amplified by a Centellax UA0L65VM broadband amplifier module owing a 65 GHz analog bandwidth. The voltage pulses propagated in 0.30 m long, 70 GHz bandwidth, 50 Ω terminated Totoku TCF280 coaxial cables. The V_{Trans} transmitted voltage was recorded by a 50 Ω terminated Keysight UXR1104A digital storage oscilloscope (DSO) at 256 GSa/s sampling rate and 113 GHz analog bandwidth. The input terminals of the DSO were protected by 60 GHz bandwidth RF attenuators. The V_{In} signal was acquired separately by eliminating the memristor device and the probes from the circuit.

Two-Dimensional Resistor Network Simulations. The $R_I^{i,j}$ resistance of an individual resistor in the I-VO$_2$ cell, indexed by (i, j), depends on the $T_{i,j}$ local temperature and $E_{i,j}$ electric field and can be written as

$$R_I^{i,j} = R_0 e^{-E_g/2k_B T_{i,j}} e^{E_{i,j}/E_c} \qquad (2)$$

where R_0 is a constant, E_g is the band gap energy in the HRS state and E_c is a characteristic electric field. In the LRS a temperature and electric field independent resistance value R_M^{ij} is assumed. By biasing the resistor network, the current starts to flow through the cells and the Joule heat dissipates on each resistor according $P_{i,j} = I_{i,j}^2 R_I^{i,j}$. The corresponding $dT_{i,j}$ temperature change depends on the Joule heating as well as on the heat conduction toward the nearest neighbor cells and the substrate according to

$$\frac{dT_{i,j}}{dt} = \frac{P_{i,j}}{C_{i,j}} - \frac{\kappa_{i,j}}{C_{i,j}} \sum_{k,l}^{NN} (T_{i,j} - T_{k,l}) - \frac{\kappa_{subs}}{C_{i,j}}(T_{i,j} - T_0) \qquad (3)$$

where $C_{i,j}$ is the thermal capacity of the cell, $\kappa_{i,j}$ (κ_{subs}) is the thermal conductance toward the neighbor cells (substrate). The substrate is assumed to be at a T_0 base temperature. Furthermore, a boundary thermal resistance was considered between the VO$_2$ and Au cells which determines the κ_{int} thermal conductance at their interface. At each time step of the simulation, the resistance of the resistor network

is calculated and the electrical potential map of the resistor network is determined by a nodal analysis. Finally, $T_{i,j}$ is calculated via eq 3 and the state of each VO_2 cell is updated.

The phase of a VO_2 cell can change between metallic and insulating states, according to the transition probabilities given by P_{IM} and P_{MI}. These transitions are thermally activated with the transition rates of

$$P_{IM} = \nu e^{-E_{IM}(T)/k_B T} \tag{4}$$

$$P_{MI} = \nu e^{-E_{MI}(T)/k_B T} \tag{5}$$

where the ν is an attempt rate set to unity. The potential barriers $E_{IM}(T)$ and $E_{MI}(T)$ separate the metal and insulator states. Both energy barriers have a linear temperature dependence, which vanishes at the phase transition temperature $T_{c,heat}$ and $T_{c,cool}$, respectively, as

$$E_{IM}(T) = \begin{cases} \epsilon_{IM}(T_{c,heat} - T), & \text{if } T < T_{c,heat} \\ 0, & \text{if } T \geq T_{c,heat} \end{cases} \tag{6}$$

$$E_{MI}(T) = \begin{cases} \epsilon_{MI}(T - T_{c,cool}), & \text{if } T > T_{c,cool} \\ 0, & \text{if } T \leq T_{c,cool} \end{cases} \tag{7}$$

where ϵ_{IM} and ϵ_{MI} are constants. The electrical parameters R_0 and E_c were deduced from the measured low-bias $R(V)$ dependence. The thermal parameters κ_{VO2}, κ_{subs} and κ_{int} were determined by fitting the high-bias $R(V)$ trace in the insulating phase.

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Author Contributions

T.N.T. and L.P. fabricated the devices. The VO_2 layers were grown by G.M. M.C. and Y.H. developed the fast resistive switching setup. S.W.S. and M.C. acquired and analyzed the resistive switching data. B.S. and Z.P. contributed to the lower frequency characterization of the samples. L.P. developed the two-dimensional resistor network model and performed the numerical simulations. A.H. and M.C. conceived the idea of fast resistive switching experiments and supervised the project. The manuscript was prepared by M.C., S.W.S, L.P., and A.H. All authors contributed to the discussion of the results.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

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