Charge transport in polymeric field-effect devices

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Scope and outline

In the last years organic semiconductor based devices have made the step from the laboratory to the market in mobile telephones displays or RF-ID tags, becoming more and more present in everyday life devices. The organic semiconductors can be separated in two classes - small molecules and polymers. From a device point of view the difference between the two classes arises from the way the devices are built: the small molecules have to be evaporated as they are usually insoluble while the polymers are processed from solution. What makes the semiconducting polymers attractive for applications is the ease of processability, meaning low costs and the possibility to build complex electronic devices on flexible substrates, which would lead to smaller, more compact and durable devices. The range of applications is still quite limited as the semiconducting polymers are usually sensitive to the ambient factors - oxygen humidity, UV-radiation. For this reason a lot of research has been done in order to find the right materials for encapsulation and protection against radiation. This is not a trivial task as the protective layers should not interfere in any way with the functionality of the device by chemical reactions or degradation in time. Nonetheless materials satisfying these requirements have been found and organic devices are reaching the market, as already mentioned, in the RF-ID tags but also in the displays area.
The scope of this thesis is to investigate the influence of preparation on the electrical properties of poly(3-hexyl)thiophene in different devices (field-effect transistors, metal-insulator-semiconductor diodes and hole-only diodes). Firstly the influence of various organic and inorganic insulators is analyzed. Another important issue is the modification of the silicon oxide surface energy through self-assembled monolayers, thus promoting a better self-organization of the P3HT molecules during the film formation. The last but not the least important process which leads to an improvement of the electrical characteristics of FETs and MIS diodes is the post spin-coating annealing. At the same time special attention will be given to the influence of external parameters as temperature, light and environment upon the operation of these devices. A comparison of our data with existing models describing the charge transport will be attempted in the end.

Chapter 1

Theoretical Background

1.1 Charge transport in organic materials

There are two different classes of organic materials which are used in the fabrication of organic field-effect devices - the conjugated polymers and the small molecules. The preparation methods of the devices are differing from one class to the other. In order to create thin films, the polymers are usually spin-coated from solution while the small molecules are evaporated in high-vacuum. In general the structure of the polymeric thin films is amorphous while the small molecules can form highly crystalline films. In some cases due to the interaction between the polymeric chains, crystalline regions can form and thus the morphology to these films can be regarded as highly crystalline regions embedded in an amorphous matrix, as shown in figure 1.1(b). The poly(3-hexyl-thiopehene) (P3HT), see figure 1.1(a), is one of these polymers. In the crystalline regions the chains orientation is so that they are parallel to the substrate while the side hexyl chains tend to be perpendicular on it [1], [2]. The size and crystallinity of these regions depends on a number of parameters which will be analyzed in chapter 6.

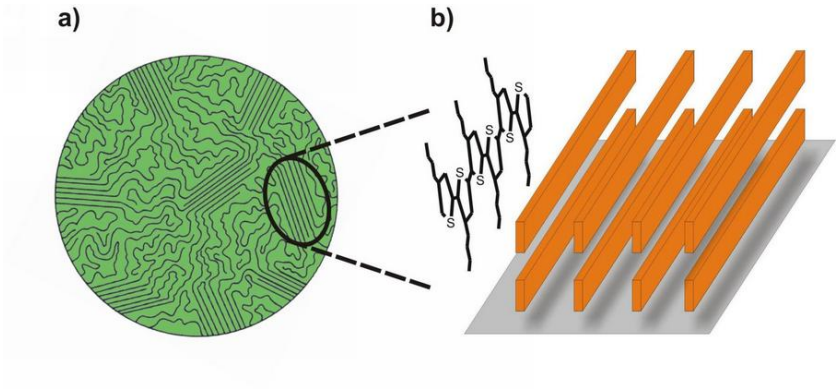

Figure 1.1: (a) Poly(3-hexyl-thiophene) chemical structure, (b) thin film morphology and (c) crystallite structure

The standard device used in measurements of the field-effect mobility of amorphous materials is the field-effect transistor (FET), whose structure is schematically presented in figure 1.2(a). In such a device the charge transport takes place between the source and the drain thus in order to obtain a good performance, the semiconductor material has to have a good conductivity in the direction parallel to the substrate. The P3HT, due to the self-organization mentioned above, is a good polymeric candidate, as in the crystalline regions the overlapping of the π orbitals is high, thus a high charge carrier mobility being promoted. Nonetheless, due the the mixed nature of the films - small crystallites in an amorphous matrix, the overall mobility of P3HT films is in the 0.01-1 cm^2/Vs, as the amorphous regions act like barriers for the charge carriers.
If one computes the charge distribution in the semiconductor material, by solving the Poisson equation, it can be noticed that this is very high near the insulator surface and decreases very fast in the bulk of the semiconductor, as it can be seen figure 1.2(b). Considering this, the semiconductor polymers which can be used to build performant devices are limitted to the ones which show good transport in the direction parallel to the substrate and at the same time form films with a low enough number of defects, so that a small number of carriers will be pinned.

In effect, in order to obtain high performance devices, one has to also modify the sub-

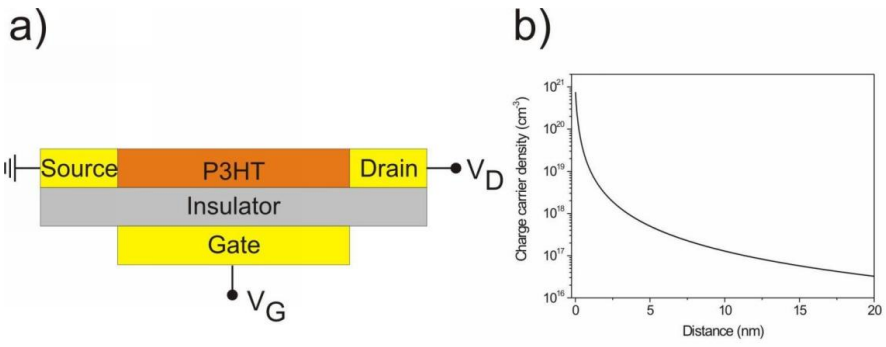

Figure 1.2: a) Stadard FET structure and b) charge density in the channel

strate's surface, by increasing its surface energy, while at the same time trying to reduce the ammount of dangling bonds, via the growth of self-assembled monolayers on SiO_2 or by choosing a proper organic insulator. The need for an increased surface energy is related to the film formation and the self-organization of the P3HT chains, as a surface with a higher energy allows them to move more and thus to form larger and better crystalline domains. At the same time a high surface energy means that there are less broken bonds which could act as trapping centers.
Apart from the transport in the direction parallel to the substrate, which is of direct interest for the fabrication of the devices mentioned in the introduction of this thesys, the one in the perpendicular direction has to be investigated too, in order to get a better insight in the morphology and electrical properties of the polymeric films. This is realized through

the use of the MIS (metal-insulator-semiconductor) structure and space charge limitted diodes. In the following the theory of all these devices - FET, MIS and SCLC diodes is reviewed and the basic equations involved in the analisys of the measurements are derived.

1.2 Metal-Insulator-Semiconductor Diode

1.2.1 Introduction

The Metal-Insulator-Semiconductor (MIS) diode is the most important device for the study of the interface between silicon and silicon oxide. It has been proposed by Moll and by Pfann and Garrett in 1959 [3] and it has been used for the first time to investigate the surface of thermally oxidized silicon by Terman [29]. The main reason for analysing the MIS diodes lays in the need to get insight into the electrical and structural properties of the bulk of the thin polymeric films. These properties and the influence of the preparation methods (see chapter 4 and ch:SmplTreat) as well as the influence of external parameters on them are very important in order to be able to fabricate stable and high performance devices.
At the same time, as nowadays the quality of the silicon oxide is very high, one can use the MIS diode to investigate the electrical properties of the interface between various organic materials and the SiO_2, making use of the extensive knowledge gained during the research on inorganic devices. As the structure of an MIS diode is much simpler than the one of a FET, as it will be detailed in the following, the metal-insulator-semiconductor can prove usefull for the sceening of semiconducting polymers. The structure of an MIS diode is a simple two terminal one, as it can be seen in figure 1.3, so one of its main advantages, as already mentioned, is the simplicity of fabrication.

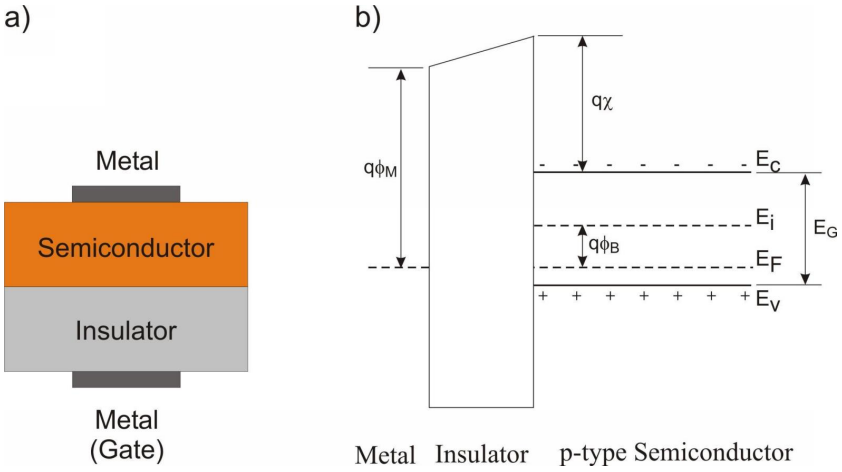

Figure 1.3: a) MIS schematic and b) energy band diagram of an MIS diode at V=0, for a p-type semiconductor

The analysis of the MIS diode can give quite accurate information about the quality of the insulator, like fixed and mobile charges, but also about the electrical properties of the semiconductor (out-off plane mobility, trap distribution). In the case of organic semiconductors and insulators this kind of analysis lets us know about the quality of the layers and allows us to predict to some extent the behavior of more complicated devices which are usually based on field effect transistors.
The quantity measured in an MIS diode is the variation of the complex impedance (admittance) with the gate bias and frequency. One can then calculate the capacitance and conductance as functions of gate bias and frequency. The gate is defined as the contact below the insulator, as by means of the applied voltage one controls the ammount of induced charge in the semiconductor layer.

1.2.2 Operation of MIS diode

Ideal inorganic MIS diode

In figure 1.3 the energy band diagrams for a p-type MIS diode, with no bias applied, are shown. It can be seen that due to the insulator a big barrier exists between the gate metal and the semiconductor, so that no free flow of carriers can take place. This way the application of a voltage on the device will create an electric field in the insulator by surface charge layers forming in the semiconductor and the metal, respectively. As the gate surface charge layer is very thin and it responds very fast to ac signal it doesn't have any influence on the total impedance of the device. The surface charge layer in the semiconductor is not thin (depends on the gate bias) and it doesn't respond instantly to the ac signal, so its variation with gate bias and frequency gives a significant contribution to the total impedance.
Depending on the sign of the gate voltage the device can be in one of the following states, as seen in figure 1.4:

1. The accumulation regime: gate voltage is negative, bands are bending upwards, the density of holes is increasing;

2. The depletion regime: gate voltage is positive, the bands are bending downwards, the density of holes is decreasing;

3. The inversion regime: at even more positive voltages the downward band bending gets larger, the intrinsic Fermi level crosses the Fermi level and the density of electrons becomes larger than the one of the holes .

As the three regimes represent the variation of the semiconductor surface charge layer, they can be explained considering the *pn* product, which should be constant everywhere in the device and that the charge neutrality should be respected in the entire device. That means if the gate voltage is negative it will attract the holes toward the semiconductor's surface leading to the formation of the *accumulation layer*.

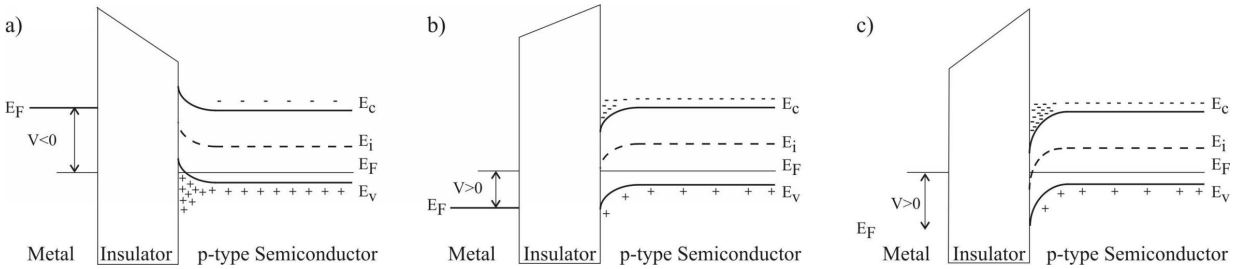

Figure 1.4: Energy band diagram for an ideal p-type MOS in: a) accumulation, b) depletion, c) inversion

As the bias is increased, more and more holes will be repelled from the surface till at a given gate bias, called *flat-band voltage*, the semiconductor will be neutral. At higher values of the applied bias even more holes will be repelled, but as the pn product should be constant the density of electrons will increase, thus a *depletion layer* being formed. The positive gate bias is compensated by the negative acceptor ions present in this layer. As the bias increases the *width of the depletion layer* increases too, to include more acceptor ions for compensation. The width of the depletion layer can extend over a few hundreds of nanometers depending on doping. At very high biases when the inversion is reached, the number of electrons near the surface is very large, being confined in a thin region - the *inversion layer*. The thickness of the inversion layer does not depend on the gate bias.
In order to have an expression for the variation of the surface charge layer with the bias, the Poisson equation has to be solved. To simplify the calculus a few conditions have to be assumed:

1. The Poisson equation will be solved in one dimension, in the direction of the field which is perpendicular to the surface. One can assume that the field is uniform as the gate is much larger than the insulator thickness.

2. Doping is uniform in the semiconductor.

3. The semiconductor is nondegenerate, meaning the applied gate bias is not extremely high.

4. The Poisson equation is solved in an approximate charge density, meaning the discrete nature of dopant ions and their spatial distribution is ignored. That means the electrons and holes can be regarded as moving in an average field and they can be treated as independent particles.

Apart from the assumptions presented above another approximation has to be made - the *band-bending approximation*. This assumes that the densities of states in the valence and conduction band are not changed by the field and that the only effect of the field is to shift the energetic levels of the band by a fixed value which is determined by the potential in each point in the semiconductor.

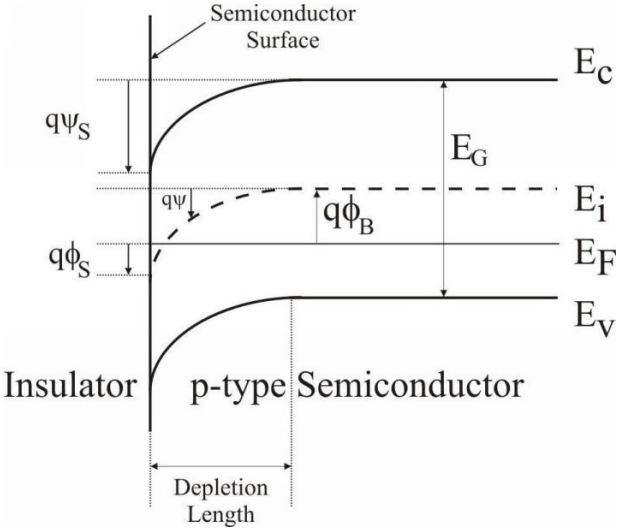

Figure 1.5: Energy band diagram for a p-type semiconductor. ψ is measured with respect to intrinsic Fermi level E_i

The expression for the density of holes, calculated along the axis perpendicular to the insulator surface and pointing toward the bulk, is given by:

$$p(x) = N_A \exp\Big[-\frac{q\psi(x)}{kT}\Big] \tag{1.1}$$

where N_A is the acceptor density, k the Boltzmann constant, T the absolute temperature, q the elementary charge and $\psi(x)$ the band bending. Figure 1.5 depicts the band bending and the quantities involved. The value of ϕ is taken with respect to the Fermi level

$$q\phi(x) = E_F - E_i(x) \tag{1.2}$$

and it is considered that if the energy levels are bent downwards. ψ is positive and if the energy levels are bent upwards then ψ is negative. When $(x \to \infty)$ $\phi(x)$ is called the bulk potential ϕ_B and when $(x \to 0)$ $\phi(x)$ is called the surface potential ϕ_S. $E_i(x)$ follows the band bending and deep in the bulk coincides with the intrinsic Fermi level.
The band bending $\psi(x)$ is defined as

$$\psi(x) = \phi(x) - \phi_B \tag{1.3}$$

If one defines the following dimensionless potentials

$$u(x) = \frac{q\phi(x)}{kT} \qquad and \qquad v(x) = \frac{q\psi(x)}{kT} \tag{1.4}$$

the electron and hole density becomes

$$n(x) = n_i \exp[u(x)] = N_D \exp[v(x)] \qquad \text{for an n-type semiconductor} \tag{1.5}$$

$$p(x) = n_i \exp[-u(x)] = N_A \exp[-v(x)] \qquad \text{for a p-type semiconductor} \tag{1.6}$$

where the donor and acceptor concentrations, respectively, are connected to the bulk potential by

$$\frac{N_D}{n_i} = \exp(u_B) \qquad \text{for a n-type semiconductor} \tag{1.7}$$

$$\frac{N_A}{n_i} = \exp(-u_B) \qquad \text{for a p-type semiconductor} \tag{1.8}$$

The minority carrier concentration can be easily calculated from $pn = n_i^2$.
In figure 1.5 the sign of ϕ_B is negative, in accumulation $\phi_S < 0$ and $\psi_S < 0$. The flat-band condition is given by $\phi_S = \phi_B$ and $\psi_S = 0$; when $\psi_S = -\phi_B$, meaning the extrinsic level touches the intrinsic level. The device is found in inversion when $\psi_S \geq -2\phi_B$.

The Poisson Equation

With the assumptions presented above and the band bending approximation, the Poisson equation can be solved for the one dimensional case, as the quantities involved vary only in the perpendicular direction to the interface. The surface potential is the solution of the following Poisson equation:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_S} \tag{1.9}$$

where $\rho(x)$ is the charge density being the sum of mobile holes and electrons, immobile ionized donors and acceptors and ϵ_S is the dielectric permittivity of the semiconductor.

$$\rho(x) = q[p(x) - n(x) + N_D - N_A] \tag{1.10}$$

Deep in the bulk the neutrality condition has to be respected and $\rho(x) = 0$ so

$$N_D - N_A = n(\infty) - p(\infty) \tag{1.11}$$

or using (1.7) and (1.8)

$$N_D - N_A = n_i\big[\exp(u_B) - \exp(-u_B)\big] = 2n_i \sinh(u_B). \tag{1.12}$$

Generalizing for any x, from (1.7) and (1.8) one can write

$$n(x) - p(x) = n_i\big[\exp[u(x)] - \exp[-u(x)]\big] = 2n_i\sinh\big[u(x)\big]. \tag{1.13}$$

Substituting (1.12) and (1.13) in (1.10) the Poisson equation becomes

$$\frac{d^2\phi(x)}{dx^2} = \lambda_i^{-2}\big[\sinh[u(x)] - \sinh(u_B)\big] \tag{1.14}$$

where λ_i is the intrinsic Debye length [18], defined as

$$\lambda_i = \Big(\frac{\epsilon_S kT}{2q^2 n_i}\Big)^{1/2} \tag{1.15}$$

Integrating with the following boundary conditions $(x = 0), u(x) = u_S$ and $(x \to \infty), u(x) = u_B$ one obtains an expression for the field at the semiconductor surface [19]:

$$F_S = \mathrm{sgn}(u_B - u_S)\frac{kT}{q\lambda_i}(2)^{1/2}\big[(u_B - u_S)\sinh(u_B) - \cosh(u_B) + \cosh(u_S)\big]^{1/2} \tag{1.16}$$

In order to simplify the above expression one can define a *dimensionless* electric field

$$F(u_S, u_B) = (2)^{1/2}\big[(u_B - u_S)\sinh(u_B) - \cosh(u_B) + \cosh(u_S)\big]^{1/2} \tag{1.17}$$

The expression of the surface field becomes:

$$F_S = \mathrm{sgn}(u_B - u_S)\frac{V_T}{\lambda_i}F(u_S, u_B) \tag{1.18}$$

where $V_T = kT/q$ and $\mathrm{sgn}(u_B - u_S)$ is positive for $u_B > u_S$ and negative for $u_B < u_S$. To calculate the total charge at the surface of the semiconductor one has to use Gauss's law, thus obtaining

$$Q_S = \epsilon_S F_S = \mathrm{sgn}(u_B - u_S)C_0 V_T F(u_S, u_B) \tag{1.19}$$

with $C_0 = \epsilon_S/\lambda_i$ the effective specific semiconductor capacitance.
The variation of the surface charge density is presented in figure 1.6 for a p-type semiconductor with a doping $N_A = 10^{15}cm^{-3}$ and an intrinsic concentration $n_i = 10^{10}cm^{-3}$ at $T = 300K$. These being typical values for organic semiconductors [20], like poly(3-hexyl)thiophene.

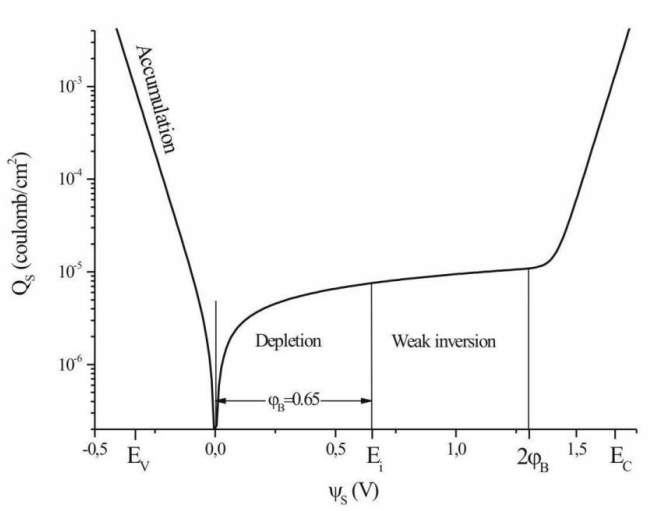

Figure 1.6: Variation of Q_S with ψ_S for a p-type semiconductor having $N_A = 10^{15} cm^{-3}$ at $T = 300K$ and $\phi_B = 0.65V$

1.2.3 Capacitance of the MIS diode

Low Frequency Capacitance

As mentioned in the beginning of the chapter, due to the insulator layer the charges cannot flow freely through the MIS diode, thus its behavior being purely capacitive. The total capacitance of the ideal structure can be described by a series of RC elements, corresponding to the insulator and semiconductor, respectively, as depicted in figure 1.7.
The total capacitance is given by the formula

$$\frac{1}{C} = \frac{1}{C_{ins}} + \frac{1}{C_s} \tag{1.20}$$

where C_{ins} is the insulator capacitance is the geometrical capacitance given by $C_{ins} = \epsilon_0 \epsilon_{ins} A / d_{ins}$. The semiconductor capacitance, C_s, is defined as the variation of the surface charge Q_s with the surface potential ϕ_s

$$C_s = \frac{\delta Q_s}{\delta \phi_s} = -\frac{q}{kT} \frac{\delta Q_s}{\delta u_s} \tag{1.21}$$

where the dimensionless potential u_s has been defined in (1.4). By substituting (1.19) in (1.21) the expression of the semiconductor capacitance becomes:

$$C_s = -\text{sgn}(u_B - u_S) C_0 \frac{\sinh(u_S) - \sinh(u_B)}{F(u_S, u_B)} \tag{1.22}$$

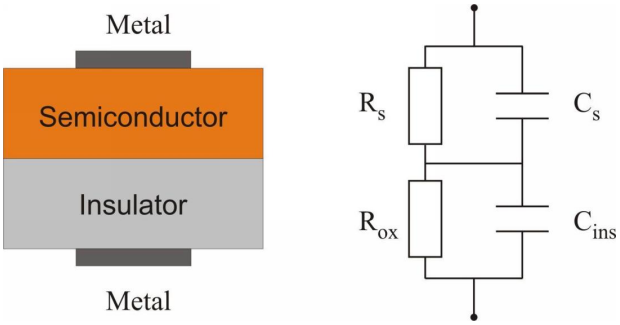

Figure 1.7: MIS diode and its equivalent electrical circuit

One should notice that the above expression for C_S is derived assuming that both minority and majority carriers are in equilibrium with the surface potential or in other words they are following instantaneously the band bending generated by the gate bias and the ac voltage. This can only happen at low frequencies thus the capacitance derived in equation (1.22) has to be called the *low frequency capacitance*. In the case of a p-type semiconductor, at positive voltages, the capcitance will increase and saturate at the insulator capacitance - the dotted line in figure 1.8.

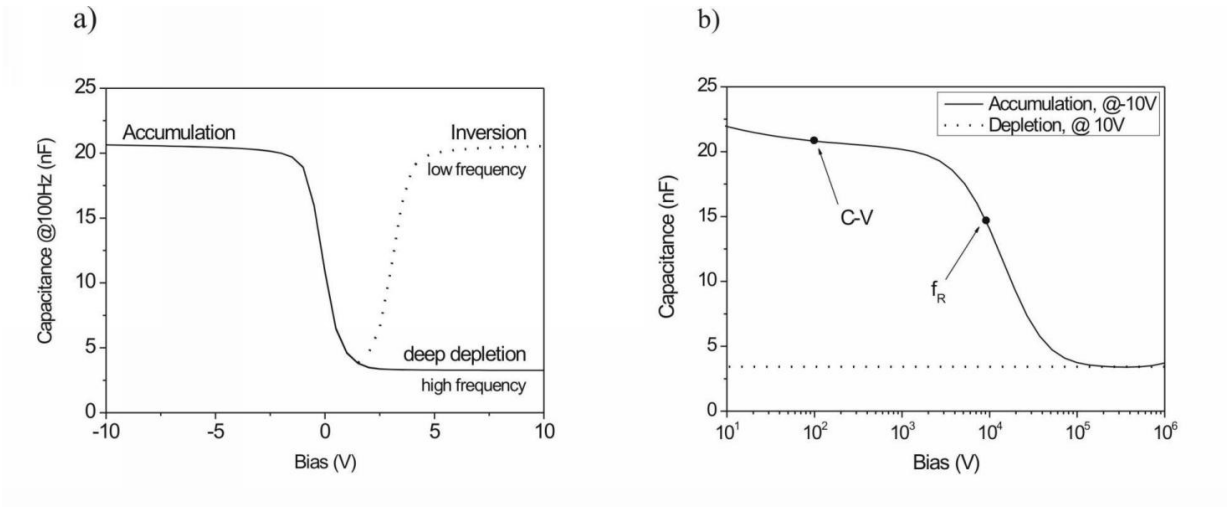

Figure 1.8: MIS diode with p-type semiconductor: a) capacitance-voltage, b) capacitance-frequency; low frequency behaviour is marked by the dotted line

This is typical for inorganic MIS diodes where the charge carrier generation speed is high enough to follow the measurement frequency. At high positive values of the bias an inversion layer will form at the semiconductor-insulator interface. This layer screens the bulk of the semiconductor against variations of the gate bias, thus resulting in a saturation of the capacitance. In the same manner, when the gate bias is negative, positive charge accumulates at the interface, screening the silicon and resulting again in the saturation of

the capacitance. In between these extremes it can be seen that the capacitance of the MIS diode is varying, the fastest change taking place when the charge at the interface consist mainly of ionized acceptors.
In the case of the organic semiconducting materials, as it will be explained in the next section, the behaviour of the capacitance, at positive bias values, is different, as shown in figure 1.8 by the continuos line. The capacitance saturates at a much lower value and it is said that the device is in deep depletion.

Deep Depletion Capacitance

When the gate bias is swept faster than the minority carrier generation speed, no inversion layer will be formed close to the interface and the device is said to be in the *deep-depletion regime*. It is important to notice that in organic materials the inversion regime is usually not reached as the generation time for minority carriers in a wide band-gap semiconductor is very large compared to the measurement frequency. Considering this, the deep-depletion regime is better suited to describe the behavior of a real organic MIS diode. In order to obtain the expression of the capacitance in this regime one has to solve the Poisson equation neglecting the term due to electrons:

$$\frac{d^2\phi(x)}{dx^2} = \frac{qn_i}{\epsilon_S}\big[2\sinh(u_B) - \exp(u_B - u_S)\big] \tag{1.23}$$

Using a similar approach as in the previous section one will obtain the expression for the surface field:

$$F_{S,dd} = \mathrm{sgn}(u_S)\Big[\frac{2qn_iV_T}{\epsilon_S}[2u_S\sinh(u_B) + \exp(u_B)(\exp(u_S) - 1)]\Big]^{1/2} \tag{1.24}$$

and the deep-depletion capacitance will have the following expression:

$$C_{S,dd} = \frac{qn_i}{F_{S,dd}}\big[2\sinh(u_B) - \exp(u_B - u_S)\big] \tag{1.25}$$

The gate bias is the sum of voltage drop on the insulator, the potential across the semiconductor and the flat-band voltage:

$$V_G = V_{FB} + V_T u_S + V_{ins} \tag{1.26}$$

where V_{ins} represents the voltage drop on the insulator and is given by

$$V_{ins} = \frac{d_{ins}\epsilon_S}{\epsilon_{ins}}F_{S,dd} \tag{1.27}$$

The origin of the flat-band voltage, defined at the beginning of this chapter, will be discussed in more detail in the following.

1.2.4 The Real MIS diode

The band diagram in figure 1.5 corresponds to a non-ideal MIS diode as at thermal equilibrium and V=0, the bands are not flat, meaning the semiconductor is not neutral everywhere. In order to achieve this a bias has to be applied to the gate and its value is called the *flat-band voltage*. The reason why there is a flat-band voltage resides in the presence of charges in the insulator and/or at the interface between the insulator and the semiconductor, as it can be seen in figure 1.9 [3].

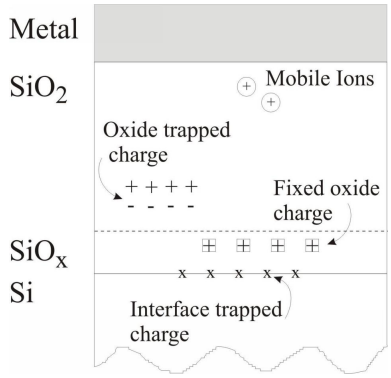

Figure 1.9: Different types of charge present in silicon oxide, after [3]

As nowadays the quality of SiO_2 is almost perfect one can neglect the influence of the total insulator and interface trapped charge. Nonetheless the extensive analysis of these kinds of trapped or mobile charges, done in the past on the the Si-SiO_2 diode, is useful when it comes to the analysis of the SiO_2-organic semiconductor or organic-organic devices, as the organic materials usually contain residues which might act as different kinds of trapped charges. Apart from the ionic contamination, at the interface there are two kinds of charge centers:

1. insulator fixed charges - localized charge centers which cannot change their charge state by exchange of mobile carriers with the semiconductor.

2. Interface trap charges - charges localized on centers that can change their charge state by exchange of mobile carriers with the semiconductor.

Both insulator fixed charges and interface trap charge are defects and their presence depends on the processing history of the device. It is not possible to determine the density of insulator fixed charges because it is not possible to tell apart the interface trap levels located close to or in the semiconductor bands, so usually the measurement results contain both the fixed charges and the band edge interface trap charges. But as the amount of fixed insulator charge is small in comparison with the interface trap charge so one can neglect it.

In this case the flat-band voltage is related to the density of interface trap charge through the next relation:

$$V_{FB} = \Phi_{MS} - \frac{qN_{if}}{C_{ins}} \tag{1.28}$$

where Φ_{MS} is the workfunction difference between the gate metal contact and the semiconductor, C_{ins} is the specific capacitance of the insulator, q is the elementary charge and N_{if} is the density of interface trap charge. Considering the expression (1.27) for the gate bias one can notice that the magnitude and the sign of the interface trap charges will shift the capacitance-voltage characteristic along the bias axes, without affecting its shape. In the next image deep depletion CV characteristics have been simulated for a p-type material with an acceptor doping value $N_A = 10^{16}cm^{-3}$, intrinsic carrier concentration $n_i = 10^{10}cm^{-3}$ and insulator thickness $d_{ins} = 50nm$. The flat-band voltage has been varied between -3 and 3V in 1V steps; the corresponding values for the interface trap charge being shown in the graph.

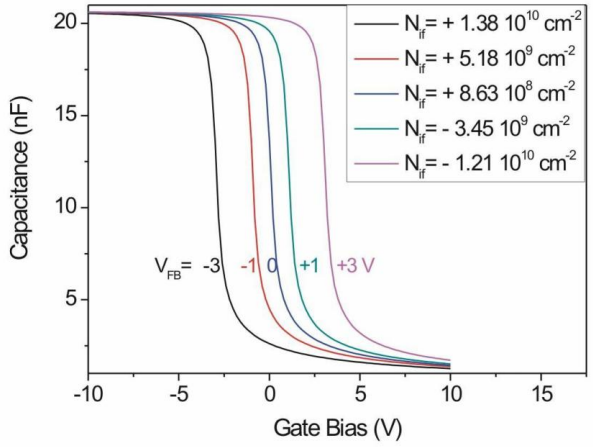

Figure 1.10: Influence of magnitude and sign of interface trap charges on the CV characteristic of an MIS diode with $d_{ins} = 50nm$, $n_i = 10^{10}cm^{-3}$ and $N_A = 10^{16}cm^{-3}$

It can be noticed that the shift of the CV curves is "inversely proportional " to the sign and magnitude of the interface trap charges, so positive interface trap charges will lead to a shift toward more negative values of the gate bias and positive interface charges to more negative values, respectively.
Another important factor determining the operation of an MIS device is represented by the trap levels in the semiconductor. These are due to impurities and as their energy levels are located in the semiconductor bandgap, they can exchange charge with the conduction or valence band. The simplest kind of these trap charges are represented by donor or acceptor

impurities. The next graph shows the influence of acceptor doping, in p-type material, on the CV characteristics for a fixed intrinsic concentration and interface trap charge.

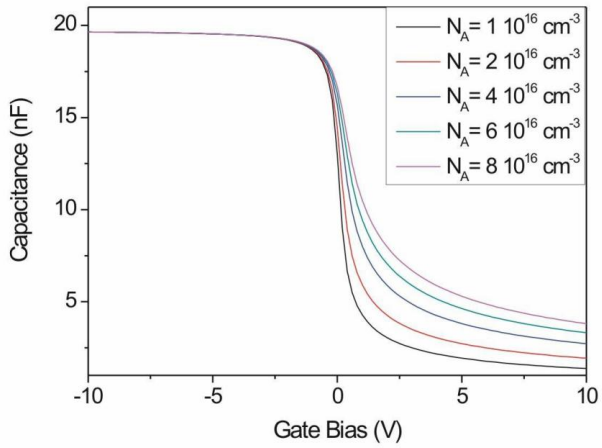

Figure 1.11: Influence of doping on the CV characteristic of an MIS diode with $d_{ins} = 50nm$, intrinsic concentration $n_i = 10^{10}cm^{-3}, V_{FB} = 0$

The depletion capacitance, at positive gate bias values, depends on the doping because of the dependence of the width of the depletion layer on it. This means the higher the doping the smaller the width of the depletion length which is necessary in order to compensate the acceptors. Thus the depletion capacitance becomes larger and the total capacitance of the series between the insulator and depletion capacitances will be smaller, as it can be seen in figure 1.11.
The influence of the doping on the CVs can be better seen if one considers the Schottky-Mott analysis of CV characteristics [3]. This basically states that the derivative of C^{-2} with respect to the gate bias is inversely proportional to the doping concentration:

$$\frac{\delta C^{-2}}{\delta V} = \frac{2}{\epsilon_0 \epsilon_S q N_A A^2} \tag{1.29}$$

where ϵ_S is the relative dielectric constant of the semiconductor, ϵ_0 the permittivity of vacuum, q the elementary charge, A the area of the device and N_A the doping concentration. Figure 1.12 shows the same data from figure 1.11 transformed for the Schottky-Mott analysis. One can notice that the slope is linearly scaling with $1/N_A$ as predicted by the Schottky-Mott model. This representation of the data is commonly used to extract the value of the doping.

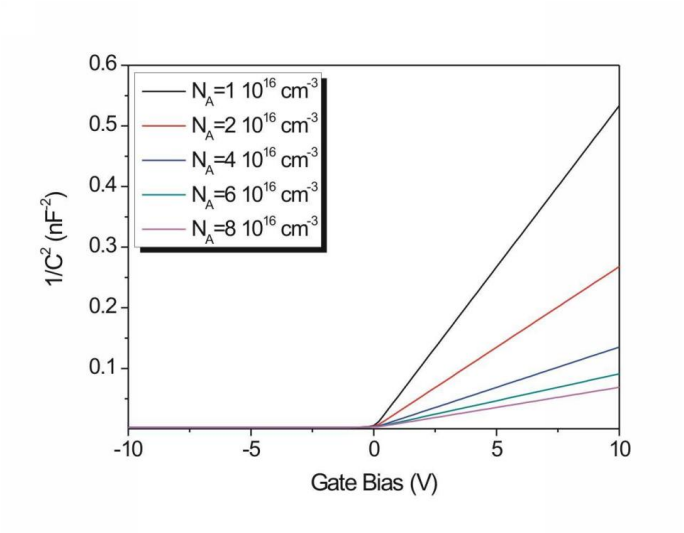

Figure 1.12: Schottky-Mott analysis of the CV characteristics presented in figure 1.11

When instead of SiO_2 organic insulators are used, they might contain mobile ions. The mobile ions are usually residues of the synthesis process of the organic insluator and they can also influence the CV characteristics. In order to evidentiate their effect on the CV, the gate bias is swept also in the reverse direction. If mobile ions are present the CV curve will develop a hysteresis, whose width is proportional to the amount and mobility of the ions. A typical curve is presented in the next figure.

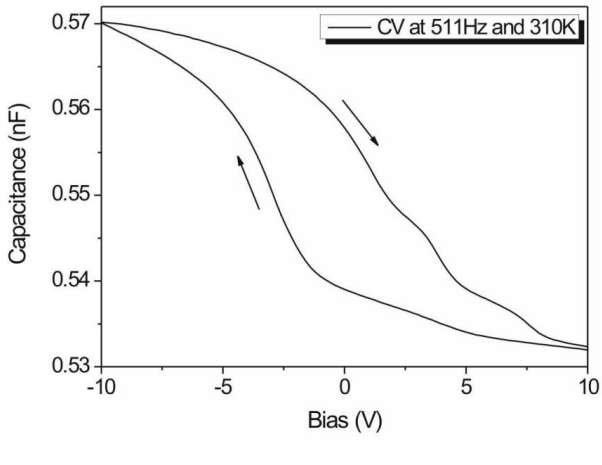

Figure 1.13: Capacitance-voltage characteristic of an Au/P3HT/Polymer Insulator/ITO MIS diode at 511Hz and 310K. The arrows indicate the sweep direction of the gate bias.

It is worth to notice that the shape of this curve is much more complicated compared to the ones previously presented. This is due to the contribution of various factors, like the mobile charges, traps, electrical properties of the insulator and their dependence on temperature and other parameters, which are going to be analysed in chapter 4.

1.3 Organic Field-Effect Transistors

1.3.1 Introduction

The organic field-effect transistors, first report dating back to 1986 [5], have been extensively researched and important progress in their performance and understanding of their operation has been made. In most of the cases the semiconductor material is a p-type small molecule or conjugated polymer, as there are only a few n-type organic semiconductors available nowadays. The performance of OFETs can be compared to the amorphous Si (a:Si) thin film transistors, the field-effect mobility being in the range of $0.5-1$ cm^2/Vs and ON/OFF ratios of 10^6-10^8. In the following the principle of operation, important parameters and means of analysis will be described.
The organic field-effect transistors have the geometry of a thin film transistor which was proposed by Weimer in 1962 [6] and is presented in figure 1.14. This kind of geometry is particularly suitable for low mobility semiconductors. OFETs are devices operating in accumulation, as the inversion regime can't be reached in organic semiconductors due to the extremely long generation times of minority carriers, as previously explained.

1.3.2 Principle of Operation

The transfer characteristics

The transfer characteristic shows the variation of the drain current with the gate bias at a given drain bias. As in the case of the MIS diode one can distinguish between three states of the device, depending on the values of the gate bias - the depletion, intrinsic and accumulation mode. In the depletion regime, figure 1.14(c), the bias applied to the gate is positive and the semiconductor is depleted of majority charges. The distance up to which it is depleted is, as in the case of the MIS diode, the depletion length and can be calculated with the same formula.

$$d_{dep} = 2 \cdot \sqrt{\frac{\epsilon_0 \cdot \epsilon_S \cdot \mid \Psi_B \mid}{q \cdot N_A}} \tag{1.30}$$

The current flowing through the device consists only of the semiconductor bulk current, which due to the low intrinsic charge carrier density is very small as seen in the corresponding region of transfer characteristic in figure 1.14 and basically does not vary with the gate voltage. This happens until the gate bias reaches the so called switch-on voltage, V_{SO}, when the semiconductor is in the intrinsic state. At the switch-on voltage the

flat-band condition is fulfilled. This means that V_{SO} is determined by any fixed charges in the insulator layer and/or any fixed charges at the semiconductor-insulator interface [3]. Above V_{SO} the current increases with V_G and the device is found to be in the accumulation regime (figure 1.14(a)).

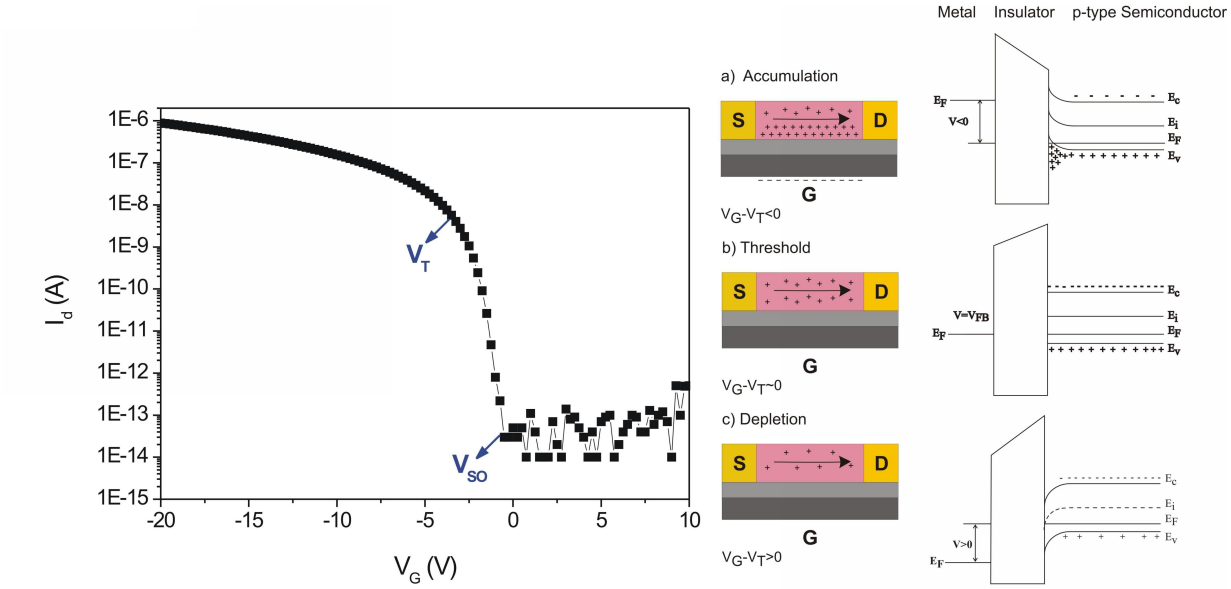

Figure 1.14: The three different regimes of operation of an OFET:
a) accumulation, $V_G - V_T < 0$, b) threshold, $V_G - V_T \sim 0$, c) depletion, $V_G - V_T > 0$ at V_D= -20 V; geometrical device parameters: Z=1000 μm, L= 5 μm, d_{ins}= 200 nm

Output characteristics

In order to determine the expression for the drain current one has to determine the elemental resistance of an element dx along the channel (see figure 1.15), which is related to the charge carrier mobility and the charge at a given position along the x axes.
The elemental resistance expression is given by

$$dR = \frac{dx}{W\mu \mid Q(x) \mid} \tag{1.31}$$

The charge $Q(x)$ is the sum of the surface charge induced by the gate voltage and the bulk charge (due to intrinsic doping of the semiconductor): $Q(x) = Q_{surf} + Q_{bulk}$. The bulk charge is $\pm qN_A d_s$, where q is the elemental charge, N_A is the intrinsic doping and d_s is the semiconductor thickness.

The gate induced charge is given by the following equation:

$$Q_s = -C_i\big[V_G - V_{FB} - V_s(x) - V(x)\big] \tag{1.32}$$

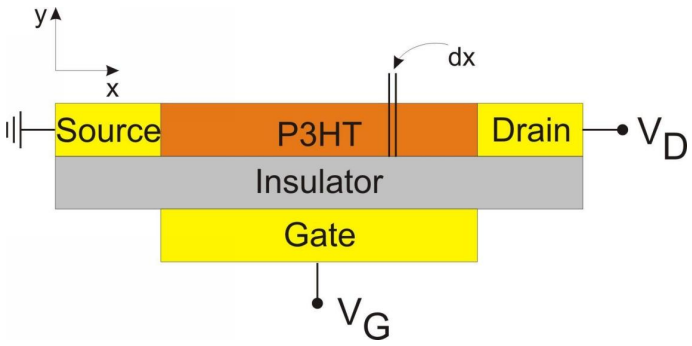

Figure 1.15: Schematic view of an OFET with elemental segment dx used in calculating elemental resistance dR

where C_i is the specific capacitance of the insulator, V_{FB} is the flat band voltage as defined for the MIS diode, $V_s(x)$ is the ohmic voltage drop through the semiconductor and V_x is the voltage in the channel. In order to compute the current one has to make some simplifying assumptions [7].
For a small drain voltage:

1. only the drift component of the current will be considered;
2. the mobility will be considered constant in the entire accumulation layer;
3. the doping is presumed homogeneous;
4. leakage currents will be neglected;
5. it will be considered that the field in the transversal direction, with regard to the substrate, is much larger than the field in the longitudinal direction.

The last assumption is called the *the gradual channel approximation* which basically states that the channel length is much larger then the insulator thickness. This way the potential $V(x)$ depends only on the drain voltage and it is gradually increasing from zero at the source electrode to V_d at the drain. With all these considered the current can be found by integrating the following equation:

$$dV = I_d dR = \frac{I_d dx}{W\mu \mid Q(x) + Q_0 \mid} \tag{1.33}$$

The integration from source (x=0, V=0) to drain (x=L, V=V_d) leads to:

$$I_d = \frac{WC_i}{L}\mu\big[(V_G - V_T)V_d - \frac{V_d^2}{2}\big] \tag{1.34}$$

where W is the channel width, L is the channel length, C_i is the insulator specific capacitance, μ is the constant mobility. At low values of the drain bias equation (1.34) can be reduced to a simpler form:

$$I_{D,lin} = \frac{W}{L}\mu C_i(V_G - V_T)V_D \tag{1.35}$$

which shows that the drain current depends linearly on the drain bias. At high values of the drain bias, when the drain current saturates and the equation (1.34) takes the following form:

$$I_{D,sat} = \frac{W}{2L}\mu C_i\left[(V_G - V_T)\right]^2 \tag{1.36}$$

where W is the length of the channel, L is the width of the channel, μ is the constant mobility, C_i is the specific areal capacitance of the insulator and V_T is the so called threshold voltage. V_T takes into account apart from the influence of the fixed charges in the insulator and/or the interface between the semiconductor and the insulator, also the bulk current. These equations would predict a linar dependence of the current with V_D, at small values of V_D - *the linear regime*, followed by a quadratic dependence up to a maximum value - *the quadratic regime* after which the current saturates with respect to V_D - *the saturation regime*. In figure 1.16 a typical output characteristic is shown and the three regions are delimited.

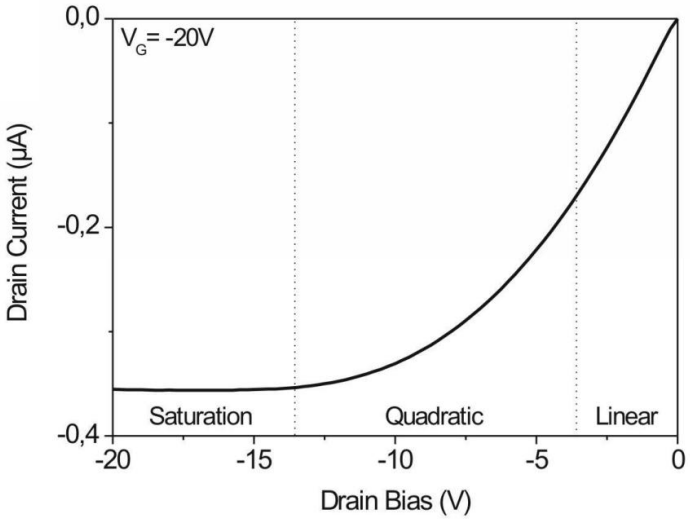

Figure 1.16: Output characteristic of an OFET at V_G= -20 V. The three regimes - linear, quadratic and saturation are visible.Device geometrical parameters: W=1000 μm, L= 5 μm, d_{ins}= 200 nm

1.3.3 The threshold and switch-on voltage

In equation (1.34) V_T is is defined as the sum of the flat-band voltage and the voltage required to induce an equal number of charges to compensate the bulk doping charge:

$$V_T = V_{FB} \pm \frac{qn_A d_s}{C_i} - 2\phi_B \tag{1.37}$$

where V_{FB} is the flat-band voltage, ϕ_B is the bulk potential, as defined for the MIS diode, the other parameters being previously defined. The V_T explains why at zero gate voltage there can be a non-zero current flowing through the structure. It should be noticed that the expression of the drain current derived here is quite identical to the one valid for the classical MOSFET. The major difference between the two devices, as mentioned in the previous section, lies in the operation mode, which for an OFET consists in the formation of an accumulation layer, while the MOSFET has an inversion layer. The presence of an inversion layer (which can't be obtained in organics) requires that the gate voltage is high enough to cause the Fermi level to cross the intrinsic level, which is the definition of the threshold voltage. So in the case of OFETs the threshold voltage is not defined, as there is no inversion layer. V_T can be regarded as a pseudo threshold voltage. The origin of V_T has been extensively analysed by Shur [8] for a-Si:H TFTs. As in amorphous silicon there is a high density of localized states in the energy gap. At low voltages all the induced charge goes into these states and transport takes place via hopping between these states. As more charge is induced by the rise of the gate voltage, more states are filled and the Fermi level moves closer to the conduction band, thus the mobility increasing. So the measured mobility is gate bias dependent, or in other words charge density dependent.
A directly observable parameter is the so called *switch-on voltage*, which is defined, based on the theory of the MIS diode, as the flat-band voltage.

$$V_{SO} = V_{FB} = \Phi_{MS} - \frac{qN_{if}}{C_{ins}} \tag{1.38}$$

At values bellow the switch-on voltage the drain current is null, while at higher values of the gate bias the drain current scales with V_G.

1.3.4 Field-Effect Mobility

The distribution of field-induced charge in the channel along the perpendicular direction to the interface is non-uniform, decreasing toward the bulk. To determine it one has to solve the Poisson equation

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\epsilon_S} \tag{1.39}$$

where V is the potential, x the direction perpendicular to the channel, ρ the charge density and ϵ_S th permittivity of the semiconductor. The Poisson equation for this case

can't be solved analytically, but only numerically [9]. A good approximation for the charge density is given by [10]

$$\rho(x) = \frac{(C_i V_G)^2}{2k_B T \epsilon_S} \left[1 + \frac{x}{\sqrt{2} L_D}\right]^{-2} \tag{1.40}$$

where ρ(x) is the charge density, C_i is the specific insulator capacitance, V_G is the gate bias and L_D is the Debye length, given by:

$$L_D = \frac{\sqrt{2} k_B T \epsilon_S}{q C_i V_G} \tag{1.41}$$

This approximation gives a good picture for the charge density only at high gate voltages, but nonetheless it shows clearly that most of the charge is concentrated in the first few nanometers from the insulator-semiconductor interface, as it can be seen in the next figure.

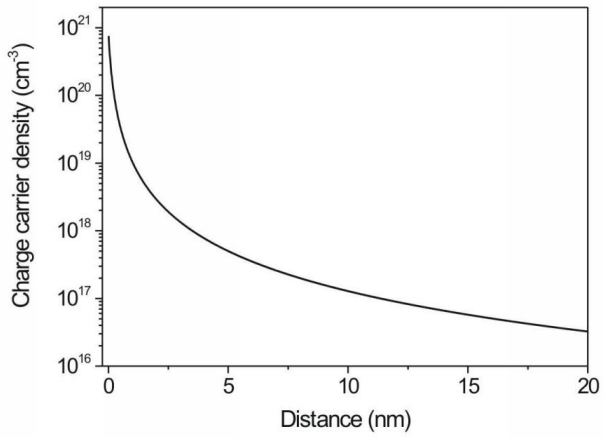

Figure 1.17: Charge distribution in the channel of an organic FET, with $C_i = 17.25 nF/cm^2$ and $V_G = 100V$

1.3.5 Charge carrier density dependent mobility

Big differences in the mobilities between FETs, MIS and hole-only diodes are usually observed in the organic devices as it has been noticed in amorphous silicon devices, too. There the explanation of this behaviour is that the mobility is charge carrier density dependent. Recently a model assuming such a dependence of the mobility in highly disordered materials has been developed by Pasveer et al. [11].
This model is establishing a unified theoretical description of the dependence of the mobility on temperature, charge carrier density and the electric field. The expression of the

mobility is determined by finding a numerical solution of the master equation representing hopping of charge carriers on a lattice of sites:

$$\sum_{j \neq i} \left[W_{ij} p_i (1 - p_j) - W_{ji} p_j (1 - p_i) \right] = 0 \tag{1.42}$$

where p_i is the probability that site i is occupied by a charge and W_{ij} is the transition rate for hopping from site i to j. The transition rates between states i to j in a system where hopping is assumed to be a thermally assisted tunneling process and assuming coupling to a system of acoustical phonons have the following expression [12]:

$$W_{ij} = \begin{cases} \upsilon_0 \cdot \exp[-2\alpha R_{ij} - \beta(\epsilon_j - \epsilon_i)] & , \epsilon_j > \epsilon_i \\ \upsilon_0 \cdot \exp[-2\alpha R_{ij}] & , \epsilon_j < \epsilon_i \end{cases} \tag{1.43}$$

where $\beta = 1/kT$, υ_0 is an intrinsic rate, $R_{ij} \equiv \mid R_j - R_i \mid$ is the distance between sites i and j, α is the inverse localization length of the localized wave functions under consideration and ϵ_i is the on-site energy of site i. The energetic disorder is described on each lattice site by a gaussian with the width σ. The solution of this equation is well parameterized by the following expression:

$$\mu(T, p) = \mu_0(T) \cdot \exp\left[\frac{1}{2}(\hat{\sigma}^2 - \hat{\sigma})(2pa)^\delta\right] \tag{1.44}$$

$$\text{with} \qquad \mu_0(T) = \mu_\infty \cdot c_1 \exp(-c_2 \hat{\sigma}^2) \tag{1.45}$$

$$\text{where } \delta = 2\frac{\ln(\hat{\sigma}^2 - \hat{\sigma}) - \ln(\ln(4))}{\hat{\sigma}^2} \text{ and } \mu_\infty = \frac{a^2 \cdot \upsilon_0 \cdot e}{\sigma} \tag{1.46}$$

where $\hat{\sigma} = \sigma/kT$ with σ the width of the Gaussian distribution of states, k the Boltzmann constant and T the absolute temperature; a is the lattice constant with a typical value in the nanometer range. The constants c_1 and c_2 have the following values $c_1 = 1.8 \cdot 10^{-9}$ and $c_2 = 0.42$. If one wants to take into account the electric field too, then the above mobility will become:

$$\mu(T, p, E) \approx \mu(T, p) \cdot f(T, E) \tag{1.47}$$

where the prefactor *f(T,E)* is parametrized by:

$$f(T, E) = \exp\left\{0.44(\hat{\sigma}^{3/2} - 2.2)\left[\sqrt{1 + 0.8\left(\frac{Eea}{\sigma}\right)^2} - 1\right]\right\} \tag{1.48}$$

It can be noticed that if the value of the field is low (V_G not too high) $f(T, E) \to 1$ and one is left with equation 1.44 as expression for the mobility.

1.4 Space Charge Limited Diodes

Apart from the MIS diode and FET a third type of device, the space charge limited diode, is used to gather further insight into the transport in organic materials. In this case, the structure of the device is simpler, the organic layer being sandwiched between two metal contacts as it is represented schematically in figure 1.18. This structure enables one to get information about the charge transport in materials with low carrier mobility at low fields, as after the charge is injected in the organic material, it will travel towards the opposite electrode under the influence of the external electrical field. The transport between the two electrodes is determined by the conduction properties of the material.

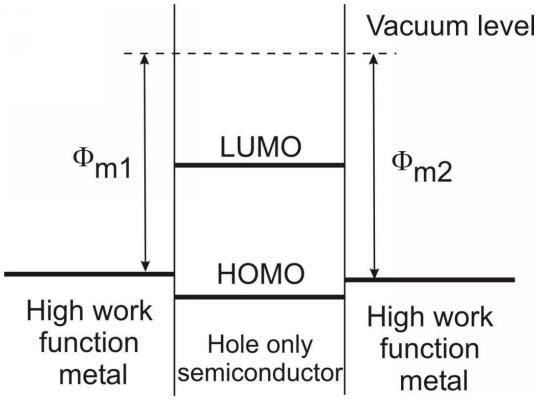

Figure 1.18: General energy band diagram of an SCL diode with a hole only semiconductor

1.4.1 Built-in voltage

When a semiconductor is being brought in contact with a metal, due to the different work-functions, the semiconductor will be depleted of majority carriers in the vicinity of the contact in order to reach equilibrium. This leads to a band bending which acts like a barrier, preventing the majority carriers to diffuse further to the metal. For the organic devices one can define the *built-in potential* as the work function difference between the electrode metals:

$$\Phi_{bi} = \Phi_{M_1} - \Phi_{M_2} = q \cdot V_{bi} \tag{1.49}$$

The built-in potential has to be firstly overcome in order for the current to flow through the device. For a precise analysis of the data one has to correct the values of the applied voltage for the built-in one.
In figure 1.19, the $J-V$ characteristic of an P3HT diode (400nm P3HT) has been corrected for the built-in voltage between the gold and the P3HT (+0.1V). As at room temperature the conduction is almost trap free (see section 1.4.3), after applying the V_{bi} correction the value of the slope of the curve is almost two.

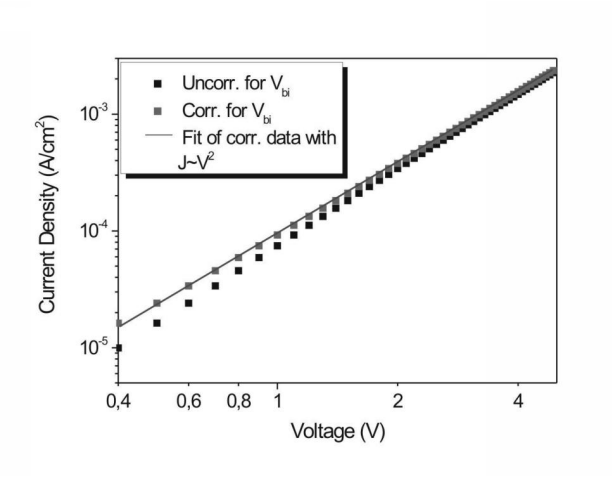

Figure 1.19: Log-log plot of current-voltage characteristic before and after correcting fot the built-in voltage

1.4.2 Current density in a space charge limitted diode

Usually the contact between the two metallic electrodes and the organic semiconductor layer is considered to be ohmic, but from electrostatic reasons, there is only a given amount of charge which can be injected into the organic semiconductor. At low fields ($<10^4$ V/cm), the current-voltage characteristic of such a device is ohmic as the number of injected charges is small compared to the intrinsic charge carrier concentration of the organic material. As the external field is increased, the number of injected charges increases, too, but as the organic materials have low charge carrier mobility, a charge build-up takes place in the neighborhood of the injecting contact which is controlling the current flow.
As a result of the space charge region the dependence of the electric field inside the device is non-uniform and the current-voltage charactersitc is non-linear, depending drastically on the charge transport in the bulk of the device. This can be influenced by the existence of traps in the semiconductor and their distribution and also by the dependence of mobility on the field and temperature, as it will be seen below. The basic equation describing the charge transport is the Poisson equation which connects the electric field and the local charge density:

$$\frac{dF}{dx} = \frac{q}{\epsilon_0 \epsilon_S}\big[p_c(x) + p_t(x)\big] \tag{1.50}$$

where q is the elementary charge, ϵ_0 is the vacuum permittivity, ϵ_S is the dielectric constant of the semiconductor, $p_c(x)$ is the density of carries in conductive states and $p_t(x)$ is the density of trapped carriers. The total charge density, $p(x)$, is given by $p_c(x) + p_t(x)$. Ignoring the diffusion contribution, the expression of the current density is given by:

$$J = q\mu F(x) p_c(x) \tag{1.51}$$

where μ is the carrier mobility and can be field or temperature dependent or both. The density of trapped charge, in equilibrium, is given by the Fermi-Dirac distribution

$$p_t(x) = \int_0^\infty \frac{g(E)}{1 + \exp\big[-\frac{E-E_F}{kT}\big]} dE \tag{1.52}$$

where $g(E)$ represents the distribution of traps. The position of the Fermi level can be determined from :

$$p_c = N_c \exp\big[-\frac{E_c - E_F}{kT}\big] \tag{1.53}$$

Combining (1.50) and (1.51) one gets the following differential equation:

$$\frac{dF}{dx} = \frac{J}{\epsilon_0 \epsilon_S \mu F(x)} + \frac{q}{\epsilon_0 \epsilon_S} p_t(x) \tag{1.54}$$

which has to be numerically solved in order to obtain the current-voltage characteristics. The boundary condition is $F(0) = 0$ states that the injecting contact is ohmic, behaving as a charge reservoir. The resulting voltage is given by $V = V_{appl} - V_{bi} = \int_0^L F(x)dx$, with L thickness of the semiconducting layer.

1.4.3 Influence of traps on SCLC

Trap-free limit

The simplest case is the one when it is assumed that the mobility is constant and there are no traps or the *trap-free space charge limited current* - TF-SCLC. This case has been first analysed by Mott and Gurney in 1940. The relation (1.54) becomes in this case

$$J = q p_c \epsilon_0 \epsilon_S \mu F(x) \frac{dF}{dx} \tag{1.55}$$

and after integration from x=0 to L results the Mott-Gurney law

$$J = \frac{9}{8} \epsilon_0 \epsilon_S \mu \frac{V^2}{L^3} \tag{1.56}$$

As mentioned before, the space charge limiting effect becomes predominant at high voltages. In a log-log plot it will be observed as a linear dependence of the current on the voltage with a slope two.

Discrete trap level

If trap levels are present in the material, at low voltage most of the injected carriers will be fixed, so the density of free carriers will be small and the currents will be smaller compared with the trap-free case, at the same value of the applied voltage.
In the case of a discrete trap level located near the conduction or valence band the distribution is given by: $g(E) = N_t \delta(E - E_t)$, where N_t is the total trap concentration and E_t

is the energetic position of the trap level. With respect to the Fermi level the densities of free and trapped carriers are given by:

$$p_c = N_c \exp\Big[-\frac{E_c - E_F}{kT}\Big] \qquad \text{and} \qquad p_t = N_t \exp\Big[-\frac{E_t - E_F}{kT}\Big]$$

One can define the ratio between the free carriers and the total carrier concentration

$$\theta = \frac{p_c}{p_c + p_t} \approx \frac{p_c}{p_t} = \frac{N_c}{N_t}\exp\Big[-\frac{\Delta E_t}{kT}\Big]$$

where ΔE_t is given by $E_t - E_c$. Thus it can be noticed that, for example, for a discrete trap level with $\Delta E_t = 0.5eV$ and $N_t = 10^{16} cm^{-3}$, with $N_c = 10^{21} cm^{-3}$ one will obtain $\theta \approx 2 \cdot 10^{-4}$, which shows that only a small fraction of the injected carriers are free. If one defines $\mu_{eff} = \theta\mu$, the current density expression is formally identical to the TF-SCLC one

$$J = \frac{9}{8} q\epsilon_0\epsilon_S \mu_{eff} \frac{V^2}{L^3} \tag{1.57}$$

being only shifted to lower currents. When the voltage is high enough that all the trap centers are filled, the current density becomes the same as in the TF-SCLC case, reaching the *trap-filled limit*-TFL. The trap-filling limit value of the voltage is given by:

$$V_{TFL} = \frac{2}{3}\frac{qd^2}{\epsilon_0\epsilon_S} N_t \tag{1.58}$$

Exponential and Gaussian trap distributions

Usually the traps in a semiconductor have a more complex distribution than the ones presented above, due to chemical impurities, unintentional doping or structural irregularities. The densities of states for trap distributions described by exponential or gaussian shapes are given by:

- $g_{exp}(E) = \frac{N_t}{kE_t}\exp(-\frac{E}{E_t})$ - for an exponential distribution
- $g_{gauss}(E) = \frac{N_t}{\sqrt{2\pi}\sigma_t}\exp(-\frac{(E-E_{tm})^2}{2\sigma_t^2})$ - for a gaussian distribution

It is assumed that the mobility is field independent and the free carrier concentration is much smaller than the trapped carrier concentration. An analytical solution can be obtained in this case [13]. The expression of the current density is given by the formula:

$$J_{Exp} = q^{l-1}\mu_p N_v \left(\frac{2l+1}{l+1}\right)^{l+1} \left(\frac{l}{l+1}\frac{\epsilon_0\epsilon_S}{N_t}\right)^{l} \frac{V^{l+1}}{L^{2l+1}} \tag{1.59}$$

where N_t is the density of traps, E_t is the characteristic constant of the distribution, which can be related to a temperature T_c ($E_t = kT_c$), k is the Boltzmann constant, ϵ_0 the permittivity of vacuum, ϵ_S the dielectric constant of the semiconductor, μ_p the carrier mobility, N_c density of states in the valence/conduction band, L is the sample thickness and l is defined as T_c/T or E_t/kT (E_t>kT), where T is the measurement temperature.

From equation (1.59) it can be noticed that the dependence of the current density on the voltage is a power law - $J \propto V^m$, where $m = l + 1$. In a log-log plot it will show as a straight line with the slope m, thus the characteristic energy (temperature) can be directly determined. However the density of traps cannot be determined directly and is taken as a fit parameter.
For the Gaussian distribution of traps there is also an analytical approximate solution, which is valid only for deep traps - $E_{tm} > E_F$. The current density expression in this case is given by [14]:

$$J_{Gauss} = q^{m-1}\mu_p N_v \left(\frac{2m+1}{m+1}\right)^{m+1} \left(\frac{m}{m+1}\frac{\epsilon_0\epsilon_S}{qN_t'}\right)^m \frac{V^{m+1}}{d^{2m+1}} \tag{1.60}$$

where $m = (1 + 2\pi\sigma_t^2/16k^2T^2)^{1/2}$ and $N_t' = (N_t/2)exp(E_{tm}/mkT)$. It can be noticed that the expression of J_{Gauss} is identical to J_{Exp} so it is not really possible to distinguish between a Gaussian distribution of traps and an exponential one without analizing the temperature dependence of the J-V characteristics by comparison with simulated data.

1.4.4 Field dependent mobility

Quite often the J-V characteristic doesn't follow a power law dependence at high voltages. This can be attributed to a field dependent mobility. This has been explained by Murgatroyd [15] as due to the Frenkel effect [16], which states that in the presence of a strong field the effective depth of a trap level is reduced. With this a very good approximate solution is given by:

$$J_{Mur} \approx \frac{9}{8}\epsilon_0\epsilon_S\mu_0\frac{V^2}{L^3}\exp(0.891\beta\sqrt{V/L}) \tag{1.61}$$

The mobility in such a case would be depending on the applied field like: $\mu = \mu_0 exp(\beta\sqrt{F})$. The voltage, at which the Frenkel effect becomes important, is approximately given by L/β^2.

Field and temperature dependent mobility

In general, in a system where the transport takes place via hopping, as in the organic materials, the mobility is temperature activated. An empirical representation is given as a Pool-Frenkel like dependence [17], with the form:

$$\mu = \mu_\infty \exp\big[-(\Delta_0 - \beta_{PF})/kT_{eff})\big] \tag{1.62}$$

where $1/T_{eff} = 1/T - 1/T_0$ is the effective temperature, with T_0 the characteristic temperature, Δ_0 is the activation energy.

Chapter 2

Experimental Methods

2.1 Materials

In this work the main semiconducting polymer used was the regio-regular poly(3-hexyl-thiophene), or in short rr−P3HT; the structure of the monomer unit can be seen in figure 2.1(a). As the side chain of the P3HT is grafted in position three, only the positions two and five are free to form bonds with other monomer units. The possible configurations are head to tail, tail to head, head-head and tail tail. The P3HT used in our devices is of the head to tail (HT) type (see 2.1(b)), with a regioregularity of about 90%. The degree of regioregularity defines how many of the monomer units are connected to each other in a given way (HT, TH, HH or TT). The reason for using HT rr-P3HT lies in the higher mobility of this material, compared to any other possible orientations.
P3HT is a $p-$type semiconductor. The monomer unit consists of thiophene rings, with a hexyl side chain. The thiophene rings and the side chains are coplanar, with π- orbitals perpendicular to this plane. The π-electrons are highly delocalized and the extent of the delocalization along the backbone of the polymer influences strongly the optical and electrical properties of the polymer. On the molecular scale the properties are influenced by the amount of intrachain delocalization - overlapping of π orbitals.
The P3HT was used to build field effect transistors, metal-insulator-semiconductor diodes and hole only diodes, via spin-coating from solution. Various solvents, solution concentration and spinning speeds have been used to produce films of different thicknesses. In the case of field-effect transistors thin films are desired as the influence of the bulk on the messured chracteristics is minimized, while in the case of the MIS and SCLC diodes, thicker films are required. For example, in order to obtain an 100nm thick film on a silicon/silicon oxide surface, a solution of toluene with two weight % P3HT and a spinnnig speed of 3000rpm has to be used. The thickness of the film, at a given spinning speed and solution concentration will depend of the properties of the substrate; the higher the surface energy of the substrate the thinner the film will be. For substrates with high surface energy, the film formation is quite difficult to control, as the solution wetting is poor.

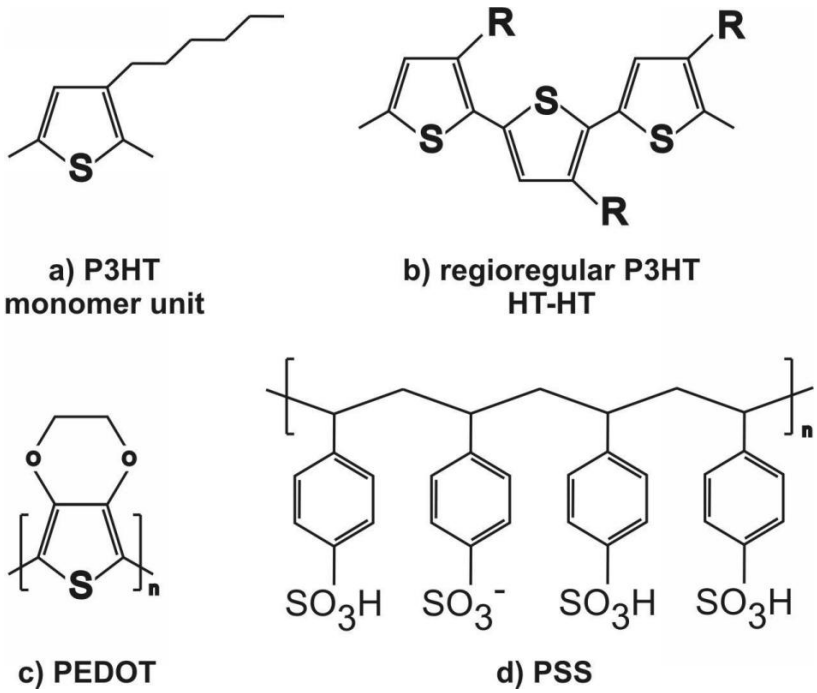

Figure 2.1: Chemical structure of: a) monomer unit of poly(3-hexyl thiophene, b) HT-HT rr-P3HT c) poly(3,4-ethylenedioxythiophene, PEDOT and d) poly(styrenesulfonate), PSS

Usually the P3HT was not doped intentionally and it was used as received (Merck) without any futher purification. The molecular weight of P3HT is in the 40,000 range. The preparation of all the devices was performed in a glove-box system, in nitrogen atmosphere, with water and oxygen levels below 1ppm, as the P3HT is sensitive to these and can be ireversibly oxidized, thus being rendered useless. Additional surface treatments (with self assembling molecules from the silanes class) of the substrates were performed in order to achieve high mobilities. The mobilities corresponding to the different surface treatments were related to the contact angle of water on the substrates. The devices have been annealed at various temperatures in high vacuum or inert atmosphere to modify the structure of the films so that they would have the highest mobility. The good solubility of P3HT allowed us to investigate the influence of the solvent on the electrical performance of the devices. In most of the cases the substrate was heavily doped silicon with high quality silicon oxide, grown via wet oxidation. Influence of other insulators has been investigated. X-Ray Diffraction spectra [21] and Atomic Force Microscopy [22] have shown that the structure of the spin-coated rr−P3HT films consists of crystalline like domains included in an amorphous matrix.

2.2 Devices

Hole Only Diodes

Samples were prepared on 20x20 mm^2 glass substrates covered with indium-tin-oxide−ITO (see cross-section in figure 2.2(a)), which was patterned as seen in figure 2.2(b). The substrates were cleaned with detergent, acetone and isopropanol, each of these steps being followed by thorough rinsing with deionized water. On top of the ITO a thin layer, about 50nm, of PEDOT-PSS (polyethylenedioxythiophene doped with polystyrenesulfonate, see figure 2.1) was spin-coated followed by an annealing step at 140C for 30 min to remove the residual water. The role of the PEDOT-PSS is double, first to improve the injection of holes from ITO into the P3HT and second to improve the planarity of the ITO. Thus when the P3HT is spin-coated on top of this structure the layers are defect free. The spin-coating of the P3HT is performed in the glove-box system mentioned previously. Different solvents for the P3HT like toluene, chloroform, chlorobenzene were used. In the end, to complete the structure gold electrodes about 50 nm thick are evaporated through a shadow mask, defining four identical devices with an area between 12 and 16 mm^2 each. The thickness of the semiconductor polymer is in the range of 100 to 200 nm, as it was determined using a Dektak profilometer.

Figure 2.2: Schematic of the hole only diodes: a) cross-section view and b) top view of the sample with four devices; the active area is marked by dashed lines; typical thickness of various layers is also indicated

Metal Insulator Semiconductor Diodes

The Metal-Insulator-Semiconductor diodes were fabricated in most of the cases on heavily doped silicon wafers with 50 nm of wet thermally grown silicon dioxide. It is very important to have a heavily doped substrate with a small resistance typically less than 0.005 Ωcm^{-1} because, as one measures in an MIS diode the impedance/capacitance variation on frequency and applied bias, one has to minimize any contact resistance which might influence drastically the measured curves, as it will be exemplified later. The substrates underwent the same cleaning procedure as explained above. Then the P3HT was spin-coated from

different solutions. The layer thickness, controlled via the rotation speed (1000 - 3000 rpm) during the spin-coating process and measured with the profilometer, varies between 100 and 300 nm. The top and the gate contacts are evaporated through a hard mask resulting in films with a thickness of about 50 nm and defining two devices with an area of about 30 mm^2. To insure a good gate contact the silicon oxide has been scratched away in a small area ($5x5mm^2$).

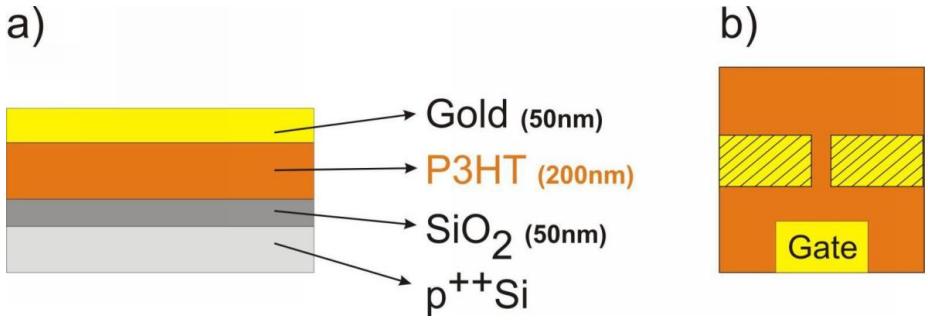

Figure 2.3: Schematic of the MIS diodes: a) cross-section view and b) top view of the sample with two devices; the active area is marked by dashed lines; typical thickness of various layers is also indicated

Field Effect Transistors

The field effect transistors were prepared, usually, on heavily doped silicon substrates with 200 nm silicon oxide. In the case the silicon oxide was replaced by an organic insulator glass was used as a substrate. A thin metallic film, with the role of the gate contact, was thermally evaporated and the organic insulator layer was subsequently spin-coated on top of it. In both cases the electrodes were patterned using conventional lithography. The different kinds of geometries of the electrodes are presented in figure 2.4(b). The circular geometry is preferable to the comb-like one as the source electrode is shielding the channel against undesired parasitic leakage currents [23]. The influence of insulator surface properties, prior to the spin-coating of the semiconductor polymer, has been demonstrated [24] and it will be analysed later, too. The silicon oxide was modified using octadeciltrichlorosilane (OTS) and hexamethyldisilazane (HMDS) in order to induce different levels of hydrophobicity of the surface.

On top of the lithographically patterned substrates the P3HT was spin-coated from solutions of toluene, chloroform and chlorobenzene. Thickness of the layers was in the range of 50 nm to 200 nm. The solubility of the P3HT in the different solvents varies, so in order to increase it they had to be heated to 50°C and stirred. As mentioned above the spin-coating was performed in a glove-box system. Samples were transfered to the cryostat using a load-lock transfer tube in order to avoid exposure to air and light. The geometrical properties of the circular measured FETs were: channel length, W = 1000 or 2500 μm and

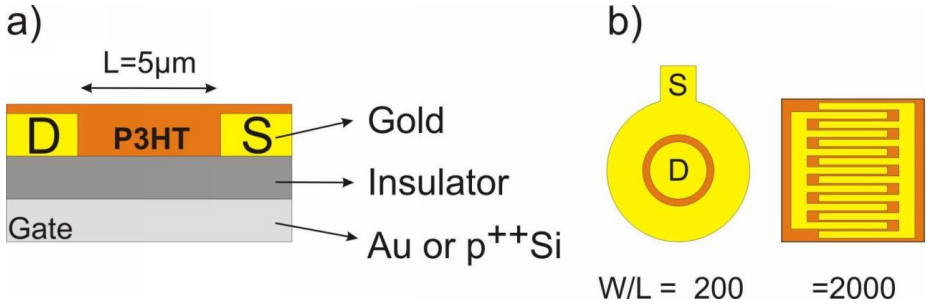

Figure 2.4: Schematic of the field-effect transistors: a) cross-section view and b) top view of the different geometries; typical channel width and ratio between channel width and length are indicated

channel width from 1 to 40 μm.

2.3 Experimental techniques

Most of the semiconductor polymers are highly sensitive to oxygen, moisture and light. Exposure to oxygen and light, especially in the UV range, at the same time can lead to an irreversible oxidation, thus rendering them useless. Moisture can induce undesired doping of the bulk of the material, altering the electrical properties of the devices. For these reasons the storage of semiconductor polymers and preparation of devices based on them has to be carried in an inert atmosphere with very low levels of moisture and oxygen. These conditions are met in a glove-box system (built by Braun GmbH), like the one presented in picture 2.5.
The nitrogen atmosphere inside the glove-box is constantly cleaned of oxygen and water with the help of a copper catalyst system, thus maintaining values below 1ppm . At the same time the atmosphere is filtered of dust. To avoid temporary high levels of water and oxygen the transfer of the materials in and out of the glove-box system is done using a load-lock system, visible on the right end side. The glove-box is fitted with a spin-coater (Suss Microtec Lithography GmbH, model DELTA 10BM) which can reach 5000rpm, used for the deposition of the organic semiconductor layers of the MIS, SCLC diodes and FETs as well as with an oven which can reach 300°C used for the drying of the samples or for thermal treatments. The solvent vapors which are released in the nitrogen atmosphere, during the spin-coating are filtered, by a built-in active carbon filter, thus preventing them to reach the copper catalyst filter and reduce its efficiency and at the same time trying to minimize their effect on the rubber gloves.
One the left hand side of the glove-box (not visible in the picture) there is also a built-in thermal evaporation system which can be used to create contacts for the devices without exposing them to air. Electrical characterization of FETs and SCLC diodes, at room temperature, can be performed inside the system using an in-house developed prober station.

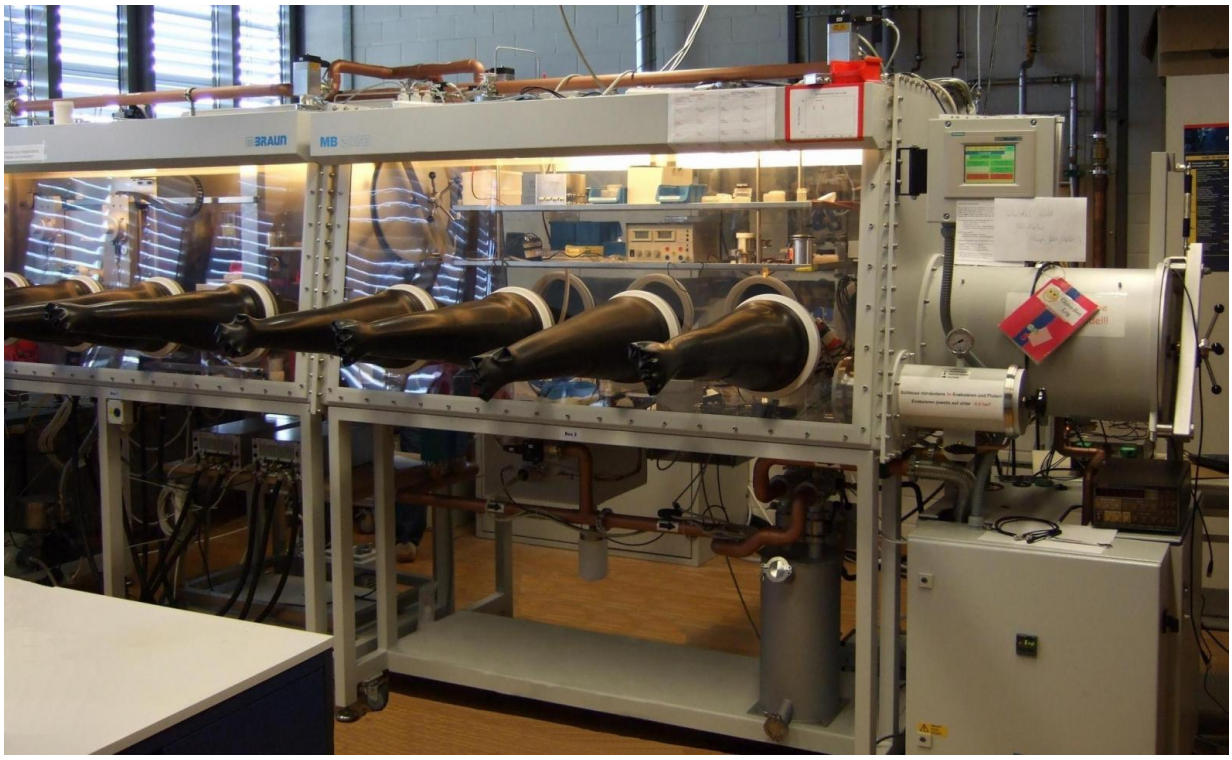

Figure 2.5: Glove-box system built by MBraun, type 200B

The temperature dependent electrical characterization of the FETs and SCLC diodes is done in a Cryovac cryostat (see figure 2.7) fitted with four DC probe heads (Suss), as seen in figure 2.6. The contacting of the samples is done via tungsten needles attached at the end of the DC probe heads, which is particularly good for establishing contacts on small areas, which is the case of the FET structures used in this work. Thus different devices from the same substrate can be probed in the same vacuum step.
The samples are transported from the glove-box to the cryostat in a load-lock system, in this way exposure to the air being avoided. The base pressure in the cryostat during measurements is in the range 10^{-6} Torr. The temperature has been typically varied between 200K and 400K. The temperature controller (Cryovac TIC 304-MA) is connected to the data aquisition PC (via GPIB) and the programs which has been developed for transistor measurements (Labview or Keithley's KITE) include an automatic temperature control loop, thus user intervention being minimized.
The characterization of the MIS and SCLC diodes is performed in the cryostat presented in figure 2.7 (b), with the help of Solartron Impedance/Gain Phase Analyser SI1260 coupled with Solartron high impedance interface 1296 in the case of MIS diodes and a Keithley SMU 2400 in the case of SCLC diodes. The commercial software 'Impedance Software' from Solartron (Solartron Analytical, Hampshire, UK) was used to record the characteristics of the MIS diodes; temperature controll for Cryovac TIC 304-MA was implemented.

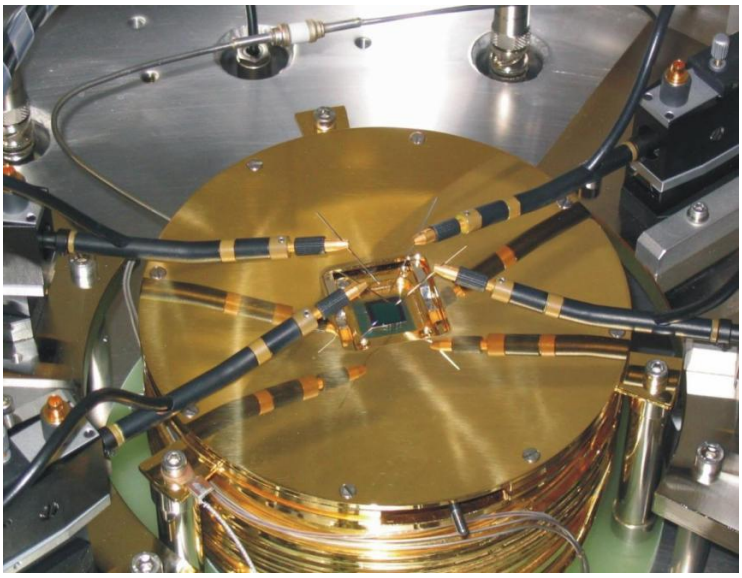

Figure 2.6: Sample holder of the Cryovac Konti-Cryostat used for electrical characterization of FETs

The cryostat used for FET measurements would not be proper due to the long connecting cables and the DC probe heads contacting method. In the case of the MIS/SCLC diodes these might induce undesired parasitic impedances/resistances and also the tungsten needles of the DC head probes might penetrate through the top electrode and semiconductor layer, altering the behavior of the devices.

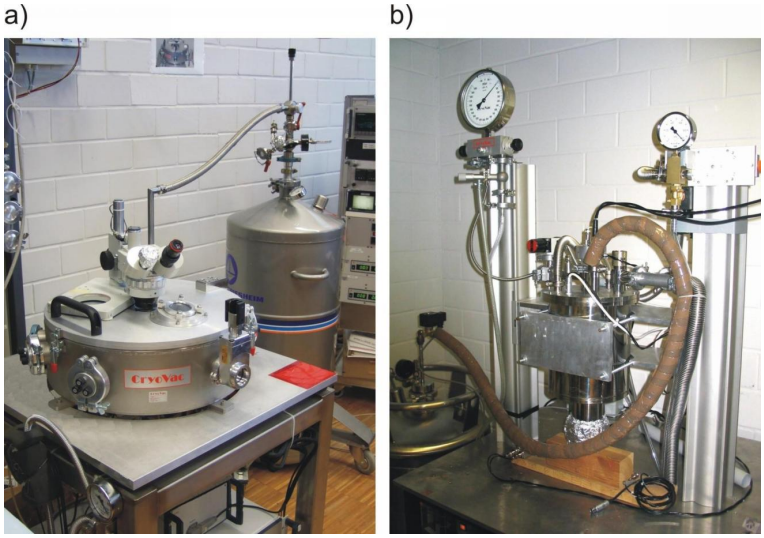

Figure 2.7: Cryostats used for electrical characterization of (a) FETs - Cryovac Konti-Cryostat and (b) MIS and SCLC diodes - Cryovac Konti-Cryostat IT Spektro

SCLC measurements

A schematic of the setup used in SCLC measurements is presented in figure 2.8. The sample-holder contacts each of the four devices. Measurements were performed in high vacuum 10^{-6} or better or under dry nitrogen, inside the cryostat, as mentioned above. Temperature dependence of the current-voltage curves has been investigated in the range 130-300K. All the measurements were performed in dark.

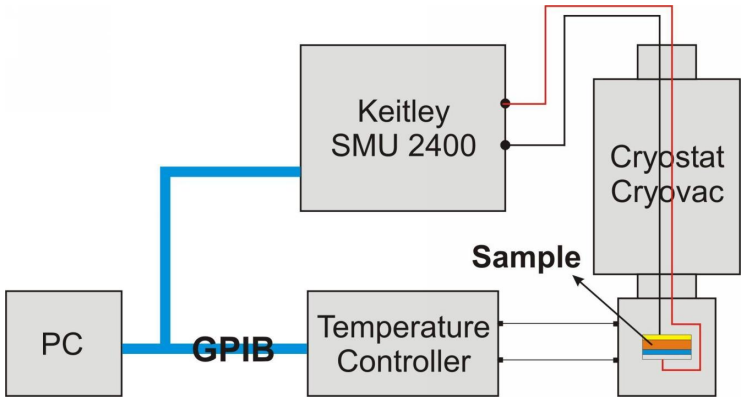

Figure 2.8: Schematic of the SCLC measurement setup.

Typical current density vs. the applied voltage characteristic for a 150nm thick P3HT SCLC diode is presented in figure 2.9. One can notice the quite high rectification of the device.

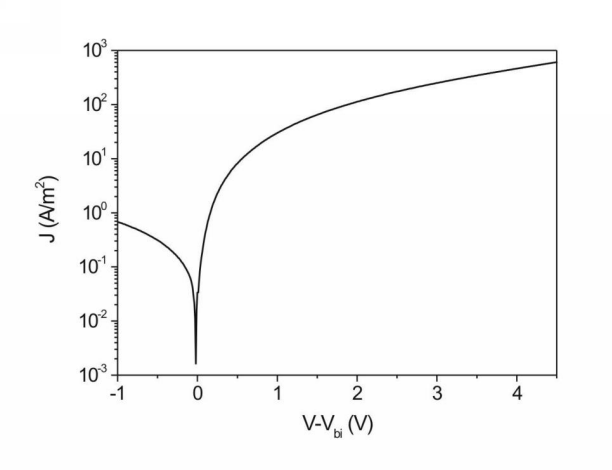

Figure 2.9: Arhenius plot of a typical $J-V$ characteristic of P3HT based hole-only diode; active area 16mm^2, semiconductor thickness 150nm and a built-in voltage estimated to 0.1V

The SCLC effect becomes important the moment the concentration of the injected carriers becomes larger than the thermal equilibrium concentration. In order to observe this behavior at least one well injecting contact is required in the device. In the case of the structure presented above the ITO/PEDOT contact is the good injecting contact. Usually the top-contacts are not perfect so one has to estimate the work function difference between the bottom and top contacts and correct the applied voltage with this value.

MIS diodes measurements

The impedance spectroscopy measurements on the MIS diodes were performed using the setup depicted schematically in Fig. 2.10. As in the case of the hole-only diodes the measurements were performed in high vacuum or under dry nitrogen, the difference between the two environments being negligible. Temperature was varied between 420K down to 100K. To completely analyse the MIS diodes two kinds of measurements are required: dependence of capacitance on frequency at fixed bias - $(C-f)$ and variation of capacitance with the applied bias at a fixed frequency - $(C-V)$.

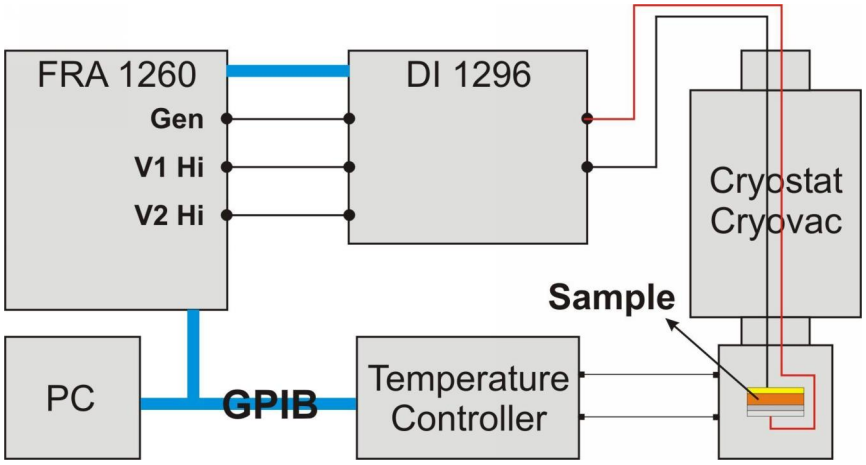

Figure 2.10: Schematic representation of the impedance spectroscopy setup.

In the Fig. 2.11 are presented the typical measured characteristics. The equivalent circuit can be regarded as a series of RC elements, corresponding to the oxide, semiconductor and the lead resistance as it will be discussed in the following chapter. The hysteresis in the $C-V$ characteristic would indicate the presence of interface defects.

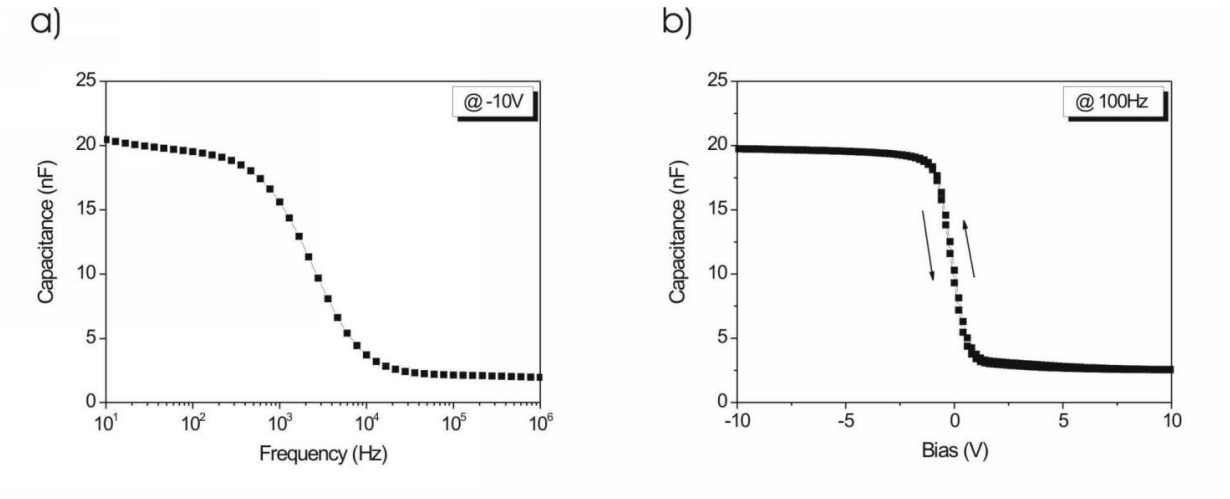

Figure 2.11: Example of (a) $C-f$ and (b) $C-V$ characteristics for an MIS diode fabricated on 50 nm SiO_2 with a thickness of the P3HT film of 246 nm and an area of 29 mm^2

Field-effect measurements

The schematic representation of the setup used in field-effect transistor measurements is presented in figure 2.12. All the measurements were performed in high vacuum, if not otherwise specified. The samples were contacted using tungsten needles connected to 3D micro manipulators controlled manually from outside the cryostat. The sensitivity of the setup was in the pA range using the Keithley SMUs and 100 fA in the case of the Keithley 4200 Semiconductor Characterization System.

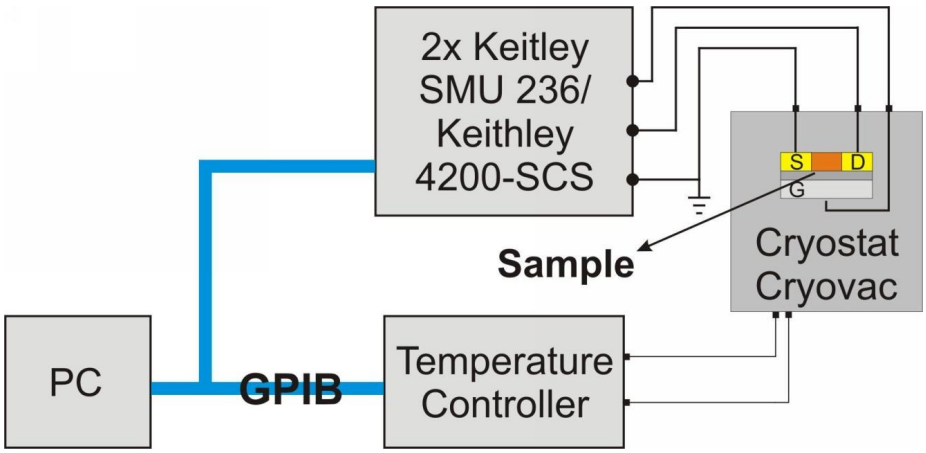

Figure 2.12: Schematic of the FET setup; contact needles, as seen in figure 2.6(b) are not represented.

Two different kind of electrical measurements were performed on the FETs - the output characteristics, I_d vs. V_d at $V_G = ct$ and transfer characteristics, I_d vs. V_g at $V_D = ct$. Typical curves are presented in figure 2.13. One can notice the saturation of the drain current, in the output characteristics, and that it scales with the gate bias as predicted by the equations presented in chapter 1. At the same time the transfer characteristics show a high on-off ration, high subtreshold slope and switch-on voltage at slightly negative voltages, which would mean there is a slight accumulation of positive charge at the interface. The dependence of the output and transfer characteristics on the temperature was also measured, temperature variation being controlled with a Cryovac TIC-304-MA temperature controller.

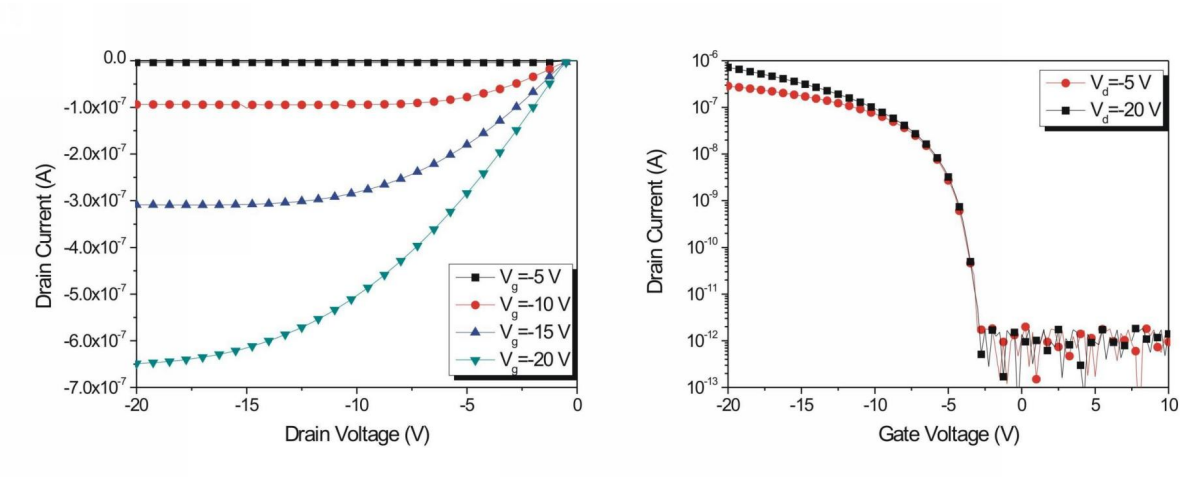

Figure 2.13: Example of output and transfer characteristics measured for an FET based on P3HT (100 nm) with gate insulator 200 nm SiO_2 , channel width 1000 μm and channel length 5 μm

Contact Angle Measurements

The contact angle measurements were performed in a setup like the one depicted in figure 2.14(a). The contact angle of a liquid is a measure of the number of disrupted bonds at the surface of a solid. Disrupted bonds at the surface of the insulator can drastically affect the behavior of field-effect devices, by inducing charge accumulation at the interface which shifts the output and transfer characteristics. For this reason it is very important to measure the contact angle of a liquid on a surface, in order to correlate its value with the measured characteristics. Deionized (DI) water was used to determine the contact angle on the substrates used in the FETs and MIS diodes. The shape of the μL water droplet was recorded via a camera attached to the ocular of the microscope; a typical image being shown in figure 2.14(b).

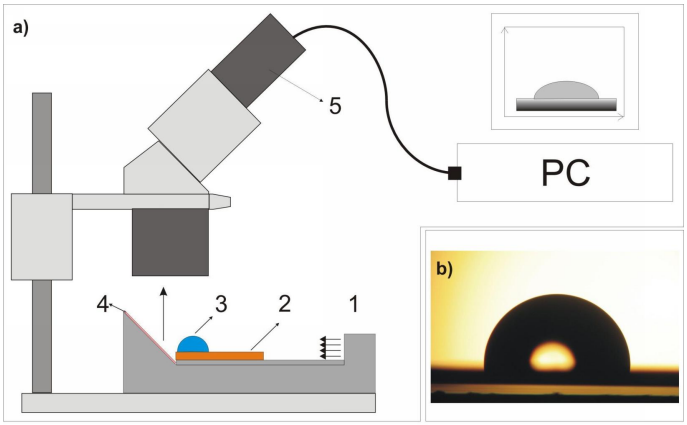

Figure 2.14: Liquids contact angle measurement setup: 1 - Light source, 2 - Sample, 3 - μL droplet, 4 - 45° mirror, 5 - ocular camera

Based on the height and width of the droplet the contact angle has been determined according to the next formula:

$$\theta = 2\text{arctan}\left(\frac{2Z}{D}\right) \tag{2.1}$$

where θ is the contact angle of the water on the given surface, Z is the height of the droplet and D is the diameter of the droplet at the interface between the liquid and the surface. The contact angle is related to the surface energy, thus the higher the surface energy of the substrate the smaller the contact angle.

X-Ray Diffraction Measurements

Structural properties of the P3HT films were investigated by grazing incidence X-ray diffraction (GIXRD). With this method the size and orientation of the crystallites were determined for films spin-coated from solutions with different solvents and also the annealing effect on the crystallite size and orientation was measured. The schematic of the GIXRD measurement is presented in figure 2.15.
The measurements were performed with a Siemens D-5000 diffractometer in grazing incidence geometry. The angle between the incident beam and the sample was 0.03° and the wavelength 1.54 $\mathring{A}$. The incident angle is fixed and the diffraction spectra is recorded by the scan of the detector along the 2θ angle. The background was extracted from the recorded spectra. The lattice constant, a, was determined from the peak positions using the Bragg condition:

$$2 \cdot a \cdot sin(\theta) = n \cdot \lambda \tag{2.2}$$

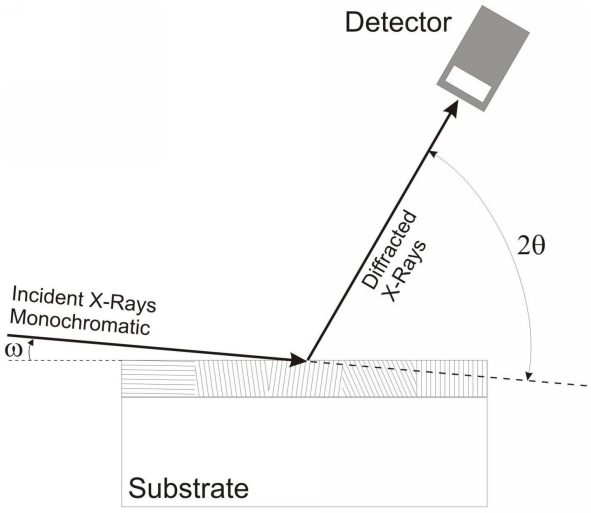

Figure 2.15: Schematic of grazing incidence x-ray diffraction setup

In polycrystalline materials, the crystallite size l can be obtained from the Scherrer equation using the relation between full width at half maximum FWHM (2θ) of the diffraction peak and the diffraction angle 2θ

$$FWHM(2\theta) = 0.94 \cdot \lambda / l \cdot cos(\theta) \tag{2.3}$$

In polymers, however, the FWHM is usually dominated by variations in interplanar spacings. Thus the width of the XRD peaks can only give a qualitative hint to the degree of crystallinity.

Chapter 3

Analysis

3.1 The Organic MIS Diode

3.1.1 Introduction

The analysis of C-f and C-V characteristics of an MIS diode gives us informations about different electrical properties of the insulator and of the semiconductor, as well as information about the electrical properties of the interface between the two. By combining the results from the capcitance-frequency and capacitance-voltage characteristics one can also extract other properties, like the out-of plane carrier mobility in the semiconductor, which would otherwise not be possible to determine from one single type of measurement.

3.1.2 The capacitance-frequency dependence

Usually, in an MIS diode, one measures the variation of the impedance, which is a complex quantity, with the frequency, applying at the same time a bias on the structure so that the MIS diode is found in the accumulation regime. The MIS diode can be described, in first approximation, by a parallel 2RC circuit. The impedance (Z) and admittance (Y) for such a circuit are given by:

$$Z = Z_R + i \cdot Z_I \tag{3.1}$$

$$Y = \frac{1}{Z} = G + i \cdot \omega C \tag{3.2}$$

where Z_R is the real part and Z_I the imaginary part of the impedance, G the conductance and C is the capacitance. Using the relation, $Y = Z^{-1}$, between the admittance and impedance one can calculate the the conductance and the capacitance as a function of the measured real and imaginary part of the impedance. The affirmation that the MIS diode can be described by a parallel 2RC circuit is based on the its structure, as one can consider the oxide as one RC element and the semiconductor layer as another. A simple comparison between the measured capacitance response and the simulated one can be seen in the next

figure, for a P3HT MIS diode with an area of 28.6 mm^2, layer thickness of 280nm and oxide thickness of 50nm:

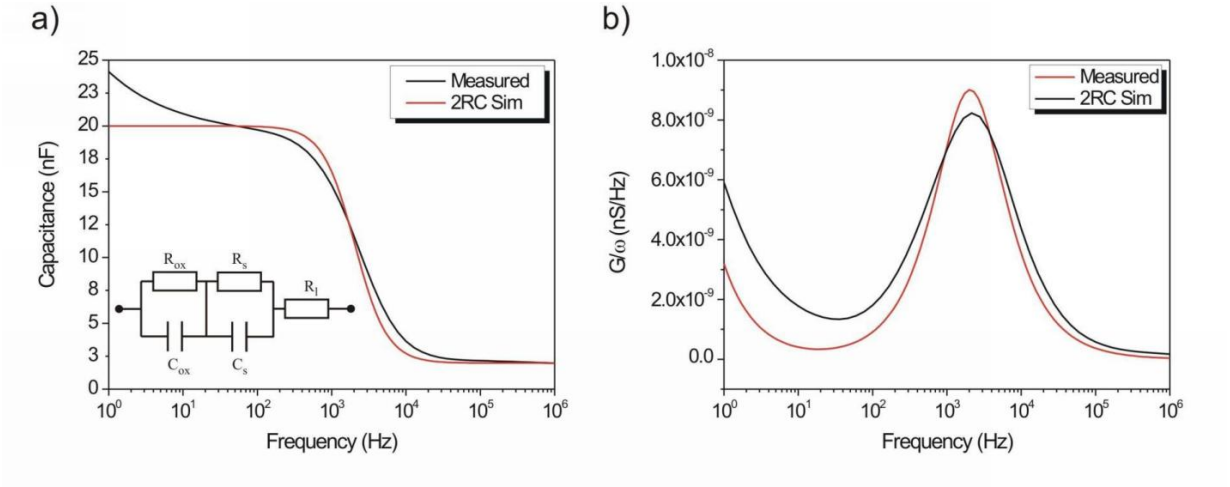

Figure 3.1: Comparison between $C-f$ and $G/\omega-f$ for a real MIS diode and a 2RC circuit; the inset shows the schematics of the 2RC circuit

The step in $C-f$ seen in figure 3.1(a), located at about 2.5kHz, can be explained considering the finite semiconductor bulk conductivity which sets the upper limit for the frequency up to which the injected majority carriers can follow the applied a.c. frequency and reach the accumulation layer at the semiconductor-insulator interface. This relaxation step and its associated relaxation frequency gives us information about the transport properties in the out off-plane direction, with respect to the oxide surface. From the $C-f$ characteristic it is quite difficult to extract the value of the relaxation frequency. For this reason a different representation of the data is required. The relaxation frequency can be extracted from the dependence of the loss (conductance divided by the angular frequency) $-G/\omega$ on frequency. It can be seen in figure 3.1(b) that such a characteristic has a peak whose maximum corresponds to the relaxation frequency. Both previously mentioned representations depend on the real part of the impedance, which in turn is proportional to the imaginary part of the dielectric constant and thus to the conductivity of the semiconductor.
From the $C-f$ characteristic, measured in the accumulation regime, figure 3.1(a), it can be noticed that the capacitance value at intermediate frequencies is equal to the oxide geometrical capacitance, 20nF in this case, as all the charge carriers can follow the applied signal, while at higher frequencies it drops to approximatively 2 nF. The increase of the capacitance at lower frequencies over the oxide capacitance value is due to charge spreading beyond the area defined by the top contact [57]. This effect can be associated to a high in-plane mobility, as it will be looked upon in more detail in a following chapter.
For a simple equivalent circuit of the MIS diode, with only one RC element describing the semiconductor, and considering that the resistance of the oxide is much larger than the

one of the semiconductor layer, the corresponding relaxation time $\tau_R = (2\pi f_R)^{-1}$ directly yields the semiconductor bulk resistance, R_S [26]:

$$\tau_R = R_S(C_{ox} + C_S) \tag{3.3}$$

The value of C_{ox} is taken from the constant value of the capacitance at low frequencies and C_S is determined from the constant capacitance at higher frequencies considering that the value in this region is the series of oxide and semiconductor capacitance:

$$C_{HF}^{-1} = C_{ox}^{-1} + C_S^{-1} \tag{3.4}$$

The value of the relaxation frequency is determined from the maximum of the $G/\omega - f$ dependence. Regardless of the circuit used to describe the MIS diode this approach gives a good value for the relaxation frequency, within 10% from the actual value, as determined by fitting the loss peak with the corresponding analytical expression.
The real MIS diode, despite the simple geometry, can have a quite complicated internal structure. This can be regarded a succession of layers corresponding to the insulator, the interface between insulator and semiconductor and the semiconductor itself. Sometimes, due to different processing conditions additional layers could be present, thus the behavior of the device getting more complex, leading to equivalent circuits with three or more RC elements. It has been shown by others [27] that an additional RC element for the accumulation layer has to be included. More sophisticated models have also been suggested recently [26]. The next figure shows the equivalent circuit when the interface between semiconductor layer and the silicon oxide is considered separately.

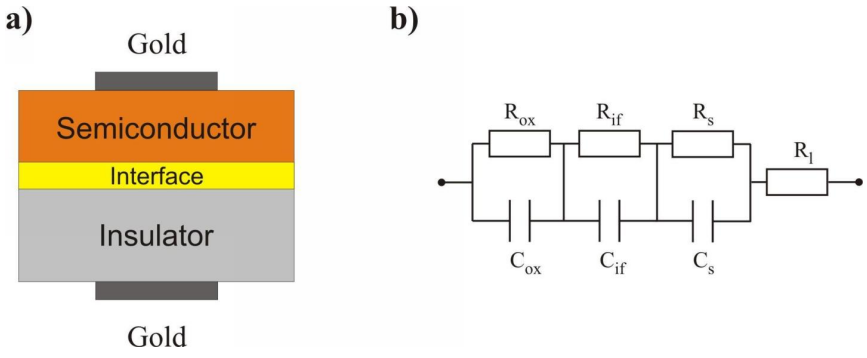

Figure 3.2: MIS diode schematic and equivalent circuit, considering also the interface layer and contact resistance

The next figure shows a comparison between the measured data and 2RC, 3RC models respectivelly.

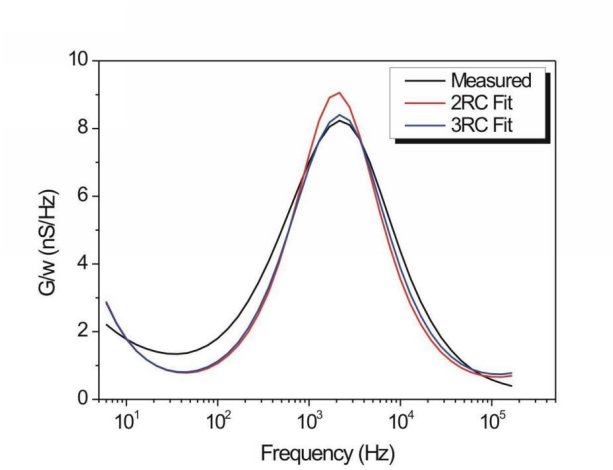

Figure 3.3: Comparison between measured $G/\omega - f$ and 2RC, 3RC equivalent circuits, respectively, for the MIS diode presented in figure 3.1

It can be noticed that the 3RC model, as expected, gives a better description of the MIS behavior compared to the 2RC equivalent circuit. The quantity of interest is the relaxation frequency, given by the expression (3.3). The corresponding values are determined using the fit parameters in the following table:

Table 3.1: Fit results of $G/\omega - f$ with 1RC and 2RC equivalent circuits, respectively

Model	$R_{ox}(\Omega)$	C_{ox}(F)	$R_b(\Omega)$	C_b(F)	$R_{if}(\Omega)$	C_{if}(F)	$R_l(\Omega)$
2RC	$9.34 \cdot 10^6$	$2\ 10^{-8}$	3436.78	$2.2 \cdot 10^{-9}$	-	-	136.86
3RC	$9.47 \cdot 10^6$	$2\ 10^{-8}$	2978.25	$2.2 \cdot 10^{-9}$	670.01	$1.69 \cdot 10^{-7}$	166.8

The corresponding relaxation frequencies are τ_{2RC}=2086 Hz and τ_{3RC}=2407 Hz, while the frequency corresponding to the maximum of the loss peak is at 2154 Hz. It can be seen that the difference between the simpler model presented in figure 3.1 and a more complicated one, like the one suggested by Scheinert and Paasch, figure 3.2(b), will lead to almost equal results, the difference being in the range of 10%. Thus in the following chapters the analysis will be performed using the frequency corresponding to the maximum of the loss peak as the relaxation frequency.

3.1.3 The capacitance-voltage dependence

The capacitance-voltage dependence of p-type organic MIS diodes presents two distinct regimes : accumulation at negative bias and depletion at positive values, respectively. The value of the capacitance corresponding to the oxide geometrical value in the first regime and to the series sum of insulator and organic semiconductor geometrical capacitances in the second. The absence of inversion is explained by the extremely long generation

times of the minority carries in the wide-gap organic semiconductors [28]. In between the two regimes there is a transition region whose properties are determined by the doping concentration in the semiconductor. The behaviour of the capacitance in this transition region is described well by the following relation, developed by Schottky and Mott:

$$\frac{1}{C^2} = \frac{2(V_G - V_{FB})}{\epsilon_0 \epsilon_S q N_A A^2} \tag{3.5}$$

Thus N_A can be extracted from the plot of $1/\mathrm{C}^2$ versus gate bias according to the following expression:

$$\frac{\partial}{\partial V}(C^{-2}) = \frac{2}{\epsilon_0 \epsilon_S q N_A A^2} \tag{3.6}$$

where ϵ_0 is the permittivity of vacuum, ϵ_S the dielectric constant of the semiconductor, A is the area of the device, V_G is the gate bias, V_{FB} is the flat-band voltage and N_A is the doping concentration in the semiconductor.
In the following we will compare the results obtained from the fit of the $C-V$ curves with the model for the deep depletion capacitance and the Schottky-Mott analysis. At the same time the value of the flat-band voltage will be determined in both cases. In the next figure both kinds of analysis are applied on the $C-V$ characteristic of a P3HT MIS diode (the same as in the previous paragraph).

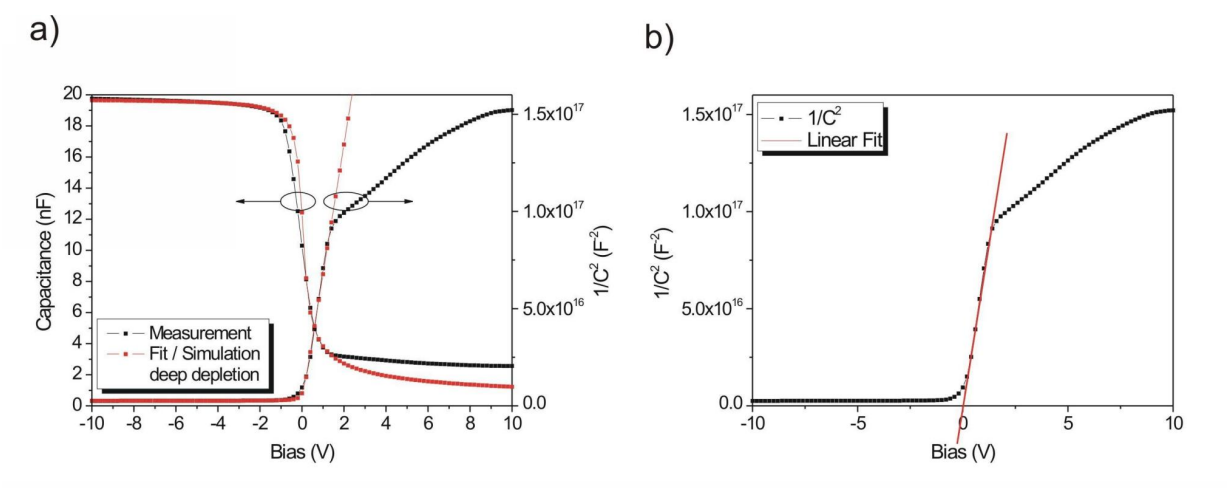

Figure 3.4: Fit of C-V curve of a P3HT MIS diode using (a) Deep depletion capacitance (the measured capacitance and the fitted capacitance are shown) and (b) Schottky-Mott analysis

The fit using the expression of the deep depletion capacitance is done by solving numerically the equation (1.26) for the surface potential in each point and at the same time applying a nonlinear least square fitting algorithm on the expression (1.25) of the deep

depletion capacitance. The parameters of the fit are the doping concentration N_A and the flat-band voltage V_{FB}. The intrinsic doping, n_i, is taken as $10^9 cm^{-3}$. The fit was performed only on a limited range of the curve, where the transition between the depletion and accumulation takes place. It can be noticed the good quality of the fit in this region for both types of analysis. The resulting values are also in very good agreement as seen in the next table:

Table 3.2: Fit results of a P3HT MIS diode with deep depletion capacitance and Schottky-Mott analysis

Model	N_A (cm^{-3})	V_{FB} (V)
Deep depletion	7.98 10^{15}	0
Schottky-Mott	8.56 10^{15}	0

In figure 3.4(a) the simulated deep depletion $C-V$ curve is shown, in the measured bias range, using the doping and flat-band voltage determined above. It can be remarked that the agreement to the measured curve is quite good, until the beginning of the depletion at 1.5V. The deviation from the original curve at values of the gate bias larger than 1.5V can be ascribed to a non-uniform doping throughout the entire layer and/or interface between semiconductor and top gold contact.
With the knowledge of the doping and of the resistance of the bulk of the semiconductor from equation (3.3) one can now calculate the charge carrier mobility $\mu_\perp$, perpendicular to the insulator via:

$$R_S = \frac{d_S}{qN_A\mu_\perp A} \quad \text{leading to} \quad \mu_\perp = \frac{d_S}{qN_A R_S A} \tag{3.7}$$

where R_S is the semiconductor resistance, extracted from the C-f characteristic, d_S the semiconductor thickness, N_A the bulk doping, q the elementary charge and A the area of the device.

3.2 Field-effect transistors

Usually the parameters of field-effect transistors are extracted from the transfer characteristics, both in the linear and saturation regime. From equation (1.35) and (1.36) the dependence of I_D in the linear regime and of $\sqrt{I_D}$ in the saturation regime, respectively, on the gate bias are both linear. In figure 3.5 an example of transfer characteristics of a P3HT based FET is shown together with linear fits.
The field effect mobility can be extracted from the transconductance $\partial I_D/\partial V_G$ in the linear regime and from the $\partial\sqrt{I_D}/\partial V_G$ in the saturation regime, the slope of the linear fits being proportional to the mobility. From the intercept value the parameter V_T can be determined. In this case the values of the mobility and threshold voltage are $\mu_{lin} = 2.1 \cdot 10^{-3} cm^2/Vs$, $V_{T,lin}$=-3.5V and $\mu_{sat} = 2.7 \cdot 10^{-3} cm^2/Vs$, V_T, sat=-5.5V in the linear and saturation regime, respectively.

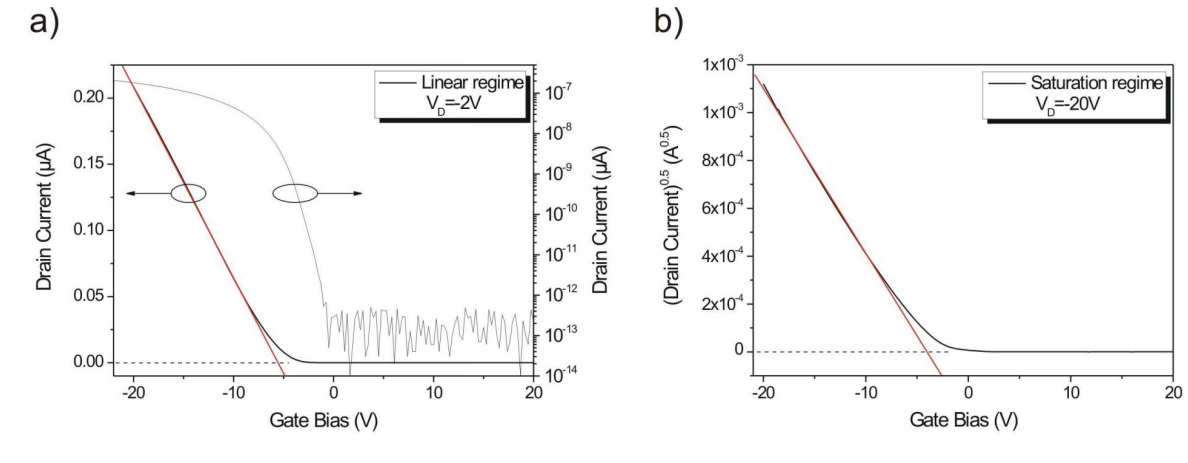

Figure 3.5: Example of transfer characteristics together with linear fit (red line); the position of the threshold voltage is given by the intersection of the fit line with the gate bias axis zero current (dotted black line); sample parameters are d_{ox}=200nm, L=5 μm and W=1000 μm

Nonetheless one has to keep in mind that the field effect mobilities thus obtained might differ from reality due to the simplifying assumptions used in the determination of the equations describing the dependence of the drain current on the gate bias, on the one hand, and on the other hand due to the contact resistance between the semiconductor layer and the source/drain metal electrodes. Another factor which can influence the shape of the transfer curves, rendering them non-linear, can be due to the dependence of the mobility on the charge carrier density. Detailed analysis of this factors and other will be made in the following chapters.

3.3 Space Charge Limited Diodes

The analysis of the $J-V$ characteristics for the SCLC diodes is mainly based on numerical simulations with different distributions of traps, as it was discussed before. But firstly, as mentioned in chapter 1 the built-in voltage has to be overcome in order for the device to operate. An example is presented in figure 3.6.

At room temperature the current density is supposed to follow a quadratic dependence on the voltage $J \sim V^2$. The work function difference between gold and PEDOT:PSS which represent the injecting contact, according to values from literature is in the range of 0.1 eV, which fits very well with the estimation presented above for the built-in voltage. If one corrects the voltage values considering V_{bi}=0.1V then the fit of the J-V gives the value two for the slope of the current density vs. voltage curve.
As mentioned above the analysis of the J-V characteristics is based on numerical simulation. This means that one has to choose a model for the charge carier transport through the diode and then generate data based on this model. In our case, as it will be seen in chapter

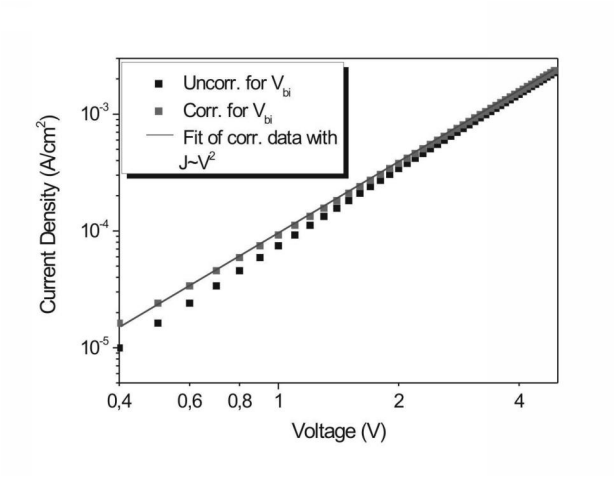

Figure 3.6: Example of uncorrected (open squares) and corrected (filled squares) J-V characteristic of a P3HT SCLC diode with a thickness d=400 nm

7, the model chosen assumes that the trasport takes place in a gaussian distribution of traps. As the number of parameters is not large and normally the range of value where the right parameters lie is not too wide, through an iterative procedure the values of the parameters can be determined using the measurements at different temperatures.

Chapter 4

Influence of gate dielectrics

4.1 Introduction

In the following the electrical properties of organic MIS diodes and field-effect transistors with different insulators in addition to the silicon oxide will be analysed. There are a few reasons why one would use other insulators than silicon oxide for the fabrication of such devices. One is the ability to build FETs and MIS diodes on different substrates, not only silicon, even on flexible ones. Thus organic insulators are a good approach as they are virtually compatible with any substrate. Another advantage might come from the use of materials with higher dielectric constants in order to reduce the operation voltage. This can be done by using, for example, aluminum oxide which has a dielectric constant three times higher than silicon oxide. There are still a few problems which have to be overcome regarding the quality of these alternative insulators, as it will be shown later.

4.2 Melamin based insulator

A comparison between two types of metal–insulator–semiconductor (MIS) devices is presented. One structure is based on Si/SiO_2 substrates, the other one uses indium–tin oxide (ITO) coated glass substrates covered with a solution processed polymer as gate insulator. In this way we can directly compare the effect of the organic–organic interface on the electrical properties of MIS diodes. Capacitance-frequency and capacitance-voltage curves in the dynamic regime have been measured. Field–effect transistors have not been successfully prepared with this polymer insulator. The reason for this lies in the lithography process, due to the use of solvent like acetone which seems to damage the organic insulator layer, thus leading to high leakage currents. Another reason is related to the diffusion of gold into the layer during the evaporation of the source and drain contact, which again leads to high leakage currents.
The inorganic MIS have been fabricated on highly p-doped silicon wafers with 50 nm of thermally grown silicon oxide and the organic type on indium-tin oxide (ITO) coated glass using an organic aromatic oligomeric resin capable of thermal or photo crosslinking in a

butanol based formulation (obtained from Merck), its formula shown in the next picture.

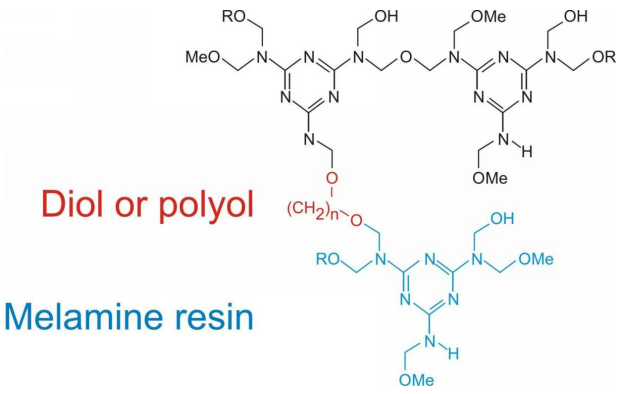

Figure 4.1: Formula of Merck melamine based resin

The organic dielectric was spin-coated from solution resulting in a film thickness of about 600 nm followed by thermal crosslinking (5 h at 340 K). The cross-linking takes place between the hydroxil and amino groups. The frequency dependence of the dielectric constant can be seen in figure 4.2. In both cases smooth, homogenous P3HT films of about 150 nm thickness were spin-coated from 5 wt.% solution in toluene, at 1500 rpm. There was a subsequent thermal treatment at 340K for 10 h. After this annealing step rectangular contacts with an area of 30mm^2 for Si substrates and about 8mm^2 for ITO substrates were produced by thermal evaporation of gold through a shadow mask. The solution processing of both, the melamine insulator and P3HT, was performed in a nitrogen-filled glove-box system with partial pressures of oxygen and water below 1 ppm.

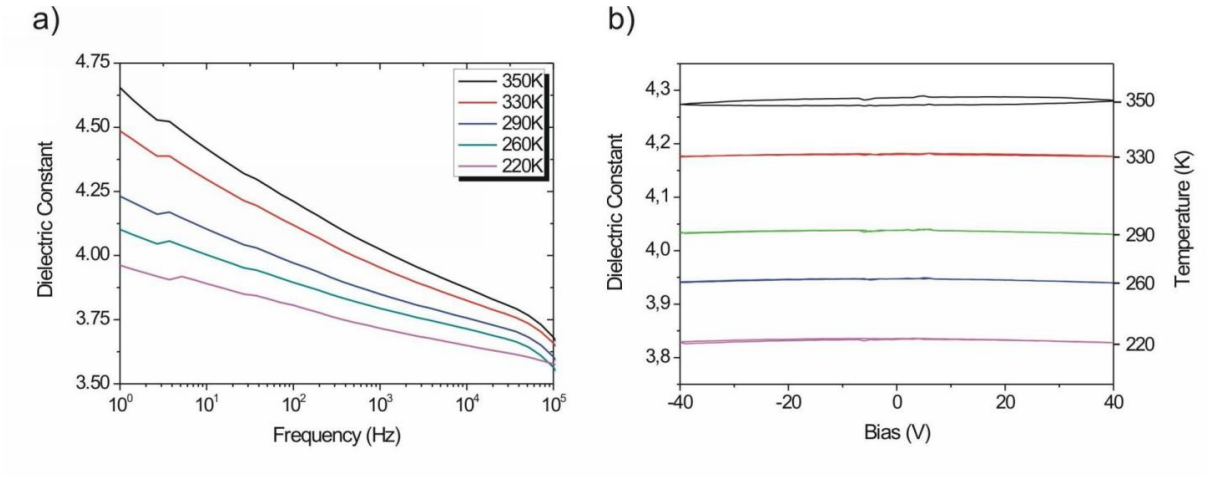

Figure 4.2: Dielectric constant of a Au/melamine insulator/ITO structure for different temperatures; a) frequency dependence at zero bias, b) bias dependence at 511Hz

It can be noticed that the dielectric constant has values in the range 3.5-4.5, depending strongly on frequency and temperature, but it has no dependence on the applied bias. The next figure presents the comparison between the C-f and C-V characteristics of the inorganic and organic diodes:

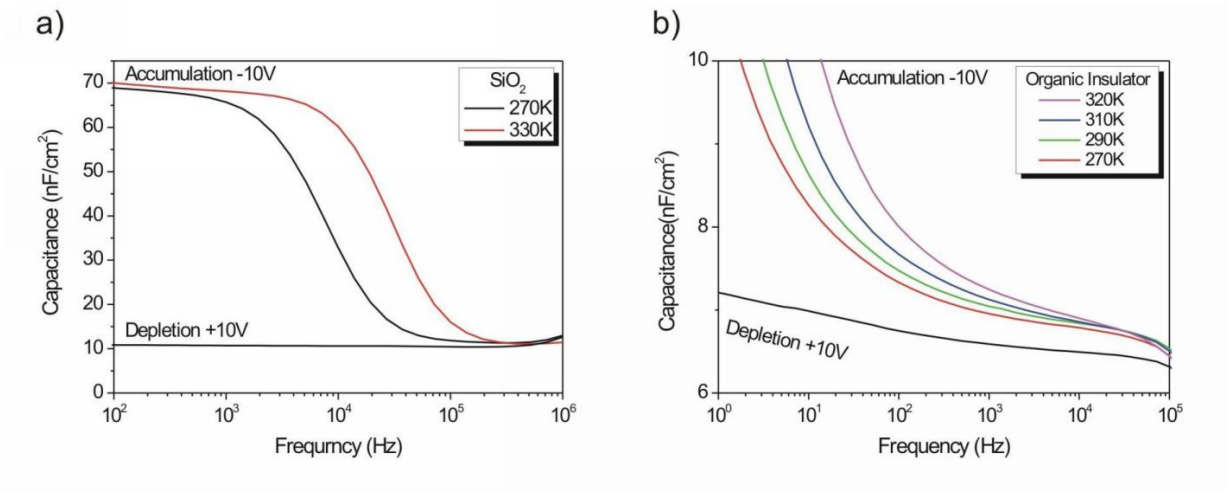

Figure 4.3: Comparison between capacitance-frequency dependence of a SiO_2 (a) and a melamine insulator (b) based MIS diode with P3HT as semiconductor, respectively

In contrast to the structure on silicon oxide the capacitance of the mealmine-based MIS, in accumulation and depletion, is temperature dependent and shows a pronounced increase at low frequencies. The main reason for this behavior is that the capacitance of the melamine insulator alone is already frequency and temperature dependent. In this case due to the increase of the capacitance at low frequencies it is difficult to define a relaxation frequency. For this reason the dependence of loss on frequency is not shown. We can nonetheless estimate that the relaxation frequency in this case is lower than the one for the MIS diode with SiO_2, which would suggest that the structural ordering of the P3HT is not so good in this case, thus leading to a smaller perpendicular mobility. For the sake of consistency the capacitance - voltage dependence was measured as in the case of the silicon oxide at 511Hz, as it can be seen in figure 4.4.

The $C-V$ characteristics for the SiO_2 diode show the typical step-like transition from accumulation at negative bias to the lower capacitance value in depletion, at positive bias values. It is noteworthy that at 270K the two bias sweeps are indistinguishable and even at 330K there is only a slight difference between the increasing and decreasing sweep. The values of the doping, determined from the Schottky-Mott analysis are about 10^{16} cm^{-3} in the temperature range from 270K to 330K, in agreement with previous studies [31],[32]. From the maximum of loss-frequency dependence (not shown here), as described in the previous chapter, the relaxation frequency was extracted (7kHz at 270K up to 27kHz at 330K). Thus the perpendicular charge carrier mobility is determined to be in the range 1 to $3 \cdot 10^{-5}$ cm^2/Vs, being comparable to the mobility obtained from space-charge limited

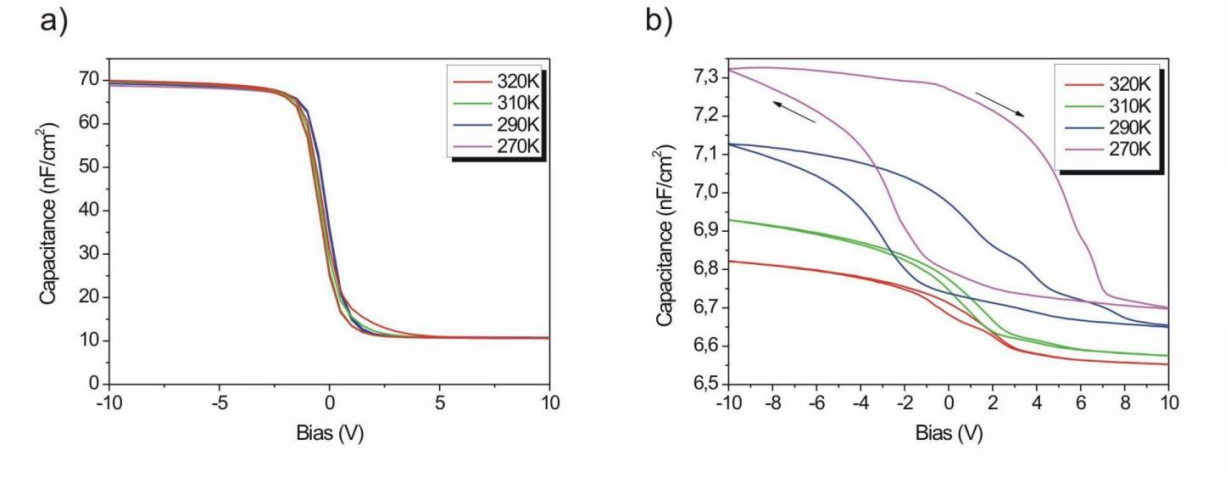

Figure 4.4: Comparison between capacitance-bias dependence of an SiO_2 (a) and melamine insulator (b) based MIS

current diodes [33].
Comparing the SiO_2 and the melamine insulator diodes, one can notice immediately the big differences between the two kinds of devices [30]. While in the MIS diodes on SiO_2 case there is almost no hysteresis, for the melamine insulator this can be very large, at the same time depending strongly on the temperature. Taking into consideration also the dependence of the dielectric constant on the temperature it is quite difficult to estimate the value of the doping. Nonetheless an approximate value of 10^{17} cm^{-3} was determined, which is almost one order of magnitude higher than in the case of the SiO_2 MIS diode, suggesting that the thermally cross-linked insulator could be responsible for additional doping by diffusion of a mobile species into the P3HT layer. This hypothesis is also suggested by the dependence of the hysteresis of the CV curves on temperature, as seen in figure 4.4(b) and explained in more detail below. Regarding the hysteresis it can be noticed that it is quite small at low temperatures but grows rapidly with increasing temperature and is as large as about 10V at 330 K. The strong increase is a first hint that mobile ions could be responsible for this behavior. Further support for this hypothesis comes from a bias-temperature stress experiment (see figure 4.5).

Depending on the sign of the bias the mobile ions will be repealed or attracted to the interface between the semiconductor and insulator, thus increasing or decreasing the amount of charge present at the interface and implicitly the value of the flat-band voltage. At 350K the device was stressed with different biases (±40 V) for 60 min. While maintaining the bias the temperature was lowered down to 220K where the already measured hysteresis is very small, which means that the mobility of ions is low; then a bias sweep was performed having as starting point the bias value which was used for stressing the device. As can be seen there is a huge difference between the two curves for +40 and -40V, respectively. Assuming that there are mobile ions in the insulator the observed behavior can

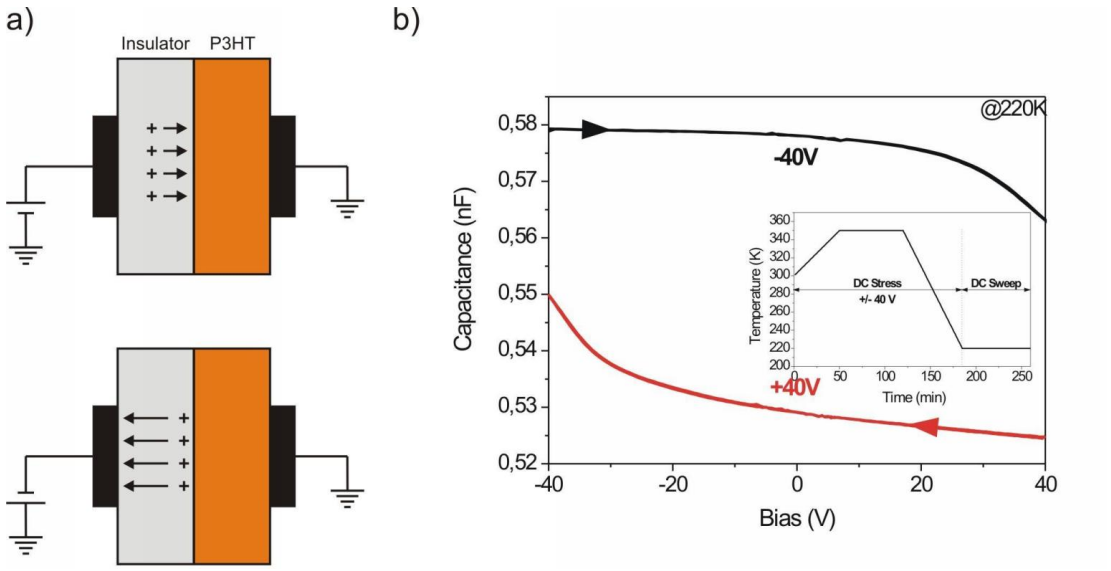

Figure 4.5: Bias stress experiment of an MIS diode with polymeric insulator. a) Schematic of the process and b) capacitance-voltage curves measured after stress at 220K; the inset shows how the bias was applied

be explained as follows. At high temperature the mobile ions, depending on the bias sign, are moving toward or away from the semiconductor insulator interface thus modifying the flat band voltage and consequently the shape of the CV curves. This behavior together with the hysteresis dependence on temperature and the comparison with the SiO_2 samples allows us to conclude that mobile ions are residing in the organic insulator. A possible origin could be the initiator necessary for starting the crosslinking process, by providing mobile charged species of one type while the countercharge located on the polymer chains is immobile.
The density of mobile ions Q_m can be calculated from the shift of the flat-band voltage ΔV_{FB} between different bias sweep directions as [34]

$$Q_m = C_{ins}(V_{FB}^{+} - V_{FB}^{-}) \tag{4.1}$$

Strictly speaking, the flat-band voltage V_{FB} should be determined at the flat-band capacitance which is a series of insulator and Debye capacitance [34]. However, the flat-band capacitance is not used here because there is a huge temperature and frequency dependence of the insulator capacitance. Instead we use as an estimate for ΔV_{FB} the width of the hysteresis at half value between minimal and maximal capacitance in the CV curve for each temperature. The resulting amount of charge increases with temperature from less than 10^{10} cm^{-2} at 280K to almost 10^{11} cm^{-2} at 320 K, as it can be seen in figure 4.6.

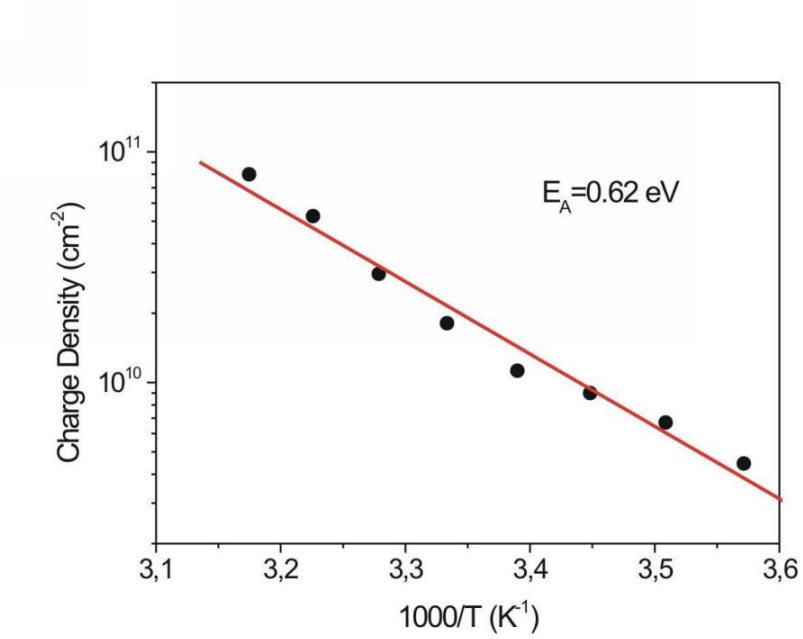

Figure 4.6: Arhenius plot of charge density determined from the width of hysteresis in Fig. 4.4(b) for the calculation of the activation energy of mobile ions

From the plot above an activation energy of 0.62eV is determined. This large value of the activation energy (varying between about 0.6 and 0.8 eV on different samples) is also supporting the assumption that mobile ions are the origin of hysteresis in MIS diodes using a cross-linked polymeric gate insulator.

4.3 PMMA as insulator

PMMA (poly(methyl methacrylate)) is another organic insulator which has been used to prepare MIS diodes and analyze their behavior. There would be a few advantages to use it as a gate insulator as it is available in large quantities with high purity grades, it withstands low temperatures, down to 170K or even below and it is transparent and water insoluble, thus providing a good barrier against moisture. In the next paragraphs PMMA and PMMA based MIS diodes will be analysed by means of impedance spectroscopy. In this case the preparation of working FETs was also not possible due to reasons similar to the case of the melamine insulator.
The devices were fabricated on patterned ITO glass, via spin-coating of a solution of 5 % PMMA in chloroform, at 5000 rpm, followed by drying, first on the hot-plate at about 60°C for one hour and then for another hour in vacuum at 100°C. The PMMA layers prepared in this way are smooth, without pinholes and have a typical thickness in the range of 500-550 nm. In order to determine the dielectric constant of the PMMA gold contacts have been

evaporated on top of the layers, defining capacitors with an area of about 16 mm^2. The MIS diodes were prepared by subsequently spin-coating a solution of P3HT in toluene (2% wt. at 3000 rpm) solution on top of the PMMA dielectric. The thickness of the P3HT layers being in the range 250-275 nm. Top gold contacts have been evaporated in order to complete the MIS diode fabrication; the active area being also about 20 mm^2.
The dielectric constant of the PMMA layers and its dependence on frequency is shown in figure 4.7.

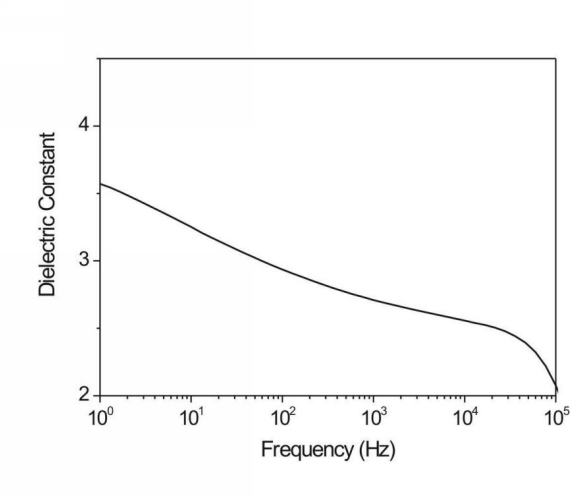

Figure 4.7: Dependence on frequency of the dielectric constant of PMMA

It can be noticed that the dielectric constant of PMMA has a moderate dependence on frequency, its value being in the range of 2.5-3.5, which is a little bit lower than expected - 2.9 instead of 3.6 at 100Hz, and it follows the typical descending trend [35]. The influence of this frequency dependent dielectric constant will be seen also in the $C-f$ characteristics of the MIS, presented below, as in the case of the melamine based insulator discussed in the previous section.
The $C-f$ dependence of the PMMA based MIS diodes (figure 4.8) shows the typical relaxation step and the relaxation frequency is relatively well defined. The increase of the capacitance at low frequencies, as mentioned before, is due partly to the insulator and can be partly due the high value of the in-plane charge carrier mobility of the P3HT (see chapter 6), which leads to a spreading of the charge around the active area defined by the top contact. This assumption is based on the fact that after each annealing step the increase of the capacitance is stronger than before. Another important effect of the annealing is the shift of the relaxation frequency (≈ 50 times) toward higher values. As the relaxation frequency is directly proportional to the value of the perpendicular mobility, this means that the out-of plane charge carrier mobility is getting higher after each annealing step.

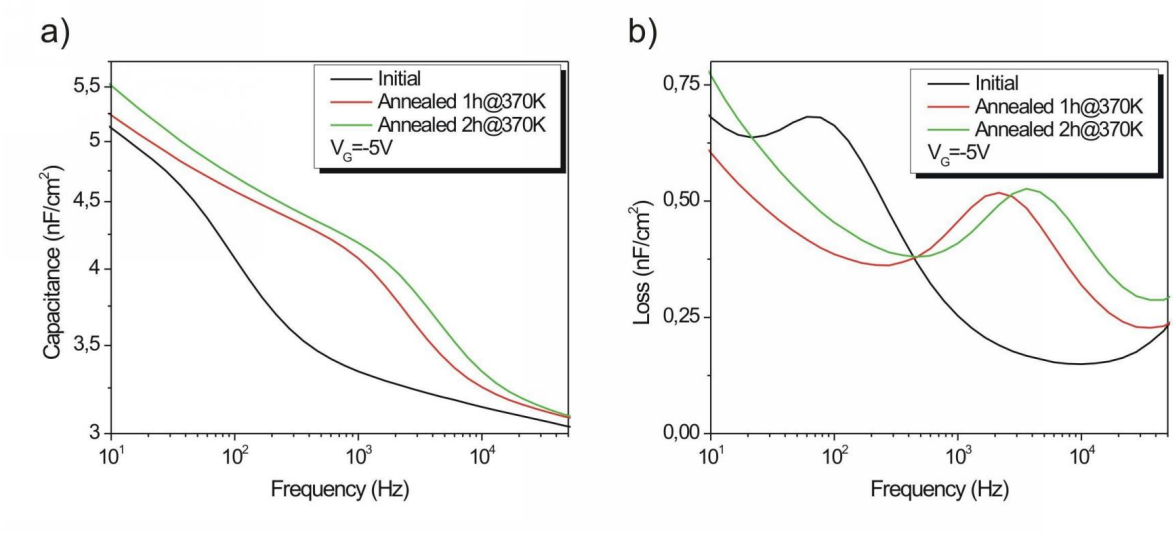

Figure 4.8: Capacitance (a), loss-frequency dependence (b) and the influence of annealing for an MIS diode with PMMA insulator

The $C - V$ characteristics presented in figure 4.9 have the typical shape with the step from depletion to accumulation. Also it has to be noticed that there is no hysteresis which shows that there are no mobile ions neither in the PMMA layer nor in the P3HT.

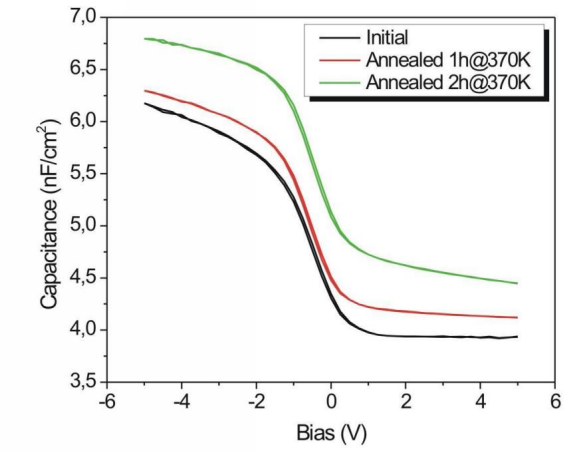

Figure 4.9: Capacitance-voltage dependence and the influence of annealing for an MIS diode with PMMA insulator

The annealing has a little peculiar effect leading to higher and higher minimum and maximum capacitances. This can be explained by a reduction of the insulator thickness, due to the fact that the annealing is done at 370K, which is very close to the glass transition temperature of the PMMA, thus reducing crystallization.
The resulting values for the doping, relaxation frequency and perpendicular mobility are summarized in the next table:

Table 4.1: Parameters of MIS diode with PMMA as insulator

Treatment	f_R(Hz)	N_A (cm^{-3})	$\mu_\perp$ cm^2/Vs
Initial	77.42	$1.72 \cdot 10^{15}$	$6.29 \cdot 10^{-7}$
Annealed 1h at 370K	2154.43	$1.84 \cdot 10^{15}$	$1.71 \cdot 10^{-5}$
Annealed 2h at 370K	3593.81	$2.48 \cdot 10^{15}$	$2.47 \cdot 10^{-5}$

As suggested by the increase of the relaxation frequency and due to the fact that the doping is basically constant the mobility increases about 50 times due to annealing.

4.4 Al_2O_3 as insulator

Aluminum oxide is a good candidate as gate insulator for organic field-effect devices. It has a dielectric constant ($\epsilon_{Al_2O_3} = 9$) about 2.5 times larger than silicon oxide ($\epsilon_{SiO_2} = 3.9$), comparable breakdown field strength, both being transparent. The advantage in using Al_2O_3 resides in the fact that it can be easily obtained, at room temperature via anodic oxidation of aluminum films, thus being compatible with flexible substrates, and due to its higher dielectric constant it would enable the operation of field-effect devices at proportionally lower voltages.
The typical setup for the anodic oxidation consists in an electrolytic bath which contains citric acid (concentration 0.01M) and a current/voltage controlled source-meter unit. The sample to be oxidized is connected to the anode and an inert counter electrode (platinum) to the cathode. Aluminum stripes (≈10mm wide) have been thermally evaporated onto 20x20 mm^2 glass substrates, with a thickness of 100nm. A constant current is passed through the electrolyte and maintained till a given anodization voltage, V_A, is reached as shown in figure 4.10(b). The thickness of the grown oxide is proportional to the anodization voltage, $d_{Al_2O_3} = k \cdot V_A$. In the case of Al_2O_3 the growth factor k is about 1.3 nm/V, as it has been verified via ellipsometric measurements. After the voltage has reached the predefined value the current starts to drop, as the oxide is self-closing and its resistance is increasing. When the current is one tenth of the initial value, the oxidation process is stopped. Finally, the samples are washed thoroughly with deionized water and dried.

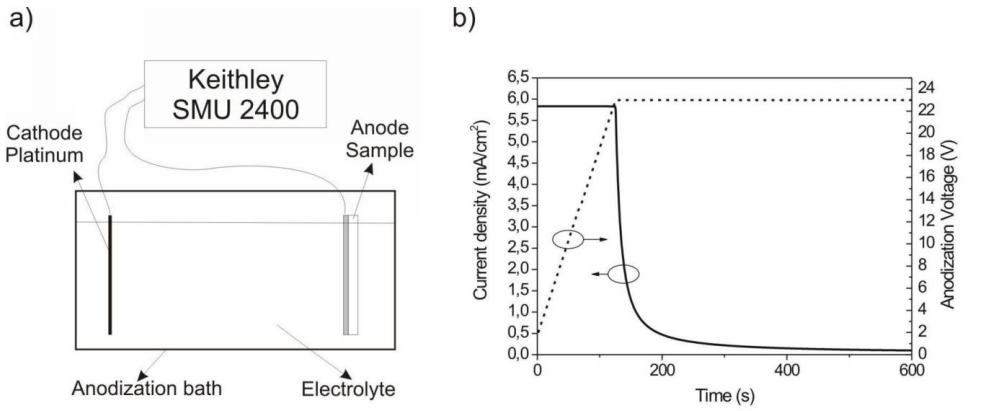

Figure 4.10: a) Anodic oxidation setup schematic and b) oxidation voltage (dashed line) and current (full line) time dependence

Atomic force microscopy was performed on the samples in order to determine the roughness of the surface of the oxide. A typical scan is presented in figure 4.11. It can be noticed that the surface is not very smooth, mean roughness being in the range of 10-15nm. This might be due to the fact that the thermally evaporated aluminum is not amorphous but polycrystalline and etching takes place at the grain boundaries. This supposition is supported by the fact that only thin films could be successfully grown. When thick films were prepared, as the oxidation time was longer, they were developing pinholes, thus rendering them useless for the fabrication of field-effect devices. It can also be noticed on the AFM image that there are some dark spots and it is to be assumed that these are the incipient pinholes.

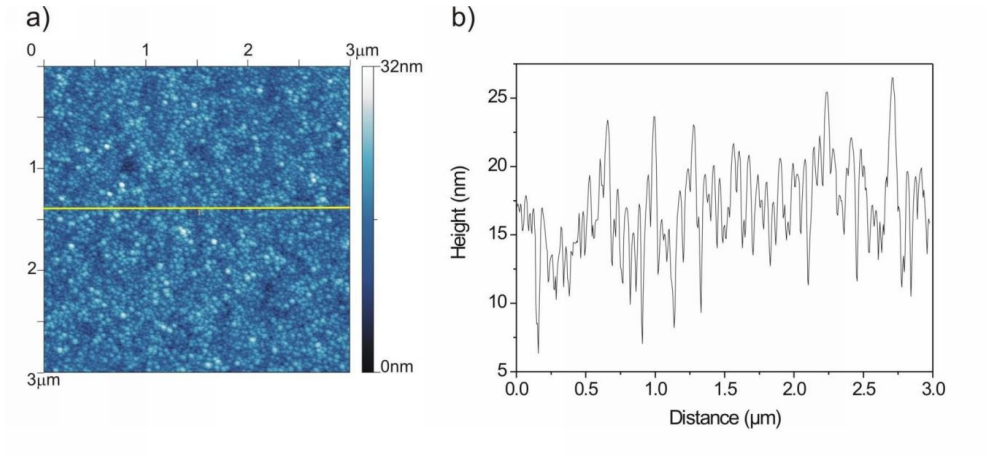

Figure 4.11: a) Atomic force microscopy image of the Al_2O_3 anodized oxide and b) a line scan to determine the surface roughness

In order to determine the dielectric constant of the aluminum oxide films rectangular gold electrodes were thermally evaporated onto the Al_2O_3 films defining an active area of about 4 mm^2. The capacitance-frequency dependence was recorded, at different biases, and the relative dielectric constant was calculated using the expression of a plane capacitor $C = \epsilon_0 \epsilon_{ox} A/d_{ox}$, where A is the area of the device, d_{ox} is the thickness of the oxide and ϵ_{ox} is the relative dielectric constant of the oxide. The resulting dependence is shown in figure 4.12.

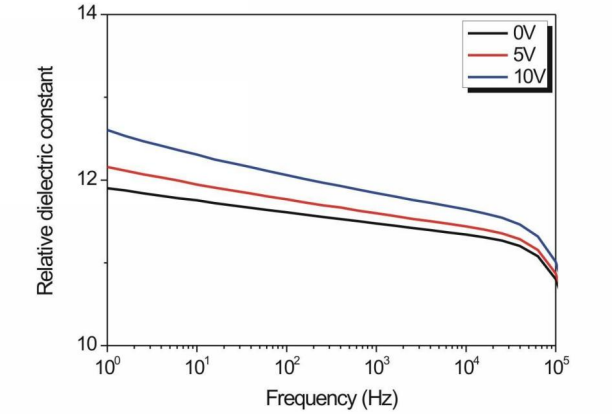

Figure 4.12: Relative dielectric constant of anodized Al_2O_3 films at different biases

The dielectric constant is slightly dependent on the applied bias. This might be due to residual electrolyte which is trapped in the film and non-stoichiometric oxide. As the aluminum oxide is a good ionic conductor (when non-stoichiometric) this increase can be caused by the ionic current, in the field generated by the applied bias. Also the value of the relative dielectric constant - 12 is about 25% higher than the typical value of 9. At the same time the assumption that electrolyte is trapped inside the film is supported by the fact that annealing (at about 100°C) of the FET structures generates high leakage currents between source/drain and bottom aluminium gate. This can happen if the solvent trapped in the Al_2O_3 evaporates and creates pin-holes in the insulator layer, generating conductive paths in the high electric fields between the top and gate elctrodes. In the case of MIS diodes this effect does not influence too much the behavior of the device as the fields are much smaller, the overall thickness of the structure being much larger. The drop of the dielectric constant at high frequencies is due to the inability of the dipols in the material to follow the frequency, thus the overall polarization and implicitely the dielectric constant of the insulator decreasing.
In order to analyze the properties of field-effect devices with aluminum oxide insulator transistors and MIS diodes have been fabricated. In the case of the MIS diodes a film of P3HT of about 400nm was spun from a 5% wt. solution in toluene and dried at 330K on a hot-plate. Subsequently gold contacts have been thermally evaporated on top.

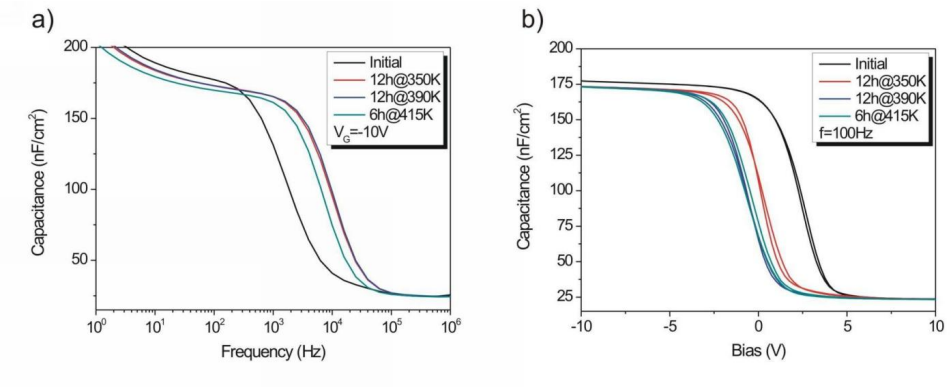

Figure 4.13: Influence of annealing on the capacitance-frequency a) and capacitance-voltage b) dependence of MIS diode with d_{ox}=135nm, d_{P3HT}=400nm and A=4mm^2

The active area of the devices so prepared is about 4 mm^2. The influence of the annealing on the capacitance-frequency and capacitance-voltage dependencies are presented in figure 4.13.
Both types of characteristics presented above are typical for the MIS diode. As seen in the previous cases annealing leads to a higher relaxation frequency, meaning that in the $C-f$ characteristic the relaxation step is shifted toward higher frequencies. We still see the increase of the capacitance at lower frequencies which as explained in the case of the melamine insulator is related to the frequency dependence of the relative dielectric constant of the insulator, on the one hand, and on the other hand is due to the spreading of the charge around the active contact. It should be remarked that the annealing at 415K leads to a slight degradation of the device, as it is shown by the fact that the relaxation frequency after this annealing step is somewhat shifted downwards.

The $C-V$ characteristics, measured at 100Hz, present minimal hysteresis. The effect of the annealing shifts the flat-band voltage from positive values toward zero, meaning that the interface trapped charge is decreasing, the hysteresis remaining very small. This shows that the Al_2O_3 despite its quite high surface roughness is of good quality. The calculated parameters of the MIS diodes are summarized in the next table:

Table 4.2: Parameters of MIS diode with Al_2O_3 as insulator

Treatment	f_R(Hz)	N_A (cm^{-3})	$\mu_\perp$ cm^2/Vs
Initial	1584.9	$6.75 \cdot 10^{16}$	$2.45 \cdot 10^{-7}$
Annealed 12h at 350K	10000	$9.86 \cdot 10^{16}$	$1.05 \cdot 10^{-6}$
Annealed 12h at 390K	10000	$8.20 \cdot 10^{16}$	$1.26 \cdot 10^{-6}$
Annealed 6h at 415K	6309.6	$8.38 \cdot 10^{16}$	$7.85 \cdot 10^{-7}$

By annealing the perpendicular mobility can be increased almost tenfold, which is still one order of magnitude smaller than the one when PMMA was used as insulator (com-

parable with SiO_2). At the same time the doping values are also one order of magnitude larger compared with SiO_2. This shows that the roughness of the surface is influencing the reorganization of the bulk of the P3HT upon annealing quite strongly.
Further, the output and transfer characteristics of field-effect transistors fabricated with Al_2O_3 as insulator are compared to the ones fabricated with SiO_2 as gate dielectric. The geometry of the transistors on aluminum oxide is as follows - insulator thickness 135nm, channel length 10μm and channel width 2500μm. The one fabricated on silicon oxide has an insulator thickness of 200nm, channel length 10μm and channel length 1000μm. Even if the geometries are a little different the important parameter is that they have the same channel length. In the figure 4.14 the comparison can be seen:

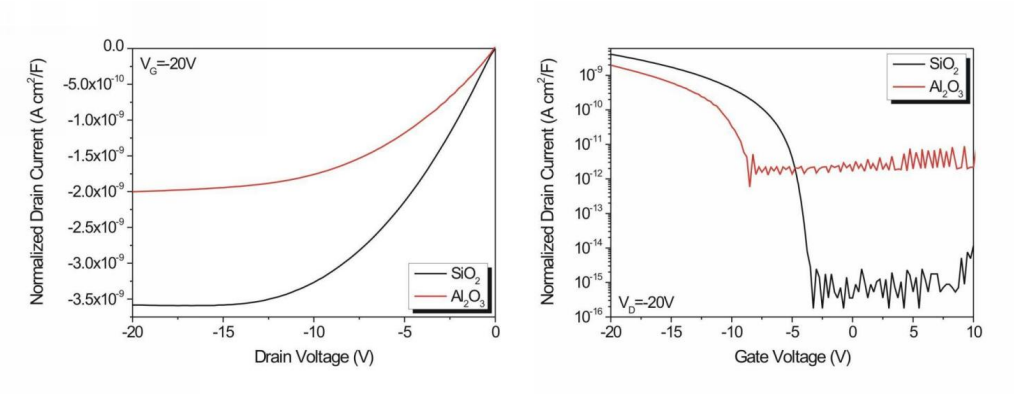

Figure 4.14: Comparison of output and transfer characteristics for OFETs fabricated with Al_2O_3 and SiO_2 as gate insulators

The *normalized drain current* has been plotted. This means the value of the drain current, in each of the cases, was divided by the respective *geometrical factor* of the FETs, $g_f = W \cdot C_{ox}/L$, where W is the channel width, L the channel length and C_{ox} the specific capacitance of the insulator. For the aluminum oxide a relative dielectric constant of 12 has been considered, as the measurements are performed in the static regime. Thus the geometrical factors, for the geometries mentioned above, are 56.5 for the SiO_2 and 45 for the Al_2O_3.
It is immediately clear that the silicon oxide FET performs much better than the aluminum oxide one. The output characteristics show the typical linear increase, at low drain voltages, in both cases, followed by the saturation of the current, but in the Al_2O_3 case this takes place at higher drain voltages which hints toward a larger threshold voltage, as seen in the following table.

The mobility calculated in the case of the aluminum oxide is about one order of magnitude lower than the one for the silicon oxide. There are a few reasons which can lead to this. Firstly one can see from the comparison of the transfer characteristics that the off current of the Al_2O_3 FET is some orders of magnitude higher than the SiO_2 which means that the bulk doping is much higher, thus the mobility being reduced. Secondly if one

Table 4.3: Comparison of OFETs parameters with Al_2O_3 and SiO_2 as gate insulators, respectively

Gate insulator	μ cm^2/Vs	V_T(V)	V$_{SO}$ (V)	ON/OFF	S (V/dec)
SiO_2	$4.75 \cdot 10^{-4}$	-5.2	-3.25	$2.3 \cdot 10^{7}$	0.25
Al_2O_3	$6.20 \cdot 10^{-5}$	-7.9	-8.5	$3.4 \cdot 10^{3}$	1.90

considers the huge differences between the surface roughness - for SiO_2 in the $\mathring{A}$ and Al_2O_3 in the tens of nm range, it is clear that the charge carriers are scattered stronger, as it has been explained in more detail in section 1.1.

4.5 Conclusions

In this chapter different gate insulators, organic and inorganic, have been used to fabricate field-effect devices. The influence of residues, in the insulator or at their surface, on the operation of the MIS diodes and field-effect transistors has been analysed.
It has been noticed that a melamin based insulator, which is thermally cross-linkable, leads to large hysteresis in the $C - V$ characteristics of the MIS diodes. Via temperature dependent measurements it has been shown that mobile ions located in the insulator are responsible for this. It was proposed that they might be related to small amounts of non-reacted cross-linking initiator.
When poly(methyl methacrylate) - PMMA was used as insulator one did not see similar effects, but typical $C - f$ and $C - V$ characteristics, with small hysteresis, comparable to devices prepared on silicon oxide. In this case, the effect of the annealing, apart from leading to an increase of the perpendicular mobility, which is implicitly correlated to the molecular ordering of the bulk of the semiconductor layer, also led to geometry modification of the MIS diode. This was seen in the different values of the insulator capacitance which were achieved after each annealing step. It has been proposed that this is due to crystallization of PMMA leading to a smaller thickness of the insulator. Nonetheless this did not lead to a failure of the device.
In the last section aluminum oxide, grown via anodic oxidation of thermally evaporated aluminum layers, was used as gate insulator. Via AFM measurements it has been shown that the surface of the Al_2O_3 layer is one or two orders of magnitude rougher than the one of SiO_2. Also residual traces of citric acid, used as electrolyte in the anodization process, led to higher doping of the P3HT films and higher dielectric constant than expected. This effect is seen in the high off current, or small ON/OFF ratio and also in the high value of the subthreshold slope. By normalizing the measured drain currents against the geometrical factor of the device, a direct comparison between FETs fabricated on Al_2O_3 and SiO_2 was possible.

Chapter 5

Influence of environmental parameters

5.1 Influence of air exposure on transport in P3HT

5.1.1 Introduction

Due to the possibility to manufacture electronic devices based on π - conjugated polymers, by printing processes, it is interesting to determine what is the influence of ambient conditions on the electrical properties of devices. We have investigated the influence of exposure to air and light upon FETs and MIS diodes.
It has already been proved that the operation of devices based on P3HT can be strongly affected by the exposure to ambient air [37],[23],[38]. For polymers with low ionization potential the interaction between the polymer and oxygen molecules is strong, leading to significant perturbations in their electrical properties. The mechanism through which this interaction takes place is based on the formation of a charge transfer complex (CTC) [39]. In the case of P3HT a weak charge transfer complex is formed. Thus after exposure to vacuum the original characteristics of the device can be recovered. The effect of the CTC is the generation of extra charge carriers. The extra charge leads to an increased doping of the bulk of the semiconducting polymer, an effect which can be seen in both MIS diodes and FETs characteristics.
As mentioned, the CTC is reversible but only as long as the semiconductor polymer is not exposed to light. For this reason all the measurements presented below are performed in dark.

5.1.2 Influence of air on the performance of MIS diodes

In the case of the MIS diodes the effect of the CTC is visible through a shift of the relaxation frequency to higher values, which corresponds to an increase of the bulk conductivity. At the same time the bulk doping, as extracted from the $C-V$ characteristics, is slightly increasing. In figure 5.1 the influence of extended air exposure of a P3HT MIS diode upon the $C-f$ and $C-V$ characteristics is presented.

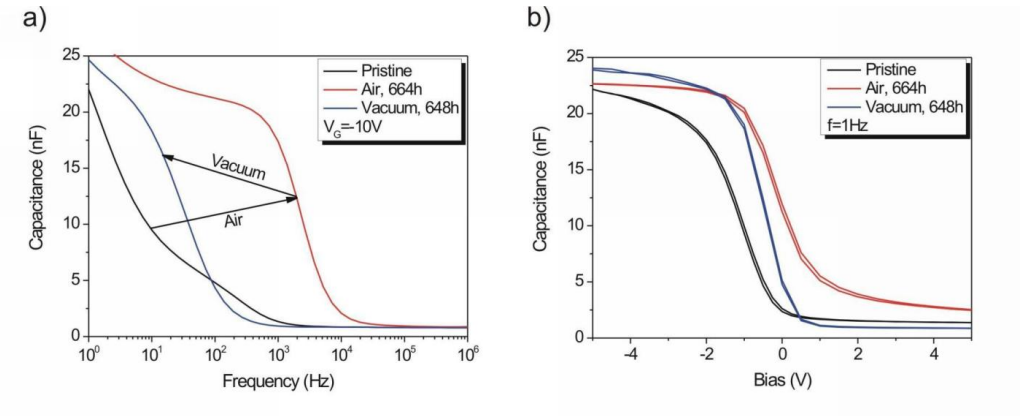

Figure 5.1: Influence of air upon the $C-f$ and $C-V$ characteristics of a P3HT MIS diode, with a layer thickness of d_S=410nm, active area A=30mm^2 and insulator thickness d_{ox}=50nm

The previous figure also presents the dedoping result which is achieved by exposing the MIS diode to vacuum together with moderate heating steps (350K). For simplicity only the extremes of the doping and dedoping processes are presented. The major influence of the air exposure is to be seen in the $C-f$ characteristics, through the shift of the relaxation frequency by about one order of magnitude from $\approx$ 200Hz to $\approx$ 2kHz. This indicates that the resistivity of the bulk is getting lower due to the oxygen doping. At the same time the values of the doping are increasing with about one order of magnitude from $\sim 2 \cdot 10^{15}$ cm^{-3} to $\sim 2 \cdot 10^{16}$ cm^{-3}. It is to be noticed that these changes are happening over a very long time ($\sim$ one month). The value of the flat-band voltage does not change too much, which might be a hint that the CTC formed with oxygen is mainly located in the bulk and not too much of it reaches the interface between the polymer and the insulator. At the same time the width of the hysteresis of the $C-V$ characteristics does not change very much, only a marginal increase being detected.
One can remark the quite atypical shape of the initial $C-f$ curve. An explanation for this can be the presence of residual doping in the sample, together with a bad organization of the bulk of the semiconductor polymer, as the MIS diode was not exposed to any thermal treatment before the first measurement. As it will be seen in the next chapter the influence of the thermal treatment upon the bulk organization is very strong.
The values of the bulk mobility and doping during the air and vacuum exposure, respec-

tively, are presented in figure 5.2:

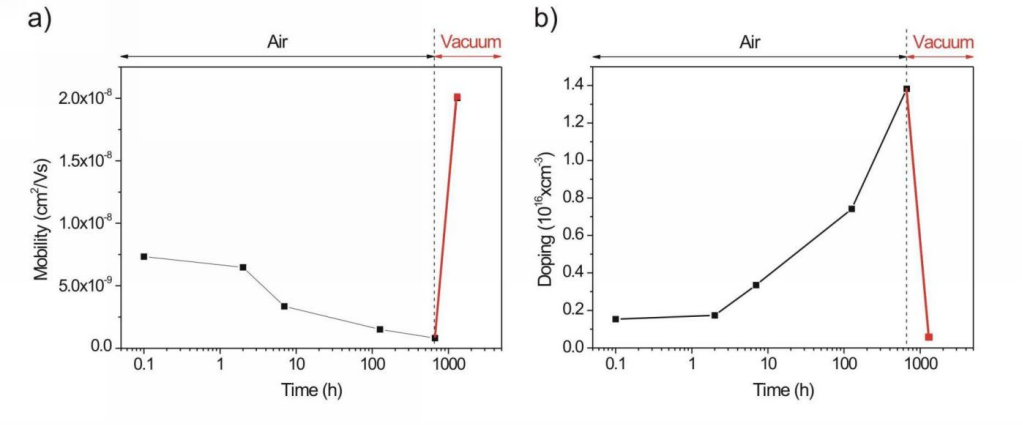

Figure 5.2: Influence of air on the bulk mobility and doping of a P3HT MIS diode, with a layer thickness of d_S=410nm, active area A=30mm^2 and insulator thickness d_{ox}=50nm

The dedoping process is also a quite slow process, as seen above. It can be seen that the relaxation frequency of the dedoped sample is somewhat larger then the initial one. The shape of the dedoped $C-f$ characteristic is much better than the initial one, showing the clear transition step. This improvement can be generated apart from the removal of the oxygen from the bulk of the diode, also by the slight annealing of the device. The purpose of the annealing is to accelerate the removal of the oxygen from the sample, but at the same time, as already mentioned, it leads to an improvement of the structural order in the bulk of the semiconductor. This supposition is supported by the fact that during air exposure the mobility is decreasing by about one order of magnitude, while after the dedoping process the increase is two orders of magnitude higher.

5.1.3 Influence of air on the performance of FETs

While in the case of MIS diodes the only influence of air is due to the oxygen doping, for the FETs also an influence of water molecules adsorbed on the surface can be detected. In special conditions, as the water molecules, due to their large dipole moment can induce additional charges in the top layers of the semiconductor polymer under the right circumstances, thus leading to a substantially increased bulk current. The difference between the oxygen doping and the influence of water molecules adsorption on the behaviour of the FETs can be told through the time constant of the processes, the one corresponding to diffusion being much larger than the adsorption one [40]. As only bottom contact FETs have been used in the following and no sudden increase of the bulk current has been observed upon exposure to air it can be concluded that for this geometry of the FETs the effect of water is negligible.
The influence of air on the electrical properties of the P3HT based FETs, as well as meth-

ods to make it more stable against O_2 doping effects has been given a lot of attention in the past few years [41], [43]. It has been proposed that the doping is due to a charge transfer complex with the oxygen molecules, see figure 5.3. As P3HT is a electron donor, while the oxygen is a electron acceptor, a weakly bound CTC is formed. The relatively high ionization potential of P3HT prevents the formation of a strongly bound CTC which would completely alter the electric performance of the devices. It has also been shown that the O_2 influence is proportional to the pressure - the higher the pressure the more *ohmic-like* the behaviour of the FET [39].

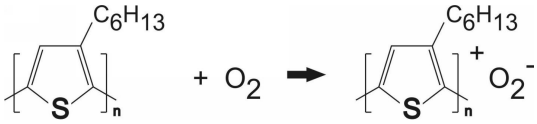

Figure 5.3: Schematic diagram of poly(3-hexylthiophene)-oxygen charge transfer complex formation.

It is important to mention that the doping effect of oxygen is not very strong, as it will be seen later in this chapter, in the absence of the light. Upon simultaneous exposure of the FETs to air and light, however, the electrical properties are highly degraded and more importantly the FETs can not be dedoped in vacuum, as the films suffer an irreversible photo oxidation.

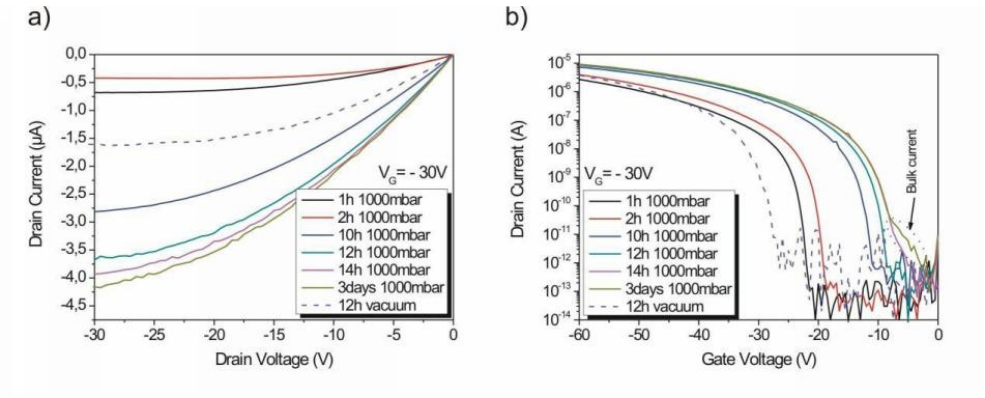

Figure 5.4: Influence of doping (air) and dedoping (vacuum) on the output (a) and transfer (b) characteristics of a P3HT FET, with a layer thickness of d_S=50nm, channel length L=7.5μm, channel width W=1000μm and gate silicon oxide thickness d_{ox}=200nm; the dashed line represents, in both cases, the curve after vacuum dedoping

The time scale on which the oxygen doping is visible is much sorter than in the case of the MIS diodes, as it can be seen in figure 5.4, due to the thinner semiconductor polymer layer and also due to the fact that there is no metal top electrode to protect the P3HT film.

The influence of oxygen doping on the output characteristics consists in an increase of the current over time, the saturation region being not so well defined anymore. This can be explained by a shift of the threshold voltage toward more positive values as seen in the transfer characteristics in figures 5.4(b) and 5.5. This shift is caused by an increased bulk doping and negative charge accumulation at the interface between silicon oxide and P3HT. At the same time the doping is seen in an increase of the subthreshold slope together with a decrease of the ON/OFF ratio. After a long exposure to air a shoulder-like feature can be observed in the transfer characteristics, around the switch-on voltage. This feature was noticed by others too [44] and it is related to the fact that at high values of the bulk doping the device behaves in a manner similar to a junction field-effect transistor. This behavior adds to the normal operation of the OFET. In order to see this effect one needs a system where the mobility is charge carrier dependent. In cases when the field-effect mobility is the same as the bulk mobility this effect is not observed [41]. At the same time the saturation mobility, as determined from the transfer characteristics, is slightly increasing, as it can be seen in the figure 5.5:

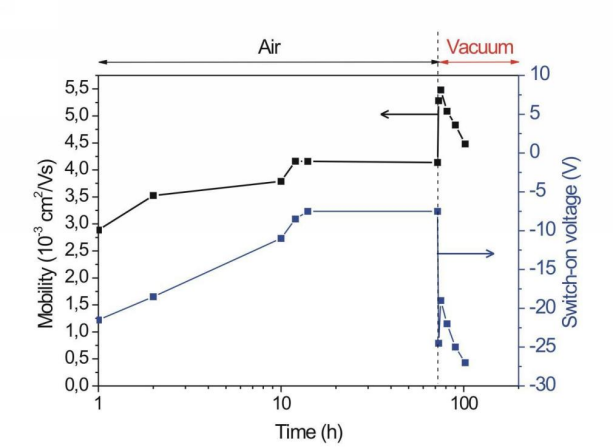

Figure 5.5: Variation of the saturation field-effect mobility and switch-on voltage (V_d=-50V) upon doping and dedoping with oxygen, in air

The dedoping procedure was carried out in high vacuum (10^{-6}mbar or better) and after twelve hours the output and transfer characteristics are close to the original ones (dashed lines in figure 5.4). The dedoping process is much faster then in the case of the MIS diodes, due to the reduced layer thickness and lack of top metal electrode. This way the oxygen molecules have to travel only through 100-150nm compared to microns in the case of the MIS diodes. At the same time the switch-on and threshold voltage are shifting back to more negative values as the bulk doping and interface charge are decreasing.

5.2 Influence of light

The influence of light is of major importance for the operation of organic devices as it can induce undesired effects, like hysteresis and threshold voltage shift. At the same time knowing the response to illumination of the FETs can enable their use as light detectors. Hysteresis effects can be observed in both transfer and output characteristics, but usually they are more pronounced in the transfer characteristics (see figure 5.6). The measurements were performed on a field-effect transistor with OTMS SAM treated SiO_2 as insulator. OTMS stands for oxy-(tri-methyl)silazane and it has been grown on the surface as a monolayer. Its purpose is to enable the formation of a P3HT film with better quality and at the same time to minimize the interface effects. The next chapter deals in detail with surface modifications and their influence of the electrical properties of FETs. In order to illuminate the sample with different wavelengths a monochromator was attached to the microscope used to help contacting the sample. This way the light could be focused onto the sample. All the measurements were performed in high vacuum (10^{-6} mbar or better) and precautions against influences coming from the ambient light were taken.
The next figure presents the output and transfer characteristics under illumination with different wavelengths compared to the ones in dark.

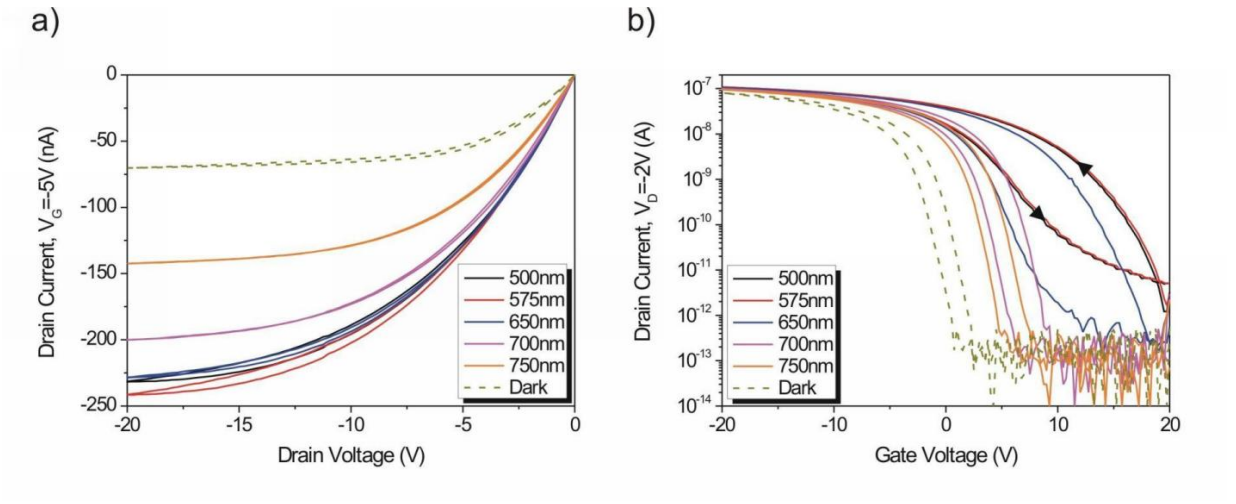

Figure 5.6: Influence of illumination with different wavelengths on the output (a) and transfer (b) characteristics and the comparison with measurements in dark (dashed lines) for a FET with 1000μm channel length, 5μm channel width and 200 nm thick silicon oxide

In order to see better the influence of illumination the output characteristics were measured at low gate voltages (V_G=-5V) and the transfer ones in the linear regime (V_D=-2V). It can be noticed that the hysteresis is quite small in the output characteristics compared to the hysteresis in the transfer ones. This would be a hint that the effect of illumination is located at the interface between the organic semiconductor and the silicon oxide. At the same time the maximum output current is scaling with the wavelength of the incident light,

increasing about three times from dark to 575nm, while no evidence of contact resistance can be noticed.

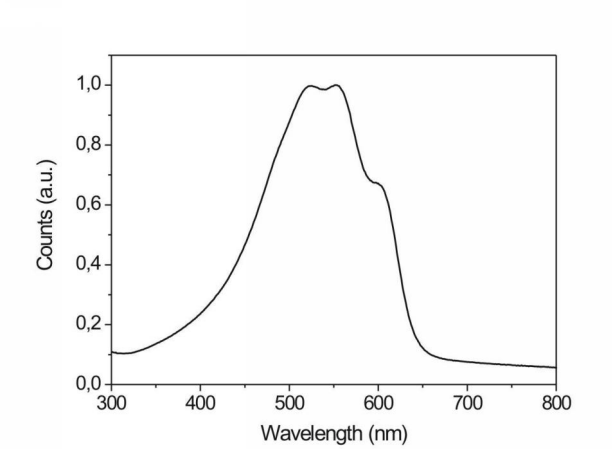

Figure 5.7: Absorption spectra of P3HT thin film (100nm) on quartz glass

From figure 5.7 it can be seen that the P3HT has an absorption maximum in the range 525-550nm. Unfortunately, the closest wavelength at which the characteristics were recorded is 575nm. Nonetheless the increase of the current, in the output characteristics, follows the absorption spectra of the P3HT. At the same time the hysteresis of the output characteristics is also scaling with the wavelength.
Major changes from dark to illumination can be seen in the transfer characteristics, too, as an increase of the hysteresis and of the off-current together with a strong shift of the switch-on voltage, similar to the effect of oxygen exposure. The shift of the threshold voltage is due to negative charge accumulation at the interface between the organic semiconductor and the silicon oxide, as detailed in the previous chapters. The value of the off-current is also increasing, by about one decade at 575nm, which is due to a higher value of the bulk doping. The device parameters (mobility, variation of threshold voltage and switch-on voltage,ON/OFF ratio,...) extracted from the transfer characteristics, for the illumination with different wavelength, are presented in table 5.1.
The shift of the switch-on voltage, under illumination, toward more positive values, compared with the dark measurement, shows that a negative charge build-up takes place at the interface. This could be explained by the formation of polarons [45], [46], which are quite immobile and have long life time. The polarons are kinetically metastable at dilute concentrations in low molecular-weight polymers, as the number of defects and imperfections is high enough to limit their mobility and inhibit the bipolaron formation [47]. During the gate sweep from depletion to accumulation part of these polarons are detrapped thus decreasing the charge density at the interface and leading to a shift of the switch-on voltage toward zero.

Table 5.1: Comparison of P3HT properties for different wavelength illumination

Wavelength (nm)	μ cm^2/Vs	ΔV_T(V)	ΔV_{SO} (V)	ON/OFF	S (V/dec)
Dark	$7.26 \cdot 10^{-4}$	1.71	1.75	$3.5 \cdot 10^5$	1.03
500	$6.77 \cdot 10^{-4}$	6.18	11.75	$2.1 \cdot 10^4$	3.44
575	$6.82 \cdot 10^{-4}$	6.33	11.75	$2.1 \cdot 10^4$	3.44
650	$7.09 \cdot 10^{-4}$	5.46	9.75	$3.7 \cdot 10^5$	1.75
700	$7.62 \cdot 10^{-4}$	2.57	3	$4.7 \cdot 10^5$	0.92
750	$7.65 \cdot 10^{-4}$	1.94	3	$6.7 \cdot 10^5$	0.88

5.2.1 Conclusions

In conclusion, the exposure of the MIS diodes and FETs to ambient air leads to oxygen doping as no evidence of the influence of water can be detected. The oxygen diffusing into the P3HT layer forms a weak, fully reversible charge-transfer complex with the P3HT molecules, thus increasing the charge carrier concentration in the bulk of the semiconductor. This is seen as an increase of the doping and the mobility in both MIS diodes and FETs, followed by a sharp decrease upon exposure to high vacuum.
Illumination leads to a qualitatively similar behavior in both situations. The electrical properties of the MIS diodes and FETs are affected due to the formation of polarons, which as previously mentioned have a long dissociation time constant, thus leading to the observed hysteresis effects. At the same time it has been shown that the intensity of the illumination effect depends on the wavelength and can be correlated with the absorption spectra of the poly(3-hexyl)thiophene.
A comparison between the influence of air exposure and illumination shows us that in both cases a shift of the threshold voltage is present, meaning that they both lead to negative charge accumulation at the interface between the organic semiconductor and the insulator. At the same time one observes an increase of bulk doping, this being responsible for the increased current in the off-state. The combined exposure to air and light, especially in the UV range, usually leads to irreversible photo-oxidation of P3HT, thus rendering it useless.

Chapter 6

Influence of preparation parameters in SiO_2 field-effect devices

6.1 Introduction

The operation of the organic field-effect devices can be drastically influenced by the interface between the insulator and the semiconductor, as mentioned in the previous chapters. This influence is due to different factors like existence of traps at the interface but also due to the insulator surface energy, which influences the way the organic semiconductor layer grows, in the case of small molecules, or reorganizes, in the case of polymers.
One common method to change the insulator surface properties is by chemisorption of molecules on a solid substrate by the retraction method from solution [48], [49]. Thus self-assembled monolayers (SAMs) are formed on the surface. On the one hand, SAMs, due to their large band gap $\sim$ 4 - 4.5 eV, will improve the properties of the insulator by decreasing leakage currents and neutralizing surface defects which can act as traps. On the other hand, they can introduce defects of their own, altering the performance of the devices, as it will be detailed during this chapter.
Improvement of the behavior of MIS diodes and FETs can be obtained if they are annealed in vacuum after preparation. It has been shown to have a positive influence on both semiconducting polymers and small molecules [50]. The effect of annealing is influencing both the structural and chemical properties of the organic films. Usually the crystallinity is increasing which leads, in case of OFETs to higher mobilities. At the same time the residual doping, like oxygen or other dopant species, coming from the preparation process, is reduced, sometimes even by orders of magnitude, which would lead, for example, to higher On/Off ratio of organic FETs. At the same time the amount of traps present at the semiconductor-insulator interface can be reduced, thus reducing hysteresis effects.
Another parameter which can influence the charge transport is the choice of solvent. This is easily understood if one takes into consideration the evaporation speed. In most of the cases the semiconducting polymer films are created via spin-coating, so the boiling point (evaporation speed) of the solvent is very important. If a solvent with high evaporation

speed, like chloroform, is used it is quite clear that the film formation kinetics are very fast and the polymeric chains do not have time to organize themselves (crystallize). On the contrary, if a solvent with lower evaporation speed is used, like toluene or dichlorobenzene (DCB), the film formation kinetic is slower and the polymer chains have the opportunity to organize themselves, as it will be shown later in this chapter. In other words the P3HT film has a longer time to crystallize if the boiling point of the solvent is high ($BP_{Toluene}$= 111 °C, BP_{DCB}= 181 °C) [51].

6.2 Self assembled monolayers on SiO_2

In the present case the molecules used for growing SAMs are octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HMDS). Their chemical structures and the resulting SAMs are schematically presented in figure 6.1.
Silicon oxide was used as insulator and different SAMs were grown on it. The SAM growth requires a few steps. First the substrate is exposed to O_2 plasma resulting in an oxygen enriched surface. Then the samples are rinsed with deionized water in order to obtain a hydroxyl rich surface, required for this silanization procedure. The last step, which represents the actual SAM growth step, consists in immersing the samples in a low concentration solution ($10^{-3} - 10^{-4}$ M) containing the molecules to be grafted, for 24 hours. In the case of the HMDS this is done at a temperature of 60°C.

In the case of OTS molecules the end chloride atoms are removed and the molecule bonds to the hydroxyl groups on the SiO_2 surface, forming a brush-like structure, the long chain axis oriented roughly perpendicular to the solid substrate, as seen in figure 6.1. The OTS is in particular more attractive as during the SAM formation it suffers a lateral cross-linking, too, by condensation of neighboring SiOH groups into siloxane Si-O-Si linkages. Due to the van der Waals interactions between the neighboring chains the OTS molecules cannot orient themselves perpendicular to the surface, but they are slightly inclined[52]. It has been shown that the SAMs grown this way form a monolayer on the SiO_2 surface, with low interface density of states reflected also in the high contact angle [53]. Another similar molecule, the octadecyltrimethoxysilane - OTMS, has been used to grow SAMs on SiO_2 surfaces. In the OTMS molecule the chloride atoms are replaced with methoxy groups. The growth of the monolayer is similar to the one for the OTS with the exception that methanol and not chloride is the reaction byproduct.
In the case of HMDS the reaction between the molecules and the OH covered surface goes according to the following reaction scheme [54]:

$$2[\equiv Si - OH] + (CH_3)_3 - Si - NH - Si(CH_3)_3 \rightarrow 2[\equiv Si - O - Si(CH_3)_3] + NH_3$$

meaning that the HMDS molecule splits in two at the NH group and the silicon atom bonds to the oxygen atom of the OH group on the silicon oxide surface. Ammonia gas being a by product of this reaction. The high degree of packing in the case of OTS is revealed by the value of the critical surface tension [55], which corresponds to a layer of methyl groups -

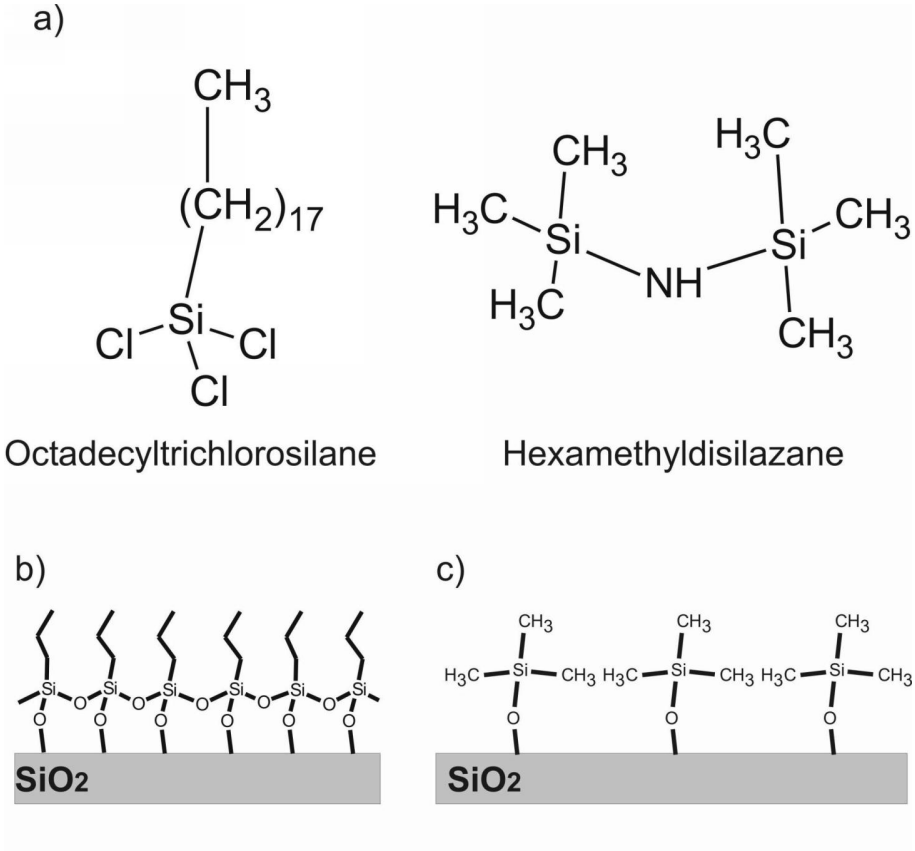

Figure 6.1: Molecules used in the growth of self-assembled monolayers on SiO_2: a) octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HMDS); b) OTS and c) HMDS cross-linked SAMs, respectively

the end-capping groups of the alkyl chains. This shows that the OTS SAM is more robust and uniform than the HMDS one.
One direct way to check the differences between the properties of surfaces after treatment consists in measuring the contact angle of the water, which is proportional to the surface energy, as described in chapter 2.3. The highest value of the contact angle is obtained for OTS, which is related to the higher density of molecules than in the case of HMDS. The treatment described as "Untreated" and "O_2" are the cases where SiO_2 was used as it was and exposed to O_2 plasma, respectively. Thus one can compare the properties of the devices over quite a wide range of contact angles. The choice of the O_2 treatment, in order to have small water contact angles, might not have been the very best one as it would definitely lead to doping of the polymer semiconductor layer. Values of the water contact angle are given in the next table:

The structure of the P3HT films was microscopically analysed using grazing incidence X-Ray diffraction, as already mentioned in chapter 2, even if only from a qualitative point

Table 6.1: Water contact angle values on different SAMs

Surface Treatment	Contact angle (°)
Untreated	62
HMDS	95
OTS	111
$O_2 plasma$	<5

of view. The results are in good agreement with the data from literature [1],[2], showing that the crystalline domains in P3HT films are in the range of 10-11 nm. The X-Ray diffraction spectra (see figure 6.2) show in all cases a peak centered at about 5.4° which is known for the organized lamellar structure of rr-P3HT with $\pi - \pi$ orbital interchain stacking within the crystallites. This corresponds to a layer spacing of about a=16 $\mathring{A}$ [56].

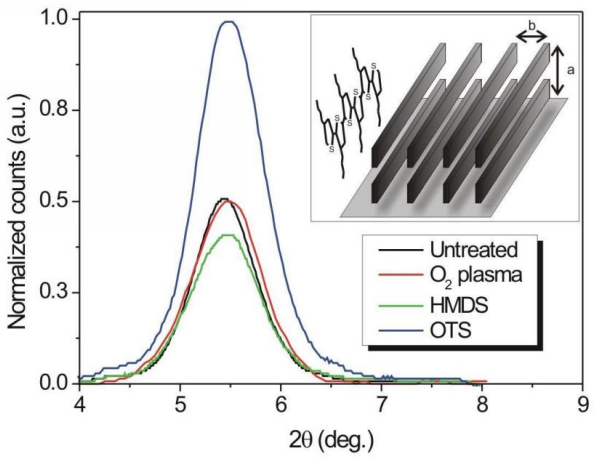

Figure 6.2: Grazing incidence X-Ray diffraction spectra of P3HT films on glass substrate for the different surface treatments; inset shows the lamellar structure of P3HT crystallites

No evidence for the other two possible orientations of P3HT with respect to the substrate (corresponding to diffraction peaks around 23°) was found.

6.3 MIS diodes with self-assembled monolayers

In the following the influence of these surface treatments will be investigated in the case of metal-insulator-semiconductor (MIS) diodes. In this case the charge transport takes place in the perpendicular plane to the insulator-semiconductor interface. The reason for studying MIS diodes is to find out if the influence of the SAM is also extending into the

bulk of the semiconductor layer, away from the interface [42].
As described in chapter 3, in order to extract the charge carrier mobility in MIS diodes, one has to measure and analyse two kinds of characteristics: the capacitance-frequency and capacitance-gate bias dependence. In figure 6.3 the capacitance-frequency and the loss-capacitance dependence of MIS diodes with modified insulators are presented.

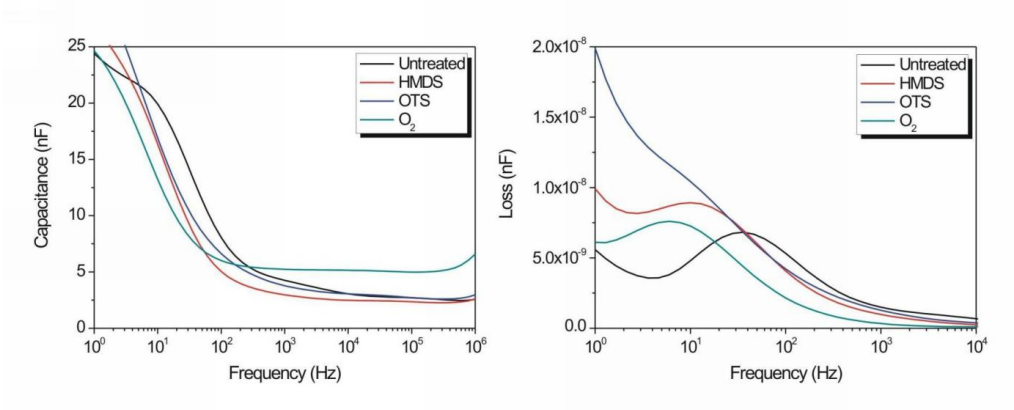

Figure 6.3: Capacitance-frequency and loss-frequency dependence for P3HT MIS diodes with different surface treatments

There are a few features which have to be explained before going further. Firstly the differences between the capacitance values in depletion (at high frequencies) is due to different contact areas and thicknesses of the semiconductor layers, as the oxide thickness is the same in all the cases. Secondly, one would expect that the capacitance, in accumulation (low frequencies), will saturate at the oxide capacitance value, but it does not. This is usually caused by charge spreading beyond the area defined by the top contact [57], thus leading to an artificial increase of the capacitance. This effect could be prevented if a shield is created around the top electrode, by evaporating another contact which is grounded. As one would expect that the out-of plane mobility is not very high then this spreading would suggest a high in-plane charge carrier mobility.
It can be noticed that the relaxation frequencies, which are given by the maximum of the loss function, are quite low, in the Hz range. This shows that the bulk conductivity is quite low meaning that the distance up to which the surface treatment is influencing the semiconductor morphology is not too large.
In order to extract the out-off plane mobility one has to determine the doping concentration as the mobility is given by:

$$R_S = \frac{d_s}{qN_A\mu_\perp A}$$

where R_S is the semiconductor resistance, extracted from the C-f characteristic, d_S the semiconductor thickness, N_A the bulk doping, q the elementary charge and A the area of the device. The figure 6.4 shows the C-V characteristics corresponding to all the surface treatments.

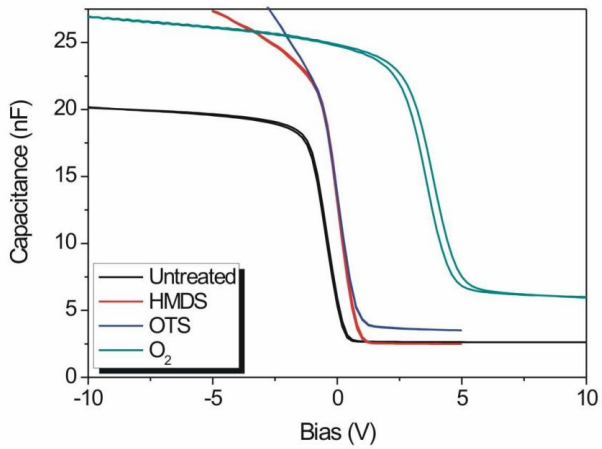

Figure 6.4: Capacitance-voltage dependence for P3HT MIS diodes with different surface treatments

The gate bias has been swept from positive (depletion regime) to negative values (accumulation regime) and back. The purpose of this kind of sweep, as in the case of transfer characteristics of FETs, is to show if trapping and release processes take place at the interface. Such processes are usually revealed by the presence of a hysteresis between the two sweep directions. One can notice that whereas the untreated, HMDS and OTS-treated MIS diodes show a sharp transition between the accumulation and depletion around zero gate bias with only marginal hysteresis between increasing and decreasing bias sweeps, the O_2 -plasma treated diode has a larger hysteretic behavior and the transition between depletion and accumulation takes place at a higher V_{FB}. This can be seen as an indication of interface states at the P3HT/SiO_2 interface created by the O_2 plasma treatment.
In the case of OTS and HMDS treated substrates the measured capacitance does not saturate at the value of the oxide capacitance, in the accumulation regime, but increases significantly above this value, which as in the case of the $C - f$ characteristics, is due to charge spreading beyond the active area of the top contact. As expected, based on the $C - f$ dependence, this effect is particularly pronounced for the OTS treated substrate. The values of the doping, relaxation frequency, flat-band voltage and perpendicular charge carrier mobility are presented in table 6.2:

In the case of the O_2 plasma treatment the bulk doping value is one order of magnitude higher than in the other cases, meaning that part of the O_2 and OH molecules which are present at the interface are diffusing into the bulk. Also interesting is the value of the mobility for the untreated substrate, the highest of all, which shows that the self-organization which is promoted at the interface by the SAM layers, beneficial for the FETs, can prevent further self-organization in the bulk of the semiconductor.
In the following the influence of SAMs on the operation of FETs will be looked upon.

Table 6.2: Relaxation frequency-f_R, bulk doping-N_A, flat-band voltage-V_{FB} and off-plane mobility-$\mu_\perp$ for MIS diodes with different surface treatments

Treatment	$f_R(Hz)$	$N_A(cm^{-3})$	$V_{FB}(V)$	$\mu_\perp(cm^2/Vs)$
Untreated	35	$3 \cdot 10^{15}$	-0.1	$9.3 \cdot 10^{-7}$
HMDS	10	$3.1 \cdot 10^{15}$	$+0.25$	$2.7 \cdot 10^{-7}$
OTS	7	$7.1 \cdot 10^{15}$	$+0.2$	$7.8 \cdot 10^{-8}$
O_2 plasma	6	$2.4 \cdot 10^{16}$	$+3.6$	$1.1 \cdot 10^{-8}$

6.4 OFET with self-assembled monolayers

In the previous section the influence of surface modification via self-assembled monolayers on the operation of MIS diodes has been analysed. This basically addresses the differences between the properties of the insulator-semiconductor interface and its influence on the charge transport in the perpendicular direction to it.
In order to investigate the influence of the substrate treatment on the operation of the field-effect transistors, output and transfer characteristics in the saturation regime, were measured. The mobility and threshold voltage were determined from a fit of the linear part of $\sqrt{I_D}$ versus V_G, as described in chapter 3.2. The output characteristics for the four different treatments are shown in figure 6.5.

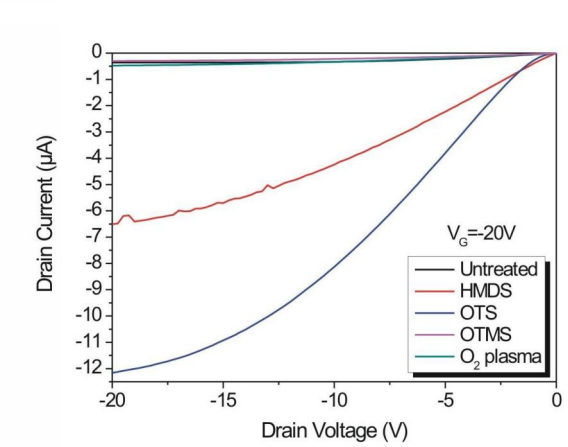

Figure 6.5: Comparison of output characteristics of P3HT FETs for different surface treatments

The surface treatment is clearly influencing the properties of the field-effect transistors, as the current is increasing from the untreated sample to the OTS treated one by about 40 times. This large difference can have different reasons. On the one hand it can be seen that the polymer layers have a better quality on the OTS and HMDS treated sample, so that the charge transfer from one crystallite to the other is more efficient. But on the

other hand it can be simply due to a large positive shift of the threshold voltage. It can be that both of these effects are present. For this reason one has to have a look at the transfer characteristics to be able to tell between the two effects. Another feature which can be observed in these output characteristics is that the onset of the output characteristics has the expected linear behavior, with the exception of the OTS treated sample. In this case some evidence of contact resistance is suggested by the non-linearity at low drain voltages. The transfer characteristics for all the surface treatments are presented in figure 6.6, together with the $\sqrt{I_D} - V_G$ dependence.

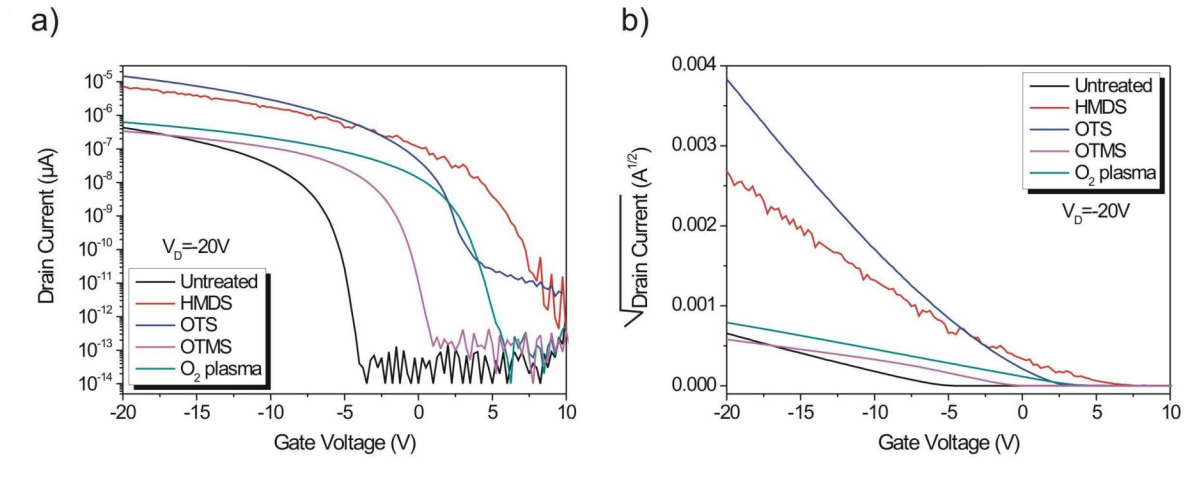

Figure 6.6: Comparison of transfer characteristics of P3HT FET for different surface treatments

Apart from the difference in current, a large shift of the switch-on voltages is also visible. In chapter 1 the switch-on voltage was defined as the flat-band voltage being proportional to the interface charge density. This, in turn, is proportional to the density of defects at the interface and is a measure of its quality. Considering this, one notices that the surface treatment with the OTS SAM is somewhat better than with HMDS, which was to be expected as long as HMDS does not undergo the lateral cross-linking described at the beginning of this chapter. In the $\sqrt{I_D} - V_G$ representation one can notice that the characteristics are linear over a large range of gate voltages, thus confirming the fact that the field-effect transistors are operating in the saturation regime. The parameters of the field-effect transistors with different surface modifications are presented in table 6.3.
The subthreshold slope which is defined as $S = \partial V_{GS}/\partial log(I_D)$ tells us how many volts are required to change the value of the drain current by one order of magnitude, at small gate voltages ($V_G < V_T$). It basically defines how fast, in terms of V_G, the transistors turn on. In a good transistor this value should be as small as possible. The minimum value of the subthreshold slope, at 300K, calculated using the Boltzmann statistics for carriers, is approximately 60mV/dec, but this value can increase in the case of organic transistors up to a few volts per decade [58]. In all cases, except for the HMDS treated sample, the

subthreshold slope has good values.

Table 6.3: OFET parameters (saturation mobility μ_{sat}, threshold voltage V_T, switch-on voltage V_{SO}, On/Off ratio, subthreshold slope S) for the different surface treatments

Treatment	$\mu_{sat}(cm^2/Vs)$	V_T(V)	V_{SO}(V)	On/Off	S(V/dec)
Untreated	$1.7{\cdot}10^{-3}$	-6.34	-4.06	$1.2 \cdot 10^7$	0.44
HMDS	$1.3{\cdot}10^{-2}$	-0.20	7.50	$7.8 \cdot 10^7$	1.56
OTS	$3.4{\cdot}10^{-2}$	-2.30	3.65	$1.4 \cdot 10^6$	0.92
OTMS	$1.1{\cdot}10^{-3}$	-0.79	1.48	$7.3{\cdot}10^5$	0.45
O_2 plasma	$8.4{\cdot}10^{-4}$	3.81	6.25	$3.0 \cdot 10^6$	0.60

The magnitude of the ON/OFF ratio which is varying from treatment to treatment shows that the surface treatments are inducing different degrees of bulk doping and interface charge density. The values of the bulk doping and interface charge density can be determined using the definitions of the switch-on voltage (1.38) and threshold voltage (1.37) from chapter 1:

$$V_{SO} \equiv V_{FB} = \Phi_{MS} - \frac{qN_{if}}{C_{ox}} \qquad \text{and} \qquad V_T \equiv V_0 = V_{FB} \pm \frac{qN_A d_s}{C_i} - 2\phi_B$$

where the Φ_{MS} is the work function difference between the gate metal and the semiconductor, q the elementary charge, C_{ox} the oxide specific capacitance, N_{if} the interface charge density and ϕ_B the semiconductor bulk potential. The calculated values for the semiconductor bulk doping and interface charge density are summarized in the next table.

Table 6.4: Bulk doping, interface charge density and sign for OFETs (N_A bulk doping and N_{if} interface charge density) with different surface treatments; the workfunction of p^{++} silicon - $\phi_{p^{++}Si}$ was considered 5.1 eV

Treatment	$N_A(cm^{-3})$	$N_{if}(cm^{-2})$	Charge sign
Untreated	$6.3{\cdot}10^{16}$	$4.3 \cdot 10^{11}$	-
HMDS	$2.9{\cdot}10^{17}$	$8.1 \cdot 10^{11}$	+
OTS	$2.2{\cdot}10^{17}$	$3.9 \cdot 10^{11}$	+
OTMS	$1.6{\cdot}10^{16}$	$1.5 \cdot 10^{11}$	+
O_2 plasma	$7.1{\cdot}10^{16}$	$6.7 \cdot 10^{11}$	+

As expected, the presence of a positive charge at the interface is shifting the switch-on voltage toward negative values, while a negative charge has the opposite effect. This shows that one could tune the position of the switch-on voltage by modifying the insulator surface. The values of the bulk doping are also following the trend visible in the transfer characteristics.

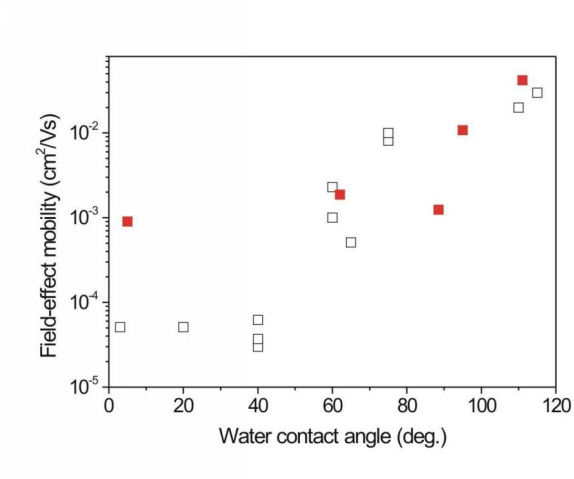

Figure 6.7: Field-effect mobility dependence on contact angle; open squares are from [59], filled squares data from this work

In conclusion the surface modification with self-assembled monolayers leads to significant changes in the parameters of field-effect transistors. The field effect mobility shows a close correlation with the water contact angle on the substrate, increasing with the hydrophobicity of the SiO_2 surface, as it has been also observed by Veres et al. [59]. Figure 6.7 compares our values of the mobility with the ones from literature, finding a very good agreement, with the exception of the value corresponding to the oxygen plasma treatment. In this case the surface is highly reactive thus leading to a much higher mobility than expected. In the following section the influence of thermal treatment will be presented and it will be shown that is has a major effect.

6.5 Influence of annealing

The effect of annealing on the properties of P3HT films was studied for the different surface treatments, already mentioned above, both from a structural and electrical point of view. The structural analysis was performed using grazing incidence X-Ray diffraction on a few hundred nanometers thick P3HT films, spin-coated on glass substrates modified with SAMs or not, as already mentioned at the beginnig of this chapter. Below a comparison of XRD spectra before and after annealing is presented.

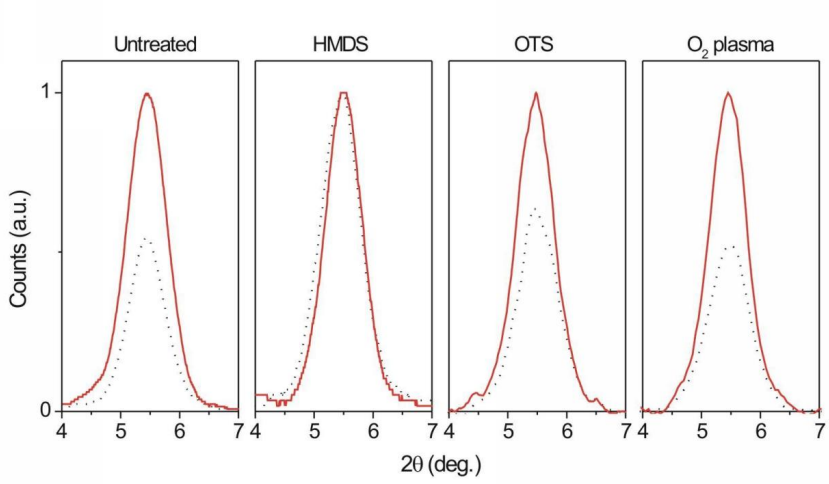

Figure 6.8: Comparison of grazing incidence XRD spectra for the different surface treatments, before (dotted line) and after annealing for 12 hours at 350K (straight line)

It can be noticed that the main effect of annealing consists in an increase of the peak height, while the full width at half maximum stays almost constant. The grain size lies in the range 10-11 nm for the as prepared samples and increases to about 13 nm after annealing. The increase of the peak height after annealing would suggest that the all over crystallinity is increasing, which would mean that the charge carrier mobility is higher, as it will be seen later. The HMDS treated substrate does not show the peak increase, but it is to be assumed that this is rather a fault of the measurement then a lack of crystallinity increase.

The effect of annealing on the MIS diodes is mainly observed in the capacitance-frequency dependence, as mentioned before. From the figure 6.9(a) two important features can be observed. On the one hand, substrate treatment has only a weak influence on the relaxation frequency, but on the other hand the effect of annealing is very strong. The relaxation frequencies of the as prepared samples are in the tens of Hertz range, after annealing they are found in the kHz range. This clearly indicates that the semiconductor bulk resistance can be reduced by up to three orders of magnitude by thermal annealing, while the substrate treatment has little influence on it.

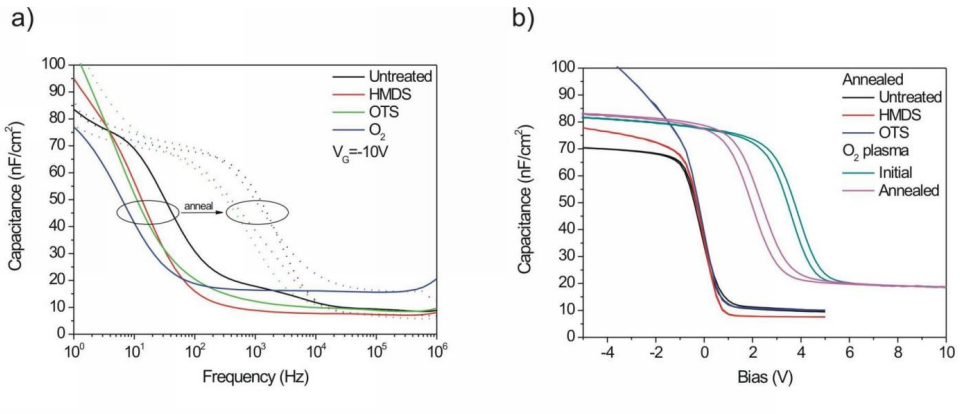

Figure 6.9: The influence of annealing on the (a) capacitance-frequency dependence of MIS and (b) capacitance-bias dependence of MIS, for the different substrate treatments

In figure 6.9(b) the $C-V$ characteristics of the MIS diodes, for different surface treatments, before and after annealing are shown. For simplicity only the after annealing curves are shown, as the change is not significant, with the exception of the oxygen plasma treated MIS diodes. The presented characteristics are measured at 1Hz, apart from the untreated MIS diode where they are measured at 10Hz.
The bulk doping concentration (see Table 6.5) is slightly reduced in the case of HMDS and OTS treated MIS diodes, while for the untreated and O_2 plasma treated MIS diodes it increases. This increase can be explained, as in section 6.4, by the diffusion of charged molecules, initially trapped at the interface between the oxide and the semiconductor (like O_2 molecules and OH groups) into the bulk of the semiconductor layer. The hysteretic behaviour of the capacitance for the oxygen plasma treated MIS diodes does not get smaller after annealing. One can notice a shift of the flat-band voltage toward zero accompanied by a slight increase of the bulk doping which would be consistent with the diffusion of charged molecules into the bulk.
Comparing the effect of the annealing on the $C-f$ and $C-V$ characteristics one has to conclude that the off-plane charge carrier mobility is strongly enhanced by thermal annealing, a fact which can be correlated with the increase of crystallinity suggested by the XRD measurements. In the following table one can see the values of the different parameters characterizing the MIS diodes after annealing together with their percentual variation.
The annealing effect, as seen in the MIS diodes, has a strong influence on the structure of the bulk, leading to a higher degree of crystallinity, thus enhancing the off-plane charge carrier mobility by a factor of 200 times in the best case.

Table 6.5: Relaxation frequency-f_R, bulk doping-N_A, flat-band voltage-V_{FB} and off-plane mobility-$\mu_\perp$ for MIS diodes with different surface treatments after annealing, together with the their relative variation

Treatment	$f_R(Hz)$	$N_A(cm^{-3})$	$V_{FB}(V)$	$\mu_\perp(cm^2/Vs)$
Untreated	2190|400x	$7.2 \cdot 10^{15}\| + 2.4$x	$0.1\| + 0.2$	$2.5 \cdot 10^{-5}\|27$x
HMDS	1135|113x	$2.5 \cdot 10^{15}\| - 0.8$x	$0.2\| - 0.5$	$3.3 \cdot 10^{-5}\|137$x
OTS	667|95x	$5.8 \cdot 10^{15}\| - 0.8$x	$0.1\| - 0.1$	$8.9 \cdot 10^{-6}\|114$x
O_2 plasma	1488|248x	$3.0 \cdot 10^{16}\| + 1.25$x	$2.1\| - 1.5$	$2.3 \cdot 10^{-6}\|209$x

The figure 6.10 presents the effect of annealing on the transfer characteristics of FETs. One can notice that the annealing is mostly influencing the position of the switch-on voltage, meaning that the properties of the interface are strongly dependent on it. The magnitude and direction of the V_{SO} shift is not the same for all samples.

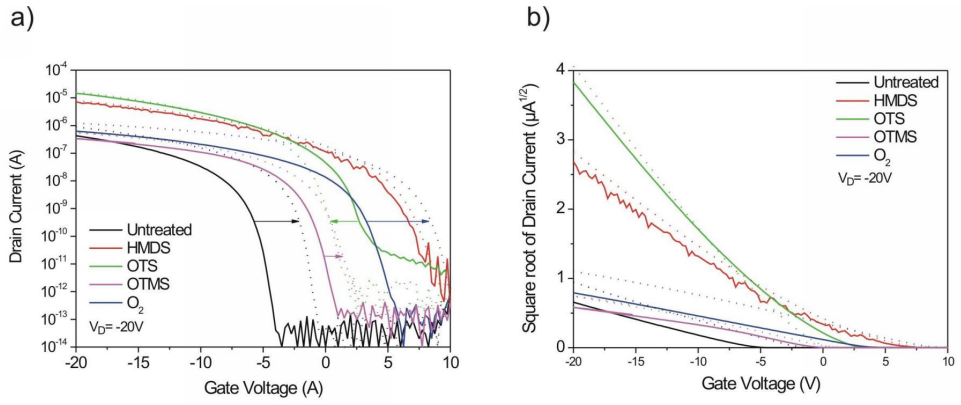

Figure 6.10: The influence of annealing on the transfer characteristics of FETs: (a) log-lin plot of $I_D - V_G$ and (b) square root of I_D vs. V_G, for the different substrate treatments

The FET on the untreated substrate shows a positive shift, whereas in the case of the OTS treated substrate the shift is negative. The HMDS treated FET does not change too much after annealing, while the V_{SO} of the O_2 plasma treated one increases dramatically. At the same time the field-effect mobility, the ON/OFF ratio and the subthreshold slope are slightly improved. The table 6.6 summarizes and compares the effect of annealing on the differently treated substrates.

It can be noticed that the structural ordering in the bulk of the films as controlled by thermal annealing has almost no influence on the field-effect mobility.
The effect of annealing on the charge carrier mobility in the case of MIS diodes and FETs is very different. While for the MIS diodes the perpendicular charge carrier mobility increases by up to four orders of magnitude, for the FETs it stays almost constant. Nonetheless between the charge carrier mobility of the two classes of devices there is a large difference between the in-plane charge carrier mobility and the off-plane one. This anisotropy of

Table 6.6: OFET parameters (saturation mobility μ_{sat}, threshold voltage V_T, switch-on voltage V_{SO}, On/Off ratio, subthreshold slope S) for the different surface treatments after annealing and their relative variation

Treatment	$\mu_{sat}(cm^2/Vs)$	V_T(V)	V_{SO}(V)	On/Off·10^7	S(V/dec)
Untreated	$2.2{\cdot}10^{-3}\|1.3x$	$-2.90\| + 3.4$	$-0.65\| + 3.41$	$2.6\|2.14x$	$0.36\| - 0.08$
HMDS	$1.3{\cdot}10^{-2}\|1x$	$0.90\| + 1.1$	$9.50\| + 2.00$	$1.9\|0.24x$	$0.85\| - 0.71$
OTS	$4.1{\cdot}10^{-2}\|1.2x$	$-2.75\| + 0.4$	$1.52\| - 2.13$	$1.7\|12.1x$	$0.62\| - 0.30$
OTMS	$1.1{\cdot}10^{-3}\|1.1x$	$-1.48\| + 1.4$	$2.41\| + 1.12$	$0.02\|1.3x$	$0.75\| - 0.50$
O_2 plasma	$8.7{\cdot}10^{-4}\|1.03x$	$12.64\| + 8.3$	$10.0\| + 3.75$	$4.0\|17.5x$	$0.49\| - 0.11$

the mobility is an indication of the lamellar structure, described at the beginning of the chapter, of highly ordered P3HT films, which will be discussed in more detail later.

6.6 Influence of solvent choice

In the following chloroform, toluene and dichlorobenzene were used as solvents for P3HT, field-effect transistors being prepared via spin-coating. Figure 6.11 shows a comparison of the output and transfer characteristics of the different FETs. The geometry of the transistors is the same in all the cases: L=5μm, W=1000μm, d_{ox}=200nm. Prior to the P3HT solution, the respective solvent was spin-coated on the substrates in order to create a monolayer.

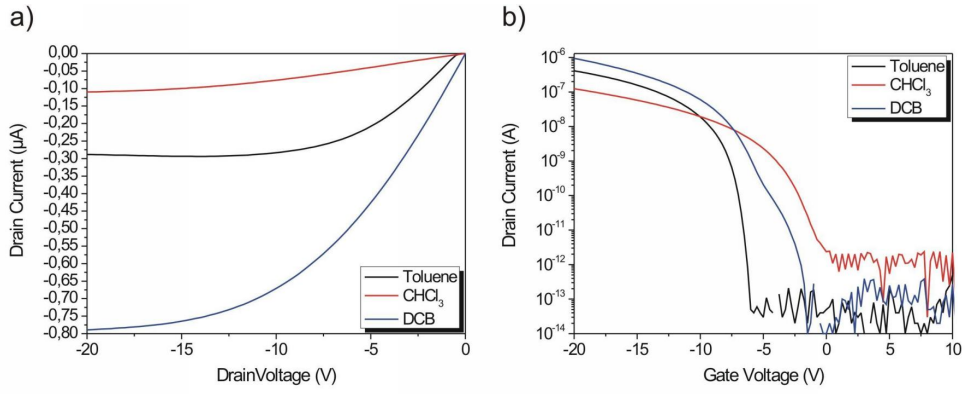

Figure 6.11: Comparison of three FETs prepared using different solvents (chloroform, toluene, dichlorobenzene): a) output and b) transfer characteristics

This has the purpose to firstly clean the substrates of any slight contamination which might have resulted during the transport from the clean-room to the glove-box system and

secondly to create a thin film of solvent on the substrate, so that the solution can wet the substrate better, leading to higher quality films.
The comparison of the output characteristics shows that the drain current scales with the solvent choice being directly proportional with the boiling point, as it can be seen in table (6.7). From the comparison of the transfer characteristics one can notice that the chloroform prepared FET has the highest off current, thus the smallest ON/OFF ratio, the most positive switch-on voltage and the largest subthreshold slope, meaning that the bulk doping in this case is high as well as the density of interface traps. The dichlorobenzene based FET shows a low off current, thus having the highest ON/OFF ratio, a slightly negative switch-on voltage. The shoulder like feature which begins at the switch-on voltage and extends till approximately -5V is a signature of bulk traps, as it has been shown by Scheinert *et. al.* [60]. This feature is retained even after annealing close to the glass temperature of P3HT ($\approx 150°C$), not shown here. The toluene FET has the most negative switch-on voltage, slightly lower maximum current than DCB, high ON/OFF ratio and the smallest subthreshold slope.
The parameters for the P3HT FETs prepared from solutions with different solvents are shown in the next table:

Table 6.7: Parameters of three FETs prepared using chloroform, toluene and dichlorobenzene as solvents (BP stands for boiling point and S for subthreshold slope)

Solvent	BP°C	$\mu(cm^2/Vs)$	$V_T(V)$	$V_{SO}(V)$	$S(V/dec)$
Chloroform	61	$2.5 \cdot 10^{-4}$	-0.76	0.25	1.1
Toluene	111	$1.8 \cdot 10^{-3}$	-3.22	-6.00	0.2
DCB	181	$3.0 \cdot 10^{-3}$	-6.71	-1.50	1.5

6.7 Conclusions

In this chapter, it has been shown that the charge carrier mobility in P3HT filed-effect transistors and MIS diodes depends very sensitively on the nature of the interface to the gate dielectric. Using silanization of the silicon oxide with different agents the field-effect mobility can be increased by almost two order of magnitude, reaching values of about $4 \cdot 10^{-2} cm^2/Vs$. A qualitative correlation between the intensity of the X-Ray diffraction peaks and the mobility can also be noticed. Interestingly, the structural ordering of the bulk of the films, as controlled by thermal annealing, does not have a major influence on the field-effect mobility in FETs, while in the case of MIS diodes it leads to an increase of the off-plane (bulk) mobility by two orders of magnitude.
Another important parameter for the performance of the semiconducting polymer based devices is the solvent choice. It has been shown that this alone can lead to an increase of the field-effect mobility of about one order of magnitude. The dependence of the field-effect mobility on the boiling temperature of the solvent has been shown, which would suggest that, for a given preparation set of parameters, its increase with the boiling point of the

solvent will eventually saturate. The next image, based on the values from table 6.7, shows the dependence of the mobility on the solvent's boiling point:

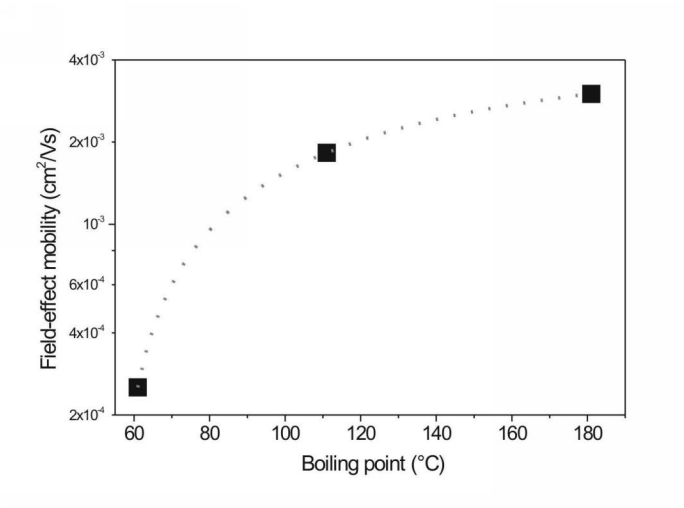

Figure 6.12: Dependence of field-effect mobility on the boiling point of the solvent; dotted line is a guide for the eye

The dotted line, which is only a guide for the eye, tries to emphasise that the mobility value might saturate at high values of the boiling point. Thus for a given set of parameters for the preparation of FETs there will be an upper for the limit mobility which can be reached, due to the film morphology which depends on the boiling point of the solvent.

Chapter 7

Charge carrier density dependent mobility

7.1 Temperature dependent mobility

In the previous chapters the characteristics of MIS diodes and FETs have been investigated at room temperature. This enabled us to have a look at the charge transport in the out of plane direction as well as in plane, with respect to the insulator surface. It has been found that there is a large difference between the mobility corresponding to the two cases. In order to get further insight into the charge transport mechanism in the different directions, the temperature dependent behavior of MIS diodes, FETs and SCL diodes has been measured and the model presented in section 1.3.5 is used to correlate the observed behavior. The accessed temperature range is between 220 and $\approx$ 400K. In the following the results for the MIS diodes and FETs with OTS modified SiO_2 will be presented and in the end a comparison with devices where other oxide surface modifications were employed will be shown.

Figure 7.1(a) shows the temperature dependent capacitance-frequency characteristics of an OTS modified MIS diode. It is worth noting that there is a large shift of the curves along the frequency axis with temperature, thus indicating that the relaxation frequency shifts also a lot as it can be seen in figure 7.1(b). At the same time the increase of the capacitance at low frequencies over the oxide capacitance value scales somewhat with the temperature, but not as strong as the relaxation frequency. In the previous chapters this increase of the capacitance has been associated with a high in-plane mobility which leads to a pseudo increase of the area of the active contact. As this effect is not very strong with the temperature this gives a hint that the variation of the in-plane mobility is not so strong. From the capacitance-voltage characteristics, not shown here for brevity, the values of the doping have been extracted as the are required for the calculation of the perpendicular mobility. The variation of N_A is not very strong, merely doubling its value at high temperatures. Thus, the strong shift of f_R directly reflects a strong temperature dependence of the perpendicular mobility in MIS diodes.

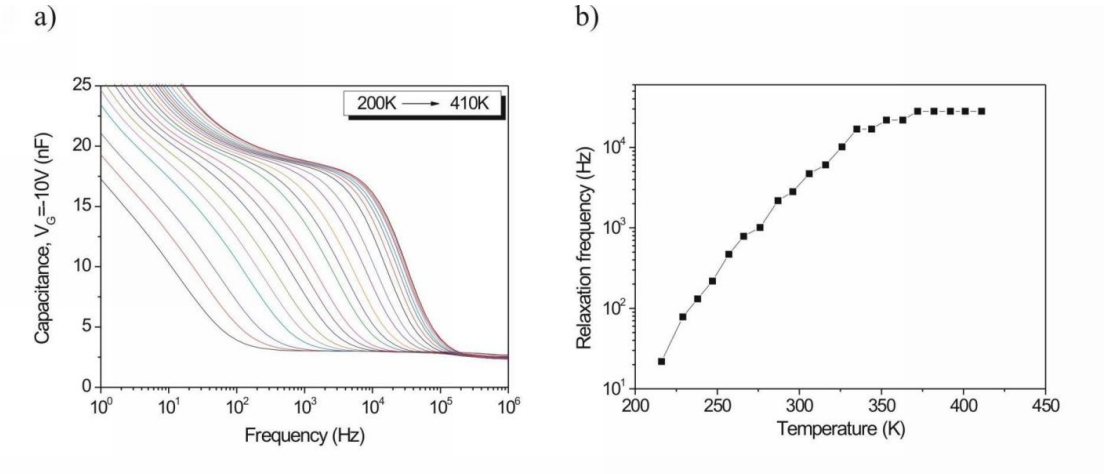

Figure 7.1: Temperature dependence of the capacitance-frequency characteristics of an OTS treated MIS diode (a) and of the determined relaxation frequency (b), in the 200 to 410K range

Contrarily, in FETs (see figure 7.2) the current at large gate voltage changes by only a factor of two over the whole temperature range (220-400K) indicating a very weak temperature dependence of the field-effect mobility parallel to the substrate. Even if the temperature is lowered to ≈ 100 K (not shown here) the mobility stays at $\approx 10^{-2}$ cm^2/Vs. This indicates that the charge transport in the monolayer near the organic semiconductor-SiO_2 interface is similar to a band-like transport due to the high degree of organization of the P3HT molecules. The shift of the switch-on voltage is not very high either.

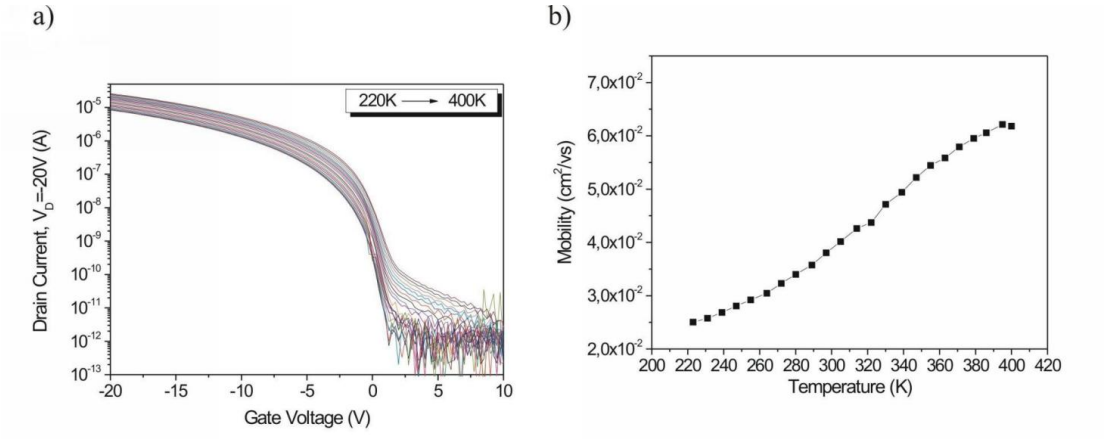

Figure 7.2: Temperature dependence of the transfer characteristics of an OTS treated FET (a) and of the determined field-effect mobility, in the 200 to 410K range

As the switch-on voltage relates directly to the value of the doping near the interface it

means that the interface is stable with temperature. The bulk current increases somewhat with the temperature as well as the subthreshold slope showing that the amount of charge is increasing, probably due to charge being released from bulk traps. This is also consistent with the slight increase of the bulk doping noticed in the MIS diodes.
The next figure shows the variation of the current density with temperature of SCLC diodes. The curves were measured between 140 and 304K.

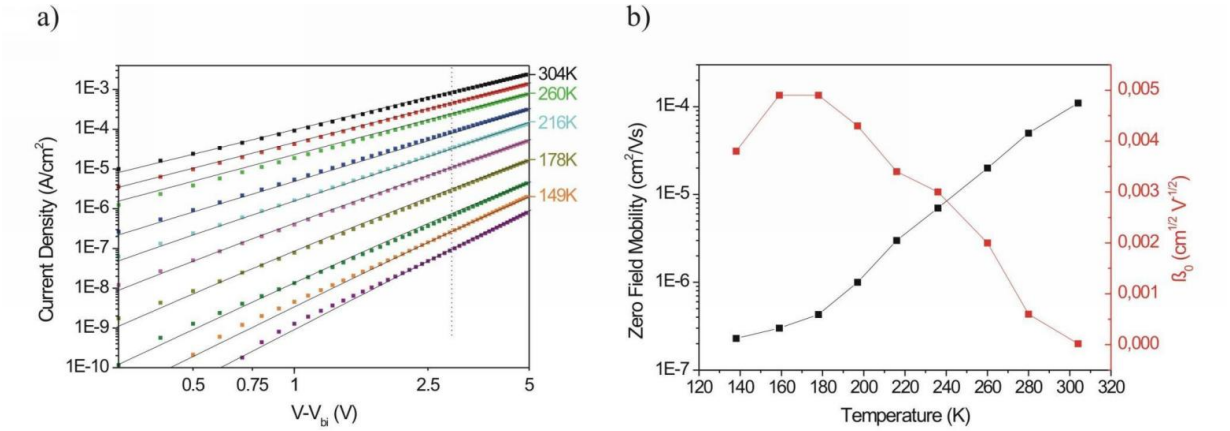

Figure 7.3: Temperature dependence of the (a) current density in SCLC diodes and (b) parameters μ_0 and β

It can be seen that, like in the case of the MIS diodes, the variation of the current density with the temperature is high, extending over a few orders of magnitude. The *J-V* characteristics were analysed using a numerical simulation program [61], therefore they corrected for the built-in voltage ($\approx$ 0.1eV). An empirical field and temperature dependent charge carrier mobility following a Poole-Frenkel behaviour

$$\mu(V,T) = \mu(T) \cdot exp\left(\beta(T)\sqrt{V}\right) \tag{7.1}$$

were considered. Additionally, a trap distribution centered at 210meV above the hole transport level (having a Gaussian width σ_G=60meV and a total density of 9x10^{15}cm^{-3}) had to be taken into account to get a satisfactory fit over the whole temperature range. Using these parameters the values for the μ(T) and β(T) were determined for each curve. The strong variation of the current density with the temperature is directly correlated with the strong variation of the mobility. The β factor has a moderate variation and if one which is understandable if one thinks it is a measure of the disorder in the system.
In figure 7.4 the comparison between the Pasveer model [11], presented in 1.3.5 and the temperature dependence of the mobility in OTS MIS diode and FET is presented. The required parameters are a hopping distance of 1.4 nm and a disorder parameter σ = 100 meV which are in going with the numbers given in Ref. [62]. The prefactor for the hopping mobility is adjusted to give the best agreement with our data for the MIS diode.

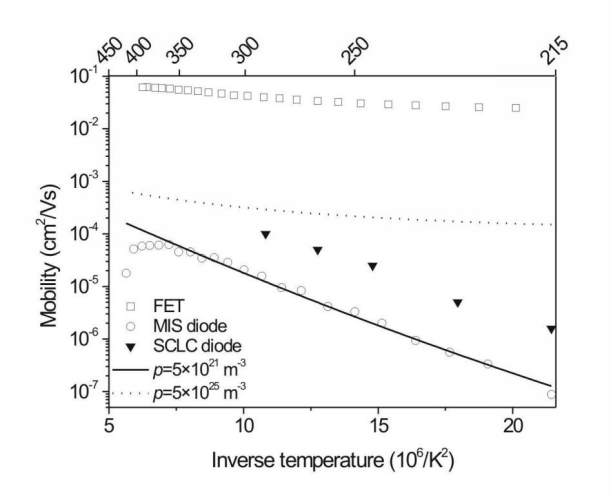

Figure 7.4: Comparison of mobility of the OTS FET, MIS diode and of the SCLC diode with the predictions of an analytical model for carrier density dependent hopping transport. The used parameters are: width of the DOS σ = 98 meV, intersite spacing a = 1.4 nm, p_{MIS} =5 · 10^{21} m^{-3}, p_{SCLC} =8 · 10^{20} m^{-3}, p_{FET} = 5 · 10^{25} m^{-3}

Since there are no other free parameters in this model, the only difference between MIS diodes and FETs lies in the charge carrier densities. For the simulation we have taken the value of the doping N_A= 5 ·10^{15} cm^{-3} for the MIS diode and the estimated density of field-effect induced carriers at V_G=-20 V of about 5·10^{19} cm^{-3} (in agreement with Ref. [62]). The comparison shows that the different temperature dependencies of the mobility in MIS diodes and FETs are qualitatively reproduced by the isotropic hopping model; however, there is a quantitative difference of about two orders of magnitude by which the experimentally observed FET mobility is higher than predicted by this model.
In the following the transfer characteristic of the OTS treated FET, at room temperature, has been measured in the linear regime, at V_D=-1V (see figure 7.5(b)). The mobility for the entire gate bias range has been calculated using the the expression (1.35) of the drain current in the linear regime. The charge carrier density value for each V_G has been calculated integrating equation (1.40) over the conductive channel thickness (2nm). In the case of the MIS diode the carrier concentration is constant being given by the the doping value determined from the capacitance-voltage characteristic ($\sim$ 3·$10^{15}$$cm^{-3}$). The carrier concentration in the hole-only diode is directly proportional to the applied bias given by the following relation:

$$\rho_{SCLC} = \frac{3}{4}\frac{\epsilon_0 \epsilon_{semi}}{qL^2}V \tag{7.2}$$

where L is the thickness of the hole-only diode and V is the applied bias.

The dependence of the FET mobility on the charge carrier density has been fitted to the Pasveer model (see figure 7.5(a)), resulting in the following parameters: σ=70meV, a=0.5nm and it has been extended to lower values of the charge carrier density.

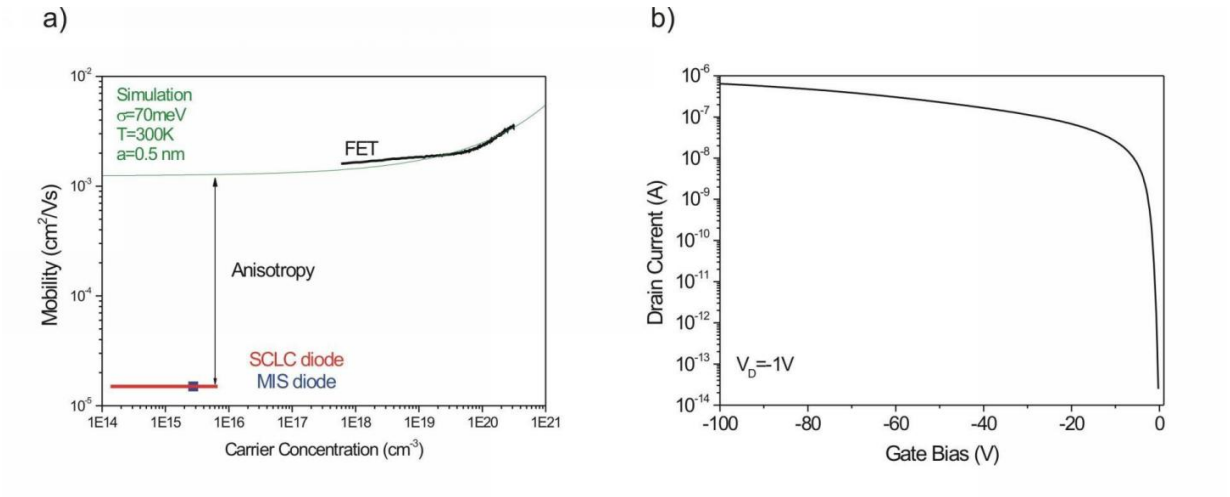

Figure 7.5: Charge carrier density dependence of the field-effect mobility, bulk mobility of the MIS diodes for the different substrate treatments and mobility of SCLC diodes (a) and transfer characteristic (b) of an OTS FET in the linear regime, V_D=-1V

The values obtained this way are clearly smaller than the values obtained from the fit of the temperature dependent mobility of the MIS diode, performed earlier.
The difference between the two σ values shows that the in the FET the charge carrier transport takes place in a more ordered medium than in the case of the MIS or hole-only diode. At the same time the lattice constant a is about three time smaller for the FET, meaning that the molecules are more closer packed, which is in going with the structural order of P3HT. From figure 7.5 it is clear that the model does not describe very well transport in P3HT based devices, as between the in-plane direction and the off-plane direction there is a strong structural and electrical anisotropy.
A comparison between the temperature dependence of the mobility of the MIS diodes, the field-effect transistors with different oxide treatments and SCLC diodes is shown in figure 7.6. It can be seen that the difference in mobility values between FETs and MIS diodes and SCLC diodes, respectively, amounts to several orders of magnitude for all the samples. At the same time the mobility of the OTS treated MIS diode is comparable with the one of the SCLC diode, while the difference becomes larger for the other MIS devices, following a similar strong dependence of temperature. This shows once again that the high degree of order found at the semiconductor-insulator interface has only a weak influence on the morphology of the bulk of the P3HT layers. Contrarily the FET mobility is strongly affected by the quality of the interface leading to a very weak temperature dependence and a variation of the absolute values over a few orders of magnitude.

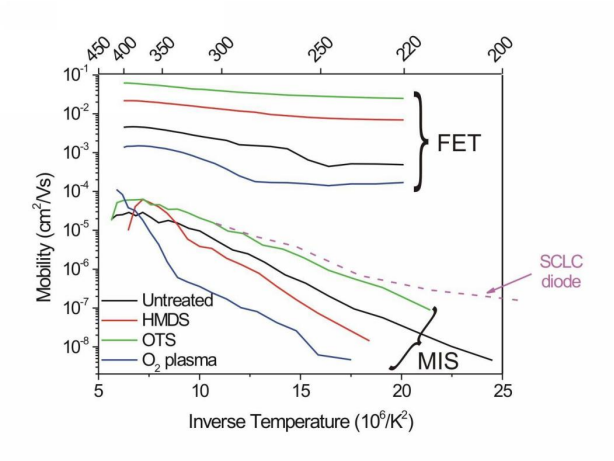

Figure 7.6: Temperature dependence of the field-effect mobility, bulk mobility of the MIS diodes for the different substrate treatments and mobility of SCLC diodes

7.2 Conclusion

Together with the results regarding the big differences between the in-plane (FET) and out of plane (MIS) mobility presented in chapter 6 the above comparison with the isotropic hopping model developed by Pasveer at al. is a convincing argument for a true electrical anisotropy of transport in P3HT films. The temperature dependent mobility data for both types of devices clearly show that charge carrier transport parallel and perpendicular to the dielectric interface can not be described by an isotropic hopping model. Thus, highly ordered films of rr-P3HT, owing to their lamellar structure, display a true electrical anisotropy which emphasises the importance of the first few monolayers of the film for charge transport even more. The picture 7.7 shows that the P3HT molecules organize themselves so that the side chains are perpendicular to the semiconductor-insulator interface, thus promoting a *band-like* charge transport in the x direction, showing a small dependence on temperature of the mobility, while the bulk is disordered leading to charge transport governed by *hopping*, with a strong dependence on temperature of the mobility.

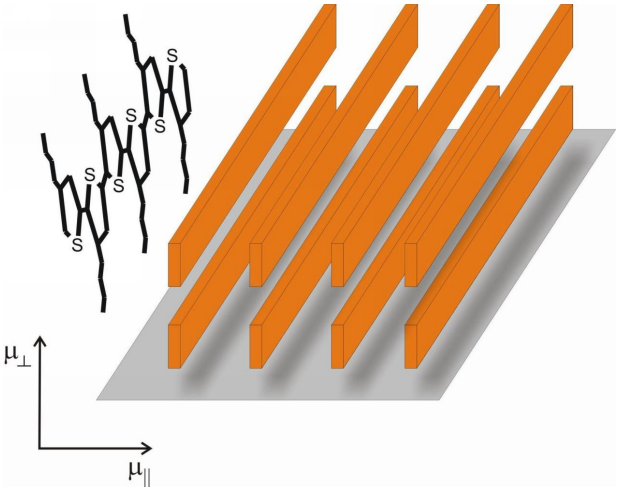

Figure 7.7: Schematic representation of the organization of the P3HT molecules near the P3HT-insulator interface

Summary

In the last few years the importance of organic electronic devices become larger and larger, as they came out of the lab and entered the consumer market. Even if their performance cannot match the one of the inorgannic devices there are fields like flexible displays, radio-frequency identification tags, chemical or optical sensors where organic devices can compete due to their low cost, ease of processability and the posibility to place the electronics on flexible substrates.
In this work, devices based on poly(3-hexyl)thiophene have been prepared and the influence of various processing parameters has been investigated. The *first chapter* explains in detail the theoretical aspects of the different devices and expressions for the various quantities involved are deduced. Firstly, the expression of the capacitance of the MIS diode and its dependence on the applied frequency and bias is derived. The different operation regimes of the inorganic MIS are analyzed and the differences to the organic ones are explained. As FETs are quite similar to the MIS diodes, from a structural point of view, part of the theory developed for the diodes can be used to compute expressions describing the current flow in the transistors.
In addition, a recent model by Pasveer et al. [11], which assumes the charge carrier mobility depends on the charge carrier concentrations is introduced at the end of the chapter. This is a very important concept as it allows one to describe within a single model the charge transport in the previously mentioned devices. The applicability of this model, for P3HT devices will be analyzed in chapter seven.
In the end various models describing the influence of traps and doping on the charge transport in hole-only diodes are presented. In chapter seven, one of these models is used for the evaluation of the measured data.
The *second chapter* describes the various organic materials involved in the fabrication of devices. For each kind of device its structure and preparation method(s) are described in detail. The last section of this chapter gives a detailed overview of the instruments, machines and methods employed in the measurements.
The *third chapter* shows how the measured data has been analyzed and what approximations were made, if any.
The *fourth chapter* presents the results obtained for MIS diodes and FETs with different organic and inorganic gate insulators. Various factors which are influencing the performance of the devices are pointed out.
The influence of air and light on the performance of MIS diodes and FETs is investigated

in the *fifth chapter*. These can modify strongly the electrical characteristics of the devices through doping and reversible or irreversible oxidation.
The *sixth chapter* presents methods used to improve charge transport in devices based on P3HT. Firstly the influence of self-assembled monolayers (SAM), deposited on silicon dioxide, on the structure and electrical properties of the semiconductor layer is presented. In general, the presence of a SAM on a surface will alter its energy. In particular octadecyltrichlorosilane (OTS) or hexamethyldisilazane (HMDS) will lower the surface energy of the silicon. Thus, during the formation of the P3HT film on such a surface, from solution, the molecules will have more freedom to reorganize. The P3HT layer, formed by spin-coating from solution, has been shown to self-organize in such a way that the lateral chains are oriented perpendicular to the substrate, thus forming crystalline domains. If the surface energy is reduced then the size of these domains will increase resulting in better electrical properties of the devices. Another process step which improves the performance of FETs and MIS diodes is the post spin-coating annealing. The last parameter which has a major influence on charge transport in devices is the solvent choice as the kinetics of film formation is influenced by the vapour pressure of the solvent.
In the end, in *chapter seven* the temperature dependent behaviour of devices prepared employing SAMs is analyzed. It is found that the mobility values determined for FETs and MIS diodes are differing by few orders of magnitude. This, together with X-Ray diffraction analysis, gives a hint toward a structural anisotropy between the bulk and the interfacial layer in a P3HT film. This assumption is further checked using a recent model developed by Pasveer et al.[11]. The model, described in detail in chapter one, is assuming that the mobility is charge carrier density dependent and for isotropic systems it is proven to be able to describe the charge transport in both FETs and hole-only diodes. As this model, which assumes an isotropic structure of the material, is not valid for FETs proofs also that there is a strong electrical and structural anisotropy in these devices.

Zusammenfassung

Die Bedeutung organischer elektronischer Bauteile nahm in den letzten Jahren durch die Überführung von Laborprototypen zur Marktreife und ihren Einzug in Konsumgüter mehr und mehr zu. Auch wenn die organischen Bauteile leistungsmäßig nicht ganz mit ihren anorganischen Pendants mithalten können, gibt es Bereiche wie flexible Displays, Radiofrequenz-Identifizierungs-Etiketten ("RF-ID-Tags"), chemische oder optische Sensoren, usw., in denen die organischen Bauteile aufgrund ihrer geringen Herstellungskosten, ihrer leichten Verarbeitbarkeit und der Möglichkeit, elektronische Schaltungen auf flexiblen Substraten aufzubringen, konkurrenzfähig sind.
In dieser Arbeit wurden Bauteile, die auf Poly(3-Hexyl)thiophen (P3HT) basieren, hergestellt und der Einfluss verschiedener Prozessparameter auf deren Eigenschaften untersucht. Im ersten Kapitel wurden die theoretischen Grundlagen der unterschiedlichen Bauteile detailliert beschrieben und die zur Bauteil-Beschreibung benötigten Gleichungen hergeleitet, wie zuerst der Ausdruck für die Kapazität der Metall-Isolator-Halbleiter-Struktur (MIS)-Diode in Abhängigkeit von der angelegten Frequenz und Durchlassvorspannung ("Bias"). Die unterschiedlichen Arbeitsbereiche der anorganischen MIS-Diode wurden untersucht und die Unterschiede zur organischen Variante erläutert.
Da Feldeffekttransistoren (FET) strukturell den MIS-Dioden sehr ähnlich sind, konnte ein Teil der für die Dioden hergeleiteten Theorie verwendet werden, um Ausdrücke abzuleiten, die den Stromfluss in den Transistoren beschreiben. Weiterhin wurde ein erst kürzlich entwickeltes Modell von Pasveer et al. [11] vorgestellt, in dem angenommen wird, dass die Ladungsträgerbeweglichkeit von der Ladungsträgerkonzentration abhängt. Dies ist ein sehr wichtiges Konzept, da es einem mit einem einzigen Modell erlaubt, den Ladungstransport in den erwähnten Bauteilen zu beschreiben. Die Anwendbarkeit dieses Modells auf die P3HT-Bauteile wurde in Kapitel 7 untersucht.
Zum Schluss des Kapitels wurden verschiedene Modelle vorgestellt, die den Einfluss von Störstellen und der Dotierung auf den Ladungstransport in Nur-Lochleitungs-Dioden beschreiben. In Kapitel 7 wurde eines dieser Modelle zur Auswertung der Messdanten verwendet.
Das zweite Kapitel beschrieb die unterschiedlichen organischen Materialien die bei der Herstellung der Bauteile verwendet wurden, und detailliert die Struktur jeder Bauteil-Art und die Präparationsmethoden. Der letzte Abschnitt dieses Kapitels gab eine genaue Übersicht über die bei den Messungen verwendeten Anlagen und Methoden. Das dritte Kapitel zeigte, wie die gemessenen Daten ausgewertet wurden und - falls dies der Fall war

- welche Näherungen verwendet wurden.
Im vierten Kapitel wurden die Ergebnisse von MIS-Dioden und FETs mit unterschiedlichen organischen und anorganischen Gate-Isolatoren vorgestellt. Verschiedene Faktoren, die die Leistung der Bauteile beeinflussen, wurden aufgezeigt. Der Einfluss von Luft und Licht auf die Leistung der MIS-Dioden und FETs wurde im fünften Kapitel untersucht. Luft und Licht können durch Dotierung und reversibler oder irreversibler Oxidation die elektrischen Eigenschaften der Halbleitermaterialien deutlich verändern.
Das sechste Kapitel präsentierte Methoden zur Verbesserung des Ladungstransports in P3HT-basierten Bauteilen. Zuerst wurde der Einfluss von auf Siliziumdioxid abgeschiedenen selbstordnenden Monolagen (self-assembled monolayers, SAM) auf die strukturellen und elektrischen Eigenschaften der Halbleiterschichten vorgestellt. Im Allgemeinen wird die Präsenz einer SAM auf einer Oberfläche deren Energie ändern. Im Speziellen reduzieren Octadecyltrichlorosilan (OTS) oder Hexamethyldisilazan (HMDS) die Oberflächenenergie des Siliziums. Daher haben die Moleküle bei der Bildung eines P3HT Films aus der Lösung auf so einer Oberfläche eine größere Freiheit sich zu reorganisieren.
Wie sich zeigte, führt die Selbstorganisation in einer durch Spin-Coating aus der Lösung gebildeten P3HT-Schicht dazu, dass die lateralen Molekülketten senkrecht zum Substrat ausgerichtet sind und sich dadurch kristalline Domänen ausbilden. Wird die Oberflächenenergie reduziert, so nimmt die Größe dieser Domänen zu was wiederum zu besseren elektrischen Eigenschaften der Bauteile führt.
Ein weiterer Prozessschritt, der die Leistung der FETs und MIS-Dioden verbessert, ist das thermische Ausheilen nach dem Spin-Coating. Einen starken Einfluss auf den Ladungstransport hat auch die Wahl des Lösungsmittels, da die Kinetik der Film-Bildung von dessen Dampfdruck abhängt.
Am Schluss, in Kapitel 7, wurde das temperaturabhängige Verhalten von Bauteilen mit SAMs untersucht. Es zeigte sich, dass sich die ermittelten Beweglichkeiten der FETs und MIS-Dioden um einige Größenordnungen unterschieden. Zusammen mit röntgendiffraktometrischen Untersuchungen gab dies einen Hinweis auf das Vorhandensein einer strukturellen Anisotropie zwischen dem Vollmaterial (bulk) und der Grenzflächenschicht in den P3HT Filmen.
Diese Annahme wurde mit dem in Kapitel 1 beschriebenen Modell von Pasveer et al. weiter untersucht, Das Modell setzt voraus, dass die Beweglichkeit ladungsträgerabhängig ist, und für isotropische Systeme wurde bewiesen, dass es den Ladungstransport sowohl in FETs, als auch in Nur-Lochleitungs-Dioden beschreiben kann. Da dieses Modell, das eine isotropische Struktur voraussetzt, das Verhalten der P3HT FETs nicht beschreiben kann, ist die starke strukturelle und elektrische Anisotropie in P3HT-basierten Bauteilen gezeigt.

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