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Charge carrier transport in organic field-effect devices based on copper-phthalocyanine

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Chapter 1

Motivation

Every day's presence of electronic devices has been increasing drastically for the last two or three decades. Fighting against saturation of markets, one of today's major challenges for industry is the development of new fields of application—the so-called "ubiquitous electronics". Examples are large-area devices or flexible constructions for displays, photovoltaic cells or light sources. This cannot be achieved easily with classical inorganic semiconductors like silicon, germanium or compound semiconductors like gallium arsenide or gallium nitride as active materials although some success has been reported on flexible thin-film transistors based on amorphous oxides [1]. Thus, a new class of electronics, which is very promising for these kinds of applications, is under intensive research: organic electronics. Herein, organic materials that exhibit semiconducting properties are used instead of inorganic semiconductors. For the last couple of years tremendous progress has been achieved in this field of research. Three types of devices are especially promising: organic light-emitting diodes (OLEDs), organic photovoltaic cells (OPVCs) and organic field-effect transistors (OFETs). Out of these three classes, OLEDs and OPVCs are already marketable. One of the outstanding features of OLEDs is the possibility to fabricate large area light sources in contrast to the point-shaped inorganic light-emitting diodes [2]. OPVCs play an important role in research at the moment and efficiencies up to 8.3% have been achieved recently [3, 4]. Field-effect transistors (FETs) are crucial for the realization of logic circuits, e.g. in computers or displays. The first OFET was reported in 1984 [5]. Since this publication the performance of OFETs has increased dramatically and nowadays performance data comparable to amorphous silicon FETs are reported [6]. OFETs are considered to be promising

candidates for the realization of flexible displays (E-paper) [7] or radio-frequency identification (RFID) tags used as passive electronic devices for the contact-free identification of products or objects [8, 9].

Generally, there are two classes of materials used for organic electronics: polymeric and molecular materials (often referred to as "small molecule semiconductors") [6]. Although these materials are semiconductors, the physical properties are different to their inorganic counterparts and not yet understood in all details. Thus, research concerning investigation of physical processes leading to charge carrier transport in these materials is still carried out.

OFETs are known to be a powerful tool for fundamental analysis [10]. This work concentrates on a typical feature of many molecular organic semiconductors: ambipolar charge carrier transport. Ambipolar transport is the transport of positive and negative charge carriers (i.e. holes and electrons, respectively) in the active material at the same time. This effect has also been observed in inorganic semiconductors, but has not yet been applied technologically. Possible applications for ambipolar OFETs are light-emitting OFETs (LEOFETs) [11, 12] or complementary logic circuits where both the *p*- and the *n*- channel are based on the same substrate [13]. In the 1970s and 1980s, it has been demonstrated by time-of-flight measurements on highly pure organic semiconductor crystals that ambipolar charge carrier transport in organic semiconductors is possible and that there is no fundamental difference between the transport of electrons and holes [14]. However, when organic semiconductors have been applied to thin-film devices in the late 1980s and the 1990s, they have usually been classified as either *p*-type or *n*-type. Nowadays it is known that charge carrier traps or injection barriers are possible reasons for the suppression of one charge carrier type. Today, highly pure materials are available and ambipolar charge carrier transport can be observed in numerous organic semiconductors. Nevertheless, there is a pronounced asymmetry between both charge carrier types in most cases, which is counterproductive for the realization of high-performance devices. In the scope of this thesis it can be seen that this asymmetry is affected strongly by various parameters, e.g. substrate material, substrate treatment or morphology of the semiconductor.

This thesis gives a systematic study of ambipolar charge carrier transport in field-effect devices based on the organic semiconductor copper-phthalocyanine.

Chapter 2

Background

The following chapter provides a short introduction into organic semiconductors. Thereafter, the fundamental basics of field-effect devices will be explained by means of a metal-insulator-semiconductor diode. Finally, the working principles of organic field-effect transistors will be discussed with the help of a model for ambipolar charge carrier transport.

2.1 Introduction to organic semiconductors

As already mentioned in the introduction there are two classes of organic semiconductors: polymers and molecular materials. Since the fundamental properties of both types are similar and since only molecular materials are used as organic semiconductors in the course of this thesis, the following section will only concentrate on this class.

Delocalized π-electron systems

Organic semiconductors consist of organic materials which exhibit semiconducting properties. The shape and the size of these molecules can vary drastically from relatively small molecules like anthracene, shown in fig. 2.1(a) over larger molecules like copper-phthalocyanine depicted in fig. 2.1(b), which will be studied intensively in this thesis, to very large and complex molecules.

A common feature of all organic semiconductors is the presence of a conjugated

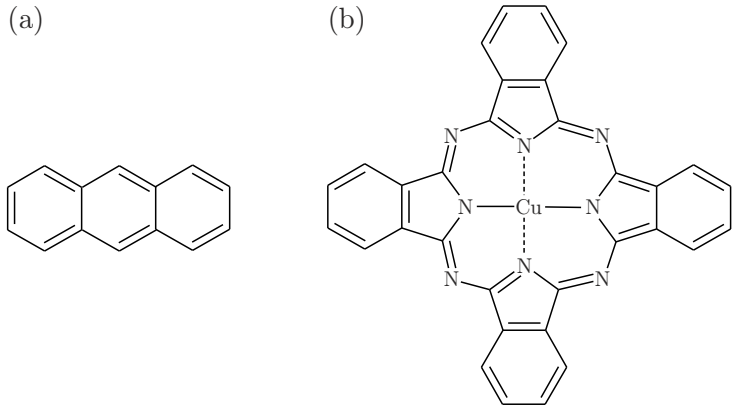


Figure 2.1: Molecular structure of two organic semiconductors: (a) anthracene and (b) copper-phthalocyanine.

π-electron system. The formation of this system can be explained by the electronic configuration of the binding carbon atoms [15]. The electronic configuration of a free carbon atom is $1s^2\,2s^2\,2p^2$, i.e. the 1s, 2s and 2p orbitals are occupied by two electrons. When two carbon atoms are bound via a double bond, an sp^2-hybridization is formed (see fig. 2.2(a)). One s- and two p-orbitals (p_x and p_y) form three coplanar degenerated orbitals. Thus, a σ-bond between two neighboring carbon atoms is formed. The two p_z-orbitals remain perpendicular to this plane. Two neighboring p_z-orbitals are overlapping and the so-called π-bond is generated, as depicted in fig. 2.2(b). The electrons in this orbital are delocalized. Due to the interaction with the unpaired electron of the neighboring carbon atom, a splitting of the energy level takes place and a bonding π- and an antibonding π^*-orbital are formed, which are referred to as highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO), respectively. This effect is depicted in fig. 2.2(c).

In organic molecular solids each of these orbitals has a slightly different energy value due to the stochastic variation of polarization energies. This leads to an energetic distribution of the HOMOs and LUMOs of the individual molecules. The strength of the π-bond is relatively weak compared to the σ-bond because the p_z-orbitals show a less pronounced overlap than the sp^2-hybridized orbitals. Thus, molecular solids with delocalized π-electron systems show electronic excitation energies in the range of one to several eV. This corresponds to the transition of an electron from the HOMO to the LUMO.

HOMO and LUMO can be seen as analogs to valence and conduction band in inorganic semiconductors, respectively. However, an important difference to inorganic semiconductors is the fact that HOMO and LUMO do not form extended band

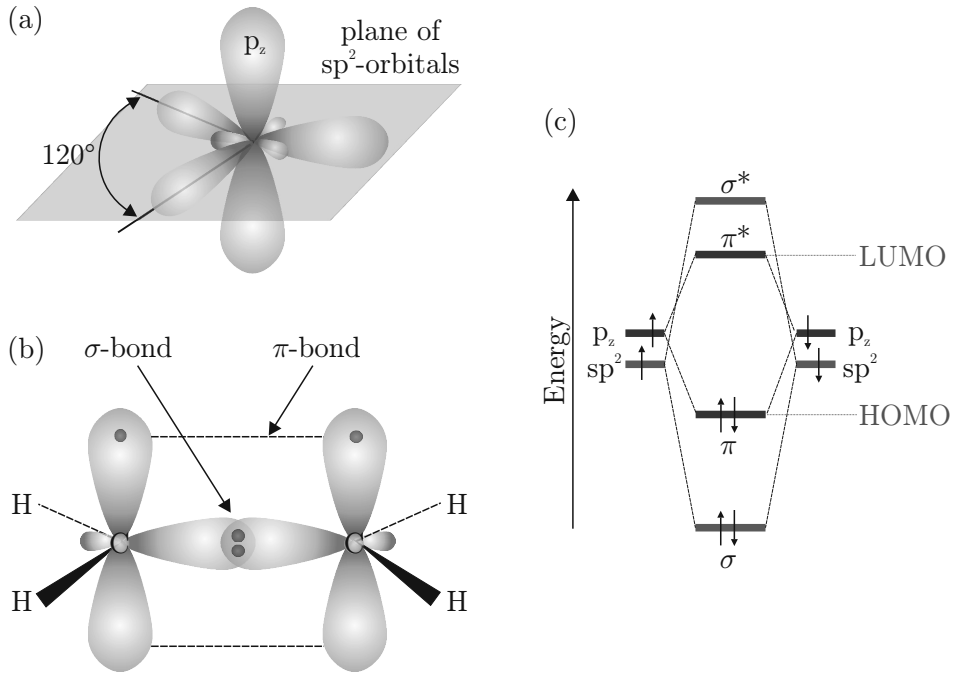


Figure 2.2: Schematic sketch of the sp^2-hybridization (a) and the formation of σ- and π-bonds (b). (c) Energy level diagram illustrating the bonding and anti-bonding molecular orbitals.

states at fixed energies but localized states with a given energetic distribution. It is assumed that charge carrier transport occurs via hopping of charge carriers from one site to another. One hopping step is an inter-molecular tunneling process of a charge carrier.

The active layer in most organic electronic devices consists of one or more thin films of organic semiconductors. These films can be amorphous or polycrystalline. Apart from thin films, also highly pure single-crystals of organic semiconductors are under intensive research. In this case, band-like transport behavior has been observed [16, 17].

Charge carrier transport

There exist many different models for the mathematical description of the energetic distribution of charge transporting states in the HOMO or LUMO [18–20]. The model presented by Bässler is the most simple one for hopping transport. The density of states (DOS) of the localized sites in the HOMO and LUMO is assumed to be Gaussian-like. This model holds for disordered organic semiconductors like amorphous polymers. However, for polycrystalline materials, the multiple trap-

ping and release (MTR) model is supposed to be more suitable. It is based on the assumption that the broadening of the DOS in polycrystalline organic semiconductors is significantly lower than for amorphous materials and can be described by an exponential function [21]. The mobility edge, a defined energy in the DOS, separates mobile from localized states [22] and the charge transport can be described by the effective transport level of the mobile states and a distribution of trap states extending into the band gap [23]. There are many different approaches to calculate these trap distributions [24–26]. All models are based on the fact that the charge carrier transport is thermally activated in polycrystalline organic semiconductors. This results in a temperature dependence of the charge carrier mobility following the law

$$\mu(T) = \mu_0 \cdot \exp\left(-\frac{E_\mathrm{a}}{k_\mathrm{B}T}\right), \tag{2.1}$$

where E_a is an activation energy, k_B denotes the Boltzmann constant and T the temperature. The definition of the mobility prefactor μ_0 depends on the respective model.

Trap states

In polycrystalline organic semiconductor layers there can be many different kinds of charge carrier traps that influence charge carrier transport heavily. Possible traps are impurities, dopants, defects or interfacial traps. Impurities can get into the organic semiconductor during synthesis of the material. The effect can be a drastically reduced device performance with low charge carrier mobilities and, especially in FETs, a poor on-off ratio or pronounced hysteresis. All organic semiconductors used in the experiments for this thesis have been purified by gradient sublimation at least once prior to use in order to avoid or reduce impurities. Dopants are impurities that enhance transport of one charge carrier type but suppress transport of the other. They can be incorporated into the film during fabrication (intentionally or unintentionally), measuring or storage. For example, oxygen doping of ambipolar OFETs can enhance hole transport but suppress electron transport [27] as will be shown in sec. 6.2.4. A common feature of all OFETs is the interface between the organic semiconductor and the insulator. It has been shown that the surface of the insulator can provide electron traps [28]. The role of these traps will be discussed in the experimental section.

Effects of grain boundaries

Another important origin of traps are defects in the crystal lattice [29, 30]. Since most molecular organic semiconductors are no single-crystals but polycrystalline

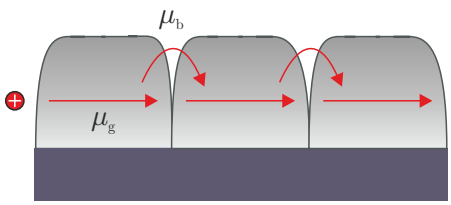


Figure 2.3: Schematic sketch of charge carrier transport in a polycrystalline film. Transport in the grains is determined by the intra-grain mobility μ_g whereas transport between the grains is limited by hopping across the grain boundaries with μ_b.

layers, there are many grain boundaries in the film. Charge carrier transport in polycrystalline films (shown schematically in fig. 2.3) is determined by two contributions: *intra*-grain transport with a relatively high mobility μ_g and tunneling processes across grain boundaries, referred to as *inter*-grain transport, with a considerably lower mobility μ_b. The overall mobility μ of the film can be written as [31]

$$\frac{1}{\mu} = \frac{1}{\mu_g} + \frac{1}{\mu_b}. \tag{2.2}$$

In many cases, the intra-grain transport is much more efficient—sometimes even band-like—than the inter-grain transport, leading to the relation $\mu_g \gg \mu_b$. Hence, the overall transport is limited by the inter-grain mobility μ_b.

2.2 Organic field-effect devices

2.2.1 Metal insulator semiconductor diodes

The physical principles of the field-effect are explained in this section with the help of metal-insulator-semiconductor (MIS) diodes. Fig. 2.4(a) depicts the schematic layout of an MIS diode. MIS diodes are the most simple devices to observe the field-effect. They are very useful to study properties of semiconductors in general, e.g. charge carrier transport perpendicular to the substrate plane. An MIS diode consists of a conducting back contact (gate), in our case a highly p-doped silicon wafer. On top of the conducting layer is the dielectric, in our case SiO_2. Thereupon is the semiconducting film followed by a metal top contact. For device operation, the top contact is connected to the ground potential and a voltage V_g is applied to the gate.

In the following, the working principle of an ideal inorganic MIS diode with a p-type semiconductor will be explained. Fig. 2.4(b) shows the corresponding energy band

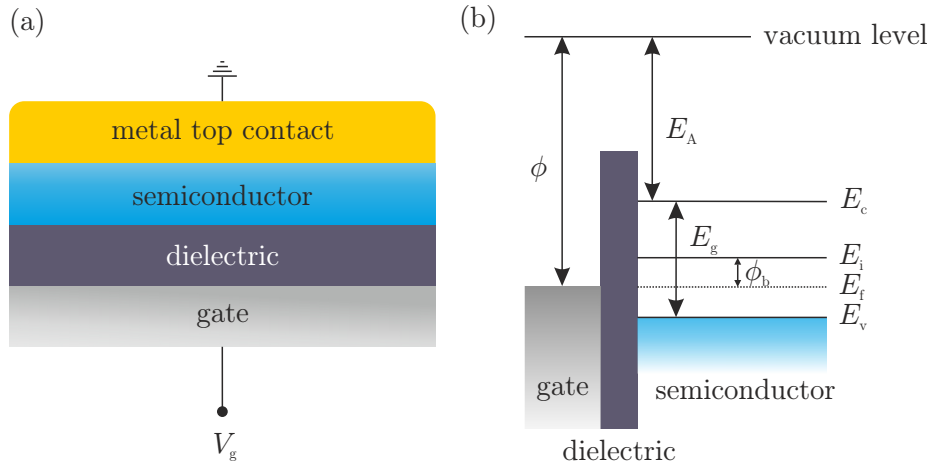


Figure 2.4: (a) Schematic layout of an MIS diode, (b) energy band diagram of an ideal MIS structure at equilibrium.

diagram at zero applied voltage. Here, ϕ is the work function of the gate electrode. E_A denotes the electron affinity of the semiconductor, E_g its bandgap and ϕ_b the potential difference between the Fermi level E_f and the intrinsic Fermi level E_i [6]. E_v and E_c denote the valence and the conduction band, respectively. In this case, the following equation is fulfilled:

$$\phi - \left(E_A + \frac{E_g}{2} + \phi_b \right) = 0. \tag{2.3}$$

The insulator forms a barrier between gate and semiconductor so that there can be no charge carrier flow and the Fermi level remains constant in the semiconductor. Thus, by applying a voltage between the top-contact and the gate, the electric field will lead to a bending of the energy bands. Since the charge carrier density depends exponentially on the energy difference $E_f - E_v$, the band bending leads to a change of the charge carrier concentration next to the semiconductor-insulator interface. This is named the field-effect [32].

Generally, there are three different regimes as a function of the applied gate voltage (see fig. 2.5). When a negative voltage ($V_g < 0$, fig. 2.5(a)) is applied to the gate, the bands are bent upwards and the valence band (HOMO in organic devices) gets closer to the Fermi level, which results in an accumulation of holes near the interface. This regime is called "accumulation". When a small positive voltage ($V_g > 0$, fig. 2.5(b)) is applied, a band bending in the opposite direction occurs and the density of holes at the interface decreases which leads to the "depletion" of the device. Accumulation and depletion are observable for inorganic and organic semiconductors. In doped inorganic MIS diodes, there is also a third regime for large positive voltages ($V_g \gg 0$, fig. 2.5(c)). Here, the bands are bent even more

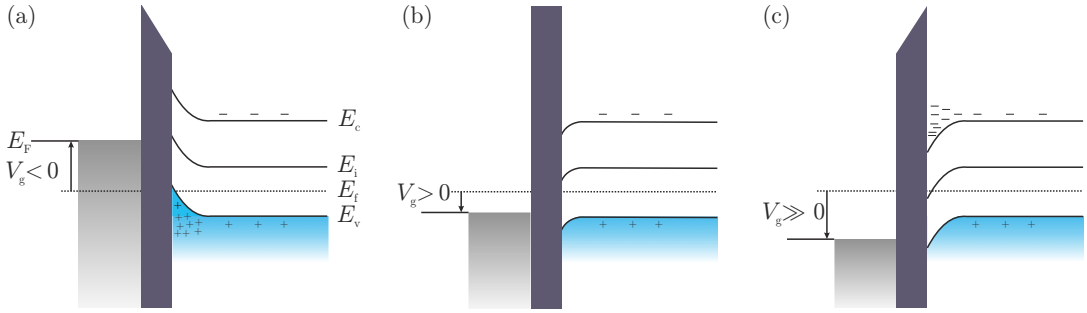


Figure 2.5: Illustration of the gate voltage-induced band bending in MIS structures for a *p*-type semiconductor. (a) Accumulation regime, (b) depletion regime and (c) inversion regime.

downwards until the intrinsic level E_i crosses the Fermi level E_f. The density of electrons at the interface now increases drastically and thus, the type of charge carriers at the interface is inverted. This regime is called "inversion".

However, the inversion regime is not observed in organic MIS diodes because organic semiconductors are usually used undoped and the generation of minority charge carriers is additionally hindered by the large bandgap. Therefore, organic field-effect devices are usually operated in the accumulation regime [33, 34]. Organic semiconductors often exhibit accumulation of holes for negative voltages and accumulation of electrons for positive voltages. That is why the working principles of OFETs will not be explained with the help of metal-oxide-semiconductor field-effect transistors (MOSFETs), which are operated in inversion but with the theory of thin-film transistors (TFTs). The TFT structure is usually used for low conductivity materials like amorphous silicon or organic thin films [6].

2.2.2 Organic field-effect transistors

Thin-film transistors

In the preceding section the field-effect has been introduced with the help of the MIS diode, the most simple device to exhibit field-effect properties. MIS diodes are two-terminal devices. The working principle of TFTs is also based on the field-effect but a TFT features a third terminal. Transistors are the most important devices in modern micro- and nanoelectronics. The systematic layout of a TFT can be seen in fig. 2.6.

The setup is similar to MIS diodes: the conducting gate is separated from the

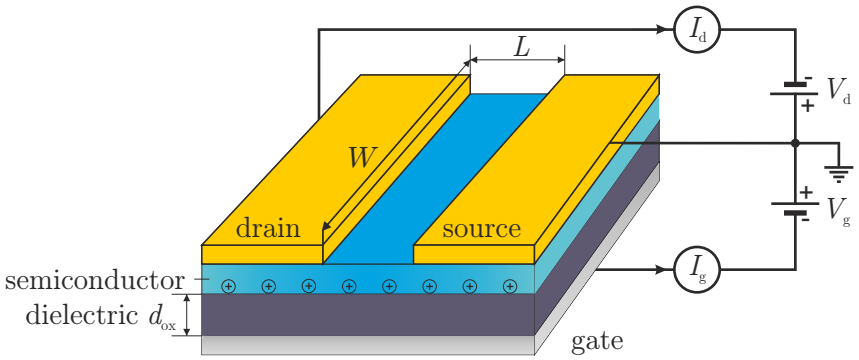


Figure 2.6: Schematic layout of a top-contact thin-film transistor. d_{ox} denotes the insulator thickness, W and L stand for the channel width and length, V_d and V_g for the drain and gate voltage, and I_d and I_g for the drain and gate current, respectively.

semiconductor by an insulator with thickness d_{ox}. In contrast to the MIS diode, there are two top electrodes: source and drain. They are separated by the so-called channel. The distance between source and drain is the channel length L, the width of the contacts is the channel width W. With the help of these three contacts it is possible to apply two voltages and measure two currents independently. The source contact is always connected to the ground. Similar to MIS diodes, the gate voltage V_g, which is applied between source and gate, can cause the accumulation or depletion of charge carriers at the semiconductor-insulator interface. The accumulated charge carriers can form a conducting channel between source and drain. The drain voltage V_d is applied between source and drain and a corresponding drain current I_d can be measured. It is possible to control I_d by V_g. The gate current I_g is the leakage current through the gate oxide and should be as low as possible. In the following a model will be presented that describes the correlations between these current and voltage values.

Charge carrier mobilities

Fig. 2.7 shows a comparison of the charge carrier mobility in silicon and in organic molecular materials for different morphologies. In silicon, it ranges from $10^{-1}\,\mathrm{cm^2/Vs}$ for amorphous films up to $10^{3}\,\mathrm{cm^2/Vs}$ for highly crystalline layers. Whereas organic semiconductors cannot compete with crystalline or polycrystalline silicon, mobilities comparable to those in amorphous silicon have been reported for some polycrystalline organic semiconductors, of which pentacene reveals the highest values up to date ($\mu_{max} = 5.0\,\mathrm{cm^2/Vs}$ for hole transport [35]). OFETs based on ultra-pure organic single-crystals reached mobilities up to $40\,\mathrm{cm^2/Vs}$ for holes,

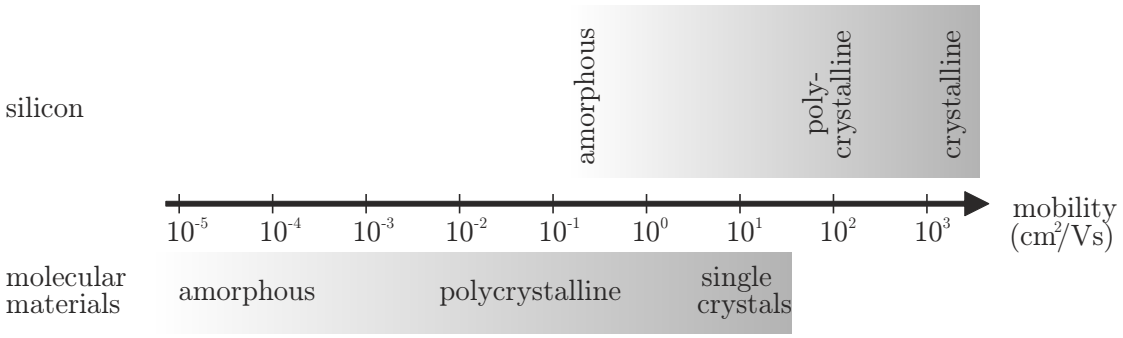


Figure 2.7: Comparison of the charge carrier mobilities in silicon and organic molecular materials [37].

which is already close to polycrystalline silicon [36]. This underlines that OFETs can be considered as adequate alternative for amorphous silicon transistors.

Unipolar description

Schmechel *et al.* developed a model to describe charge carrier transport in ambipolar polycrystalline organic field-effect transistors [38]. It will be introduced for a unipolar transistor assuming hole-only transport and then extended to the ambipolar case. The model is based on the equivalent circuit shown in fig. 2.8. x denotes the distance between source and a given point in the transport channel, L is the total channel length. The channel is represented by a series of resistors R' separated by capacitors C' from the gate. The surface charge per unit area $Q'(x)$ generated by the field-effect can be calculated via

$$Q'(x) = e\,[p(x) - n(x)] = C'\,[V(x) - V_\mathrm{g}]\,, \tag{2.4}$$

where e is the elementary charge, $p(x)$ and $n(x)$ stand for the number of holes and electrons per unit area, respectively. As mentioned above, only hole transport is considered at the moment, resulting in $n(x) = 0$. C' is the capacitance per unit area and $V(x)$ the voltage drop at each position x along the semiconductor-insulator interface. The latter can be written as

$$V(x) = V_\mathrm{d} \cdot \frac{R(x)}{R_\mathrm{tot}}. \tag{2.5}$$

Here, $R(x)$ represents the partial channel resistance between source ($x = 0$) and position x in the channel given by

$$R(x) = \int_0^x \frac{\mathrm{d}x'}{We\mu_\mathrm{h}\,p(x)}, \tag{2.6}$$

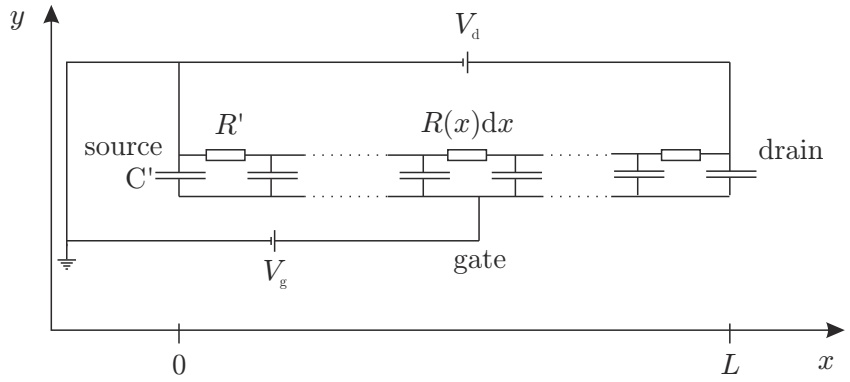


Figure 2.8: Equivalent resistor-capacitor circuit for the modeling of charge carrier transport in TFTs [38].

where $\sigma = e\mu_h\, p(x)$ is the conductivity and μ_h the hole mobility. The total resistance R_{tot} given in eq. 2.5 is defined as

$$R_{tot} = R(L). \tag{2.7}$$

As a next step, eq. 2.5 is substituted in eq. 2.4 and subsequently differentiated. Thus, one obtains the local variation of the charge in the channel:

$$\frac{dQ'(x)}{dx} = \frac{C'V_d}{R_{tot}} \cdot \frac{1}{W\mu_h} \cdot \frac{1}{Q'(x)}. \tag{2.8}$$

This is a differential equation in $Q'(x)$ and can be rewritten as

$$Q'(x)dQ'(x) = \frac{C'V_d}{R_{tot}W\mu_h}dx. \tag{2.9}$$

In order to solve eq. 2.9 one has to distinguish two cases:

Initially, $|V_d| \leq |V_g|$ is considered, representing the case of small drain voltages. One can define two boundary conditions for the charge density:

$$Q'(0) = C'V_g \tag{2.10}$$

and

$$Q'(L) = C'\left(V_g - V_d\right). \tag{2.11}$$

With the help of eq. 2.10, eq. 2.9 can be solved by partial integration. This yields the surface charge at each position x:

$$Q'(x) = \sqrt{C'^2V_g^2 + 2\frac{C'V_d}{R_{tot}W\mu_h} \cdot x}. \tag{2.12}$$

One can obtain an expression for the total resistance substituting eq. 2.11 into eq. 2.12:

$$R_{\mathrm{tot}} = \left| \frac{L}{W \mu_{\mathrm{h}} C' \left(\frac{1}{2} V_{\mathrm{d}} - V_{\mathrm{g}} \right)} \right|. \tag{2.13}$$

The second case is $|V_{\mathrm{d}}| > |V_{\mathrm{g}}|$. In this regime, there is no accumulation of charges at the drain electrode any more because the voltage drop between drain and gate becomes zero or even reversed. Thus, the second boundary condition (eq. 2.11) becomes

$$Q'(L) = 0. \tag{2.14}$$

Now, the total resistance can be written as

$$R_{\mathrm{tot}} = \left| \frac{2 V_{\mathrm{d}} L}{W \mu_{\mathrm{h}} C' V_{\mathrm{g}}^2} \right|. \tag{2.15}$$

It is possible to give an expression for the drain current defined by

$$I_{\mathrm{d}} = \frac{V_{\mathrm{d}}}{R_{\mathrm{tot}}}. \tag{2.16}$$

This yields

$$|I_{\mathrm{d}}| = \begin{cases} \dfrac{W \mu_{\mathrm{h}} C'}{L} \left(V_{\mathrm{g}} - \dfrac{1}{2} V_{\mathrm{d}} \right) V_{\mathrm{d}} & \text{if } |V_{\mathrm{d}}| \leq |V_{\mathrm{g}}|, \\ \dfrac{W \mu_{\mathrm{h}} C'}{2L} V_{\mathrm{g}}^2 & \text{if } |V_{\mathrm{d}}| > |V_{\mathrm{g}}|. \end{cases} \tag{2.17}$$

Eqs. 2.17 represent the case of an ideal unipolar organic field-effect transistor neglecting any trap states. In reality charges accumulated at the interface can be trapped in localized states and cannot contribute to charge carrier transport. Thus, the effective number of charges is reduced by these traps and charge carrier transport only takes place for gate voltages larger than a threshold voltage for hole accumulation $V_{\mathrm{t,h}}$. At $V_{\mathrm{g}} = V_{\mathrm{t,h}}$ all traps are filled and the accumulation of charges in the channel begins [6]. This can be taken into account by defining the effective gate voltage

$$V_{\mathrm{eff}} := V_{\mathrm{g}} - V_{\mathrm{t,h}}. \tag{2.18}$$

Further factors contributing to V_{t} can be built-in dipoles or impurities [10]. Now, the gate voltage V_{g} in eqs. 2.4 - 2.17 can be substituted by V_{eff}. Further on, measurements and analysis of OFETs is usually done in the *linear regime* $|V_{\mathrm{d}}| \ll |V_{\mathrm{g}} - V_{\mathrm{t,h}}|$. This allows for the simplification of eq. 2.17, which can be rewritten as

$$|I_{\mathrm{d}}| = \begin{cases} \dfrac{W \mu_{\mathrm{h}} C'}{L} \left(V_{\mathrm{g}} - V_{\mathrm{t,h}} \right) V_{\mathrm{d}} & \text{if } |V_{\mathrm{d}}| \ll |V_{\mathrm{g}} - V_{\mathrm{t,h}}|, \\ \dfrac{W \mu_{\mathrm{h}} C'}{2L} \left(V_{\mathrm{g}} - V_{\mathrm{t,h}} \right)^2 & \text{if } |V_{\mathrm{d}}| \geq |V_{\mathrm{g}} - V_{\mathrm{t,h}}|. \end{cases} \tag{2.19}$$

In the first regime $|V_\mathrm{d}| \ll |V_\mathrm{g} - V_\mathrm{t,h}|$ the drain current depends linearly on the drain voltage, that is why it is called linear regime. In the second regime the drain current is independent of the drain voltage, this is the *saturation regime*.

Characteristic parameters of OFETs

There are two different ways to characterize an OFET: output and transfer characteristics. For the output characteristics, V_g is kept constant and I_d is measured as a function of V_d. Fig. 2.9(a) depicts simulated output characteristics of an ideal TFT, i.e. threshold voltage is neglected, in the hole transport regime for four different gate voltages. The discrimination between linear and saturation regime can clearly be seen with the help of the dashed line which shows the relation $V_\mathrm{d} = V_\mathrm{g}$. Fig. 2.9(b) depicts simulated transfer characteristics of the same transistor for three different drain voltages in the linear regime ($V_\mathrm{d} = -2, -5, -10\,\mathrm{V}$) and for one drain voltage in the saturation regime ($V_\mathrm{d} = -80\,\mathrm{V}$). The transfer curves are usually shown on a logarithmic scale to determine the switch-on voltage V_so, the on/off ratio $I_\mathrm{on}/I_\mathrm{off}$ and the sub-threshold swing of the transistor. These parameters are important to characterize the performance of OFETs and will be discussed briefly in the following.

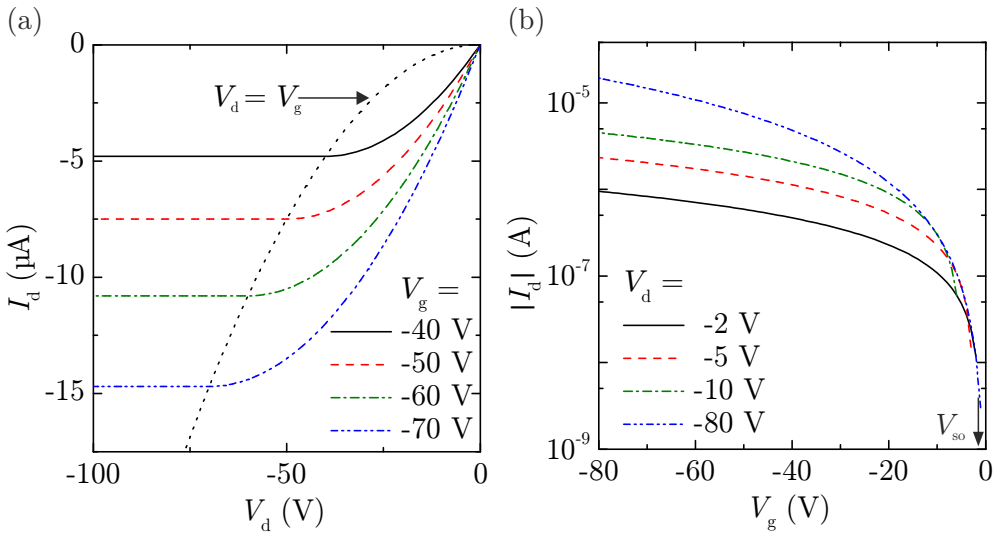


Figure 2.9: Simulation of characteristic curves of an ideal TFT in the hole transport regime. Used parameters: $C' = 1.0 \times 10^{-4}\,\mathrm{F/m^2}$, $W = 3.0\,\mathrm{mm}$, $L = 50\,\mu\mathrm{m}$, $\mu_\mathrm{h} = 1.0 \times 10^{-2}\,\mathrm{cm^2/Vs}$. (a) Output characteristics and (b) transfer characteristics of the same device. The short-dotted line in (a) depicts the relation $V_\mathrm{d} = V_\mathrm{g}$ and separates the linear from the saturation regime. V_so is the switch-on voltage of the transistor.

The switch-on voltage V_{so} is defined as the voltage at which there is no band bending in the semiconductor [39]. For gate voltages $|V_g| < |V_{so}|$, the transistor is in the off-state and the off-current I_{off} is measured. At $V_g = V_{so}$, the drain current abruptly increases above a defined low off-current level. Hence, V_{so} can easily be determined from transfer characteristics on a logarithmic scale. For an ideal transistor, there is no difference between the threshold voltage V_t and V_{so}. However, trap states can cause non-linearities in the transfer characteristics at low gate voltages resulting in a deviation of V_{so} and V_t. This effect is further discussed with the help of simulations in sec. 10.2. In inorganic FETs, V_t is the onset of the strong inversion regime, whereas in organic FETs, it is only a fit parameter of the transfer characteristics [40]. That is why V_{so}, which is directly observable, is sometimes used for characterization. The on/off ratio I_{on}/I_{off} is defined as the ratio between the drain current in the on-state and the off-current. It is a measure for the ability of the transistor to switch off. In real devices, the off-current should be as low as possible, thus, I_{on}/I_{off} should be as high as possible. For OFETs with pentacene, on/off ratios as high as 10^8 have been reached [41]. This is already higher than for amorphous silicon thin-film transistors with 10^6 but still below crystalline silicon MOSFETs with on/off ratios up to 10^9 [6]. The on/off ratio cannot be determined in case of an ideal transistor since the off-current vanishes in that case. The sub-threshold swing S is defined as

$$S = \frac{\mathrm{d}V_g}{\mathrm{d}(\log I_d)} \tag{2.20}$$

and gives information about how much voltage is needed to increase the drain current by one order of magnitude directly above the onset of I_d. S is required to be as low as possible, since low operation voltages are desired. However, there is an intrinsic limit of S for conventional inorganic MOSFETs, which is $S_{min} = k_B T/e \cdot \ln 10 = 60\,\mathrm{mV/dec}$ at room temperature [32, 42]. This limit is related to a natural width of the energetic distribution of the density of states. In high-quality single-crystal FETs with pentacene as active material, values of $S = 300\,\mathrm{mV/dec}$ have been reported [26]. In our case values of $S \approx 1.2\,\mathrm{V/dec}$ have been determined, as will be shown in the experimental part of this thesis. However, in polycrystalline OFETs, S is usually larger.

Ambipolar description

In an ambipolar transistor, both electrons and holes are accumulated at the interface depending on the applied gate voltage. Ambipolar OFETs are interesting for potential applications and scientific reasons [10]. Device architectures that can provide p- and n-channel performance can be used for the fabrication of complemen-

tary inverters without advanced patterning techniques. Additionally, the presence of electrons and holes in the channel can lead to recombination of the charge carriers at a certain point. If the conditions are favorable, the recombination can even stimulate the emission of light, which is used for the realization of light-emitting transistors [11, 12]. From a scientific point of view it is desirable to investigate electron and hole transport by direct comparison in one single device to improve the understanding of charge carrier transport in organic semiconductors.

For $(V_\mathrm{g} - V_\mathrm{t,h}) < 0$ and $|V_\mathrm{d}| \ll |V_\mathrm{g} - V_\mathrm{t,h}|$ the transistor operates in the hole-only regime (p-type), whereas for $(V_\mathrm{g} - V_\mathrm{t,e}) > 0$ and $|V_\mathrm{d}| \ll |V_\mathrm{g} - V_\mathrm{t,e}|$ the transistor operates in the electron-only regime (n-type) with $V_\mathrm{t,h}$ and $V_\mathrm{t,e}$ being the threshold voltages for hole and electron transport, respectively. The ambipolar regime occurs for $|V_\mathrm{d}| \geq |V_\mathrm{g} - V_\mathrm{t,h}|$ or $|V_\mathrm{d}| \geq |V_\mathrm{g} - V_\mathrm{t,e}|$ because the voltage drop between drain and gate is reversed and thus allows for the injection of the opposite charge carrier type. To enable the description of transistor characteristics of ambipolar TFTs the previously discussed model is extended by the additional presence of electrons inside the channel [38]. This is done by adding electrons to the surface charge per unit area. Thus, eq. 2.4 is applied with $n \neq 0$ and an electron mobility μ_e is introduced. For simplicity, the threshold voltages are assumed to be equal: $|V_\mathrm{t,h}| = |V_\mathrm{t,e}| = V_\mathrm{t}$. Deviations from this assumption will be discussed later.

Since only one charge carrier type is present in the linear regime, the derived expressions for hole transport remain unchanged. Significant differences occur in the ambipolar regime when $|V_\mathrm{d}| \geq |V_\mathrm{g} - V_\mathrm{t}|$. Assuming a high recombination rate, the channel can be separated into a hole- and an electron-transport part with the recombination taking place at the intersection point x_0. The total channel resistance can now be considered as a series of the resistances of the hole transport section R_h and the electron transport section R_e [38] with

$$R_\mathrm{h} = \frac{2x_0}{W\mu_\mathrm{h}C'|V_\mathrm{g} - V_\mathrm{t}|} \quad \text{and} \quad R_\mathrm{e} = \frac{2(L - x_0)}{W\mu_\mathrm{e}C'|V_\mathrm{g} - V_\mathrm{t} - V_\mathrm{d}|} \ . \tag{2.21}$$

Since the current in both sections is equal, a relation between R_h and R_e can be obtained:

$$\frac{|V_\mathrm{g}|}{R_\mathrm{h}} = \frac{|V_\mathrm{g} - V_\mathrm{d}|}{R_\mathrm{e}}. \tag{2.22}$$

A combination of eqs. 2.21 and 2.22 leads to an expression for the intersection point:

$$x_0 = \frac{L(V_\mathrm{g} - V_\mathrm{t})^2}{(V_\mathrm{g} - V_\mathrm{t})^2 + \frac{\mu_\mathrm{e}}{\mu_\mathrm{h}}\left(V_\mathrm{g} - V_\mathrm{t} - V_\mathrm{d}\right)^2} \ . \tag{2.23}$$

One obtains the ambipolar transistor characteristics for hole accumulation mode

($V_\mathrm{g} < 0$ and $|V_\mathrm{g}| > |V_\mathrm{t}|$) in analogy to the unipolar case (see eqs. 2.19):

$$|I_\mathrm{d}| = \begin{cases} \dfrac{W \mu_\mathrm{h} C'}{L} \left(V_\mathrm{g} - V_\mathrm{t}\right) V_\mathrm{d} & \text{if } |V_\mathrm{d}| \ll |V_\mathrm{g} - V_\mathrm{t}|, \\ \dfrac{WC'}{2L} \left[\mu_\mathrm{h} \left(V_\mathrm{g} - V_\mathrm{t}\right)^2 + \mu_\mathrm{e} \left(V_\mathrm{g} - V_\mathrm{t} - V_\mathrm{d}\right)^2\right] & \text{if } |V_\mathrm{d}| \geq |V_\mathrm{g} - V_\mathrm{t}|. \end{cases} \tag{2.24}$$

Output characteristics based on this model are shown in fig. 2.10 for the hole accumulation regime. In fig. 2.10(a) simulated curves without consideration of the threshold voltage are shown. In accordance to eq. 2.24 the linear regime remains unchanged but instead of a saturation for higher drain voltages, a further increase of the drain current occurs due to the injection of electrons from the drain electrode, which is referred to as *ambipolar increase*.

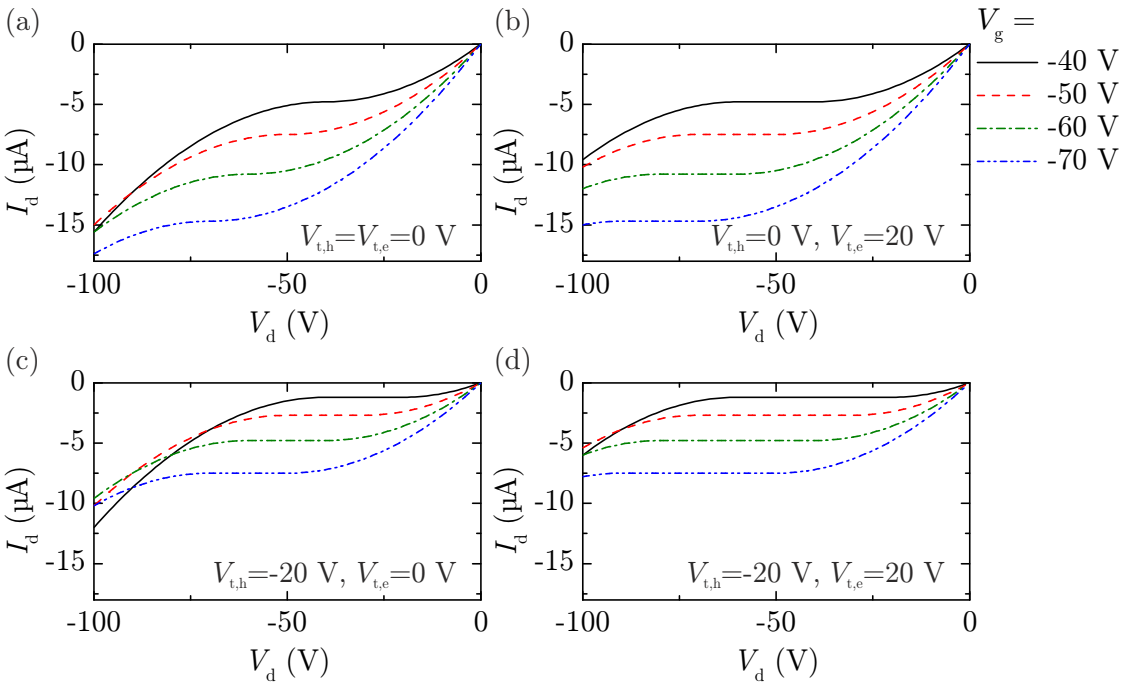


Figure 2.10: Dependence of output characteristics of an ambipolar TFT on the individual threshold voltages for different negative gate voltages. The following parameters have been used for the simulation: $C' = 1.0 \times 10^{-4}\,\mathrm{F/m^2}$, $W = 3.0\,\mathrm{mm}$, $L = 50\,\mu\mathrm{m}$, $\mu_\mathrm{h} = \mu_\mathrm{e} = 1.0 \times 10^{-2}\,\mathrm{cm^2/Vs}$.

Deviations from ideal characteristics

Up to here, all transistor data shown was for the ideal case with equal charge carrier mobilities and without threshold voltage. Now, the effects of a non-vanishing threshold voltage and asymmetric charge carrier mobilities will be discussed. In general, without the simplifying assumptions $|V_{\mathrm{t,h}}| = |V_{\mathrm{t,e}}|$ and $|V_{\mathrm{d}}| \ll |V_{\mathrm{g}} - V_{\mathrm{t}}|$, eq. 2.24 can be written as [38]

$$|I_{\mathrm{d,h}}| = \begin{cases} \dfrac{W\mu_{\mathrm{h}}C'}{L}\left(V_{\mathrm{g}} - V_{\mathrm{t,h}} - \dfrac{1}{2}V_{\mathrm{d}}\right)V_{\mathrm{d}} & \text{if } |V_{\mathrm{d}}| \le |V_{\mathrm{g}} - V_{\mathrm{t,h}}|, \\ \dfrac{WC'}{2L}\left[\mu_{\mathrm{h}}\left(V_{\mathrm{g}} - V_{\mathrm{t,h}}\right)^2 + \mu_{\mathrm{e}}\left(V_{\mathrm{g}} - V_{\mathrm{t,e}} - V_{\mathrm{d}}\right)^2\right] & \text{if } |V_{\mathrm{d}}| > |V_{\mathrm{g}} - V_{\mathrm{t,h}}| \end{cases} \tag{2.25a}$$

and

$$|I_{\mathrm{d,e}}| = \begin{cases} \dfrac{W\mu_{\mathrm{e}}C'}{L}\left(V_{\mathrm{g}} - V_{\mathrm{t,e}} - \dfrac{1}{2}V_{\mathrm{d}}\right)V_{\mathrm{d}} & \text{if } |V_{\mathrm{d}}| \le |V_{\mathrm{g}} - V_{\mathrm{t,e}}|, \\ \dfrac{WC'}{2L}\left[\mu_{\mathrm{e}}\left(V_{\mathrm{g}} - V_{\mathrm{t,e}}\right)^2 + \mu_{\mathrm{h}}\left(V_{\mathrm{d}} - V_{\mathrm{g}} + V_{\mathrm{t,h}}\right)^2\right] & \text{if } |V_{\mathrm{d}}| > |V_{\mathrm{g}} - V_{\mathrm{t,e}}| \end{cases} \tag{2.25b}$$

for hole and electron transport regime, respectively.

Fig. 2.10(b) shows output characteristics of the same device as in (a) but with $V_{\mathrm{t,e}} = 20\,\mathrm{V}$ and $V_{\mathrm{t,h}} = 0\,\mathrm{V}$. It can clearly be seen that both the linear and the saturation regimes remain unchanged because they are determined by hole transport but the increase of the drain current for large $|V_{\mathrm{d}}|$ is shifted towards more negative drain voltages as more voltage is needed for the injection of electrons due to the higher value of $V_{\mathrm{t,e}}$. Fig. 2.10(c) illustrates the effect of a finite threshold voltage for hole injection $V_{\mathrm{t,h}} = -20\,\mathrm{V}$ and $V_{\mathrm{t,e}} = 0\,\mathrm{V}$. Here, the current in the linear and saturation regimes is reduced but the onset of the ambipolar increase of I_{d} is not affected. Consequently, a superposition of both effects occurs when electron and hole threshold voltage are finite as shown in fig. 2.10(d) for $V_{\mathrm{t,h}} = -20\,\mathrm{V}$ and $V_{\mathrm{t,e}} = 20\,\mathrm{V}$.

In almost all real ambipolar devices the mobilities of electrons and holes are not equal. There can be an asymmetry of several orders of magnitude, which has a large effect on the transistor characteristics. Fig. 2.11 gives an overview of the effects of an asymmetry between electron and hole mobility. For comparison, fig. 2.11(a) shows again the data of the device already discussed in fig. 2.10(a) with $\mu_{\mathrm{h}} = \mu_{\mathrm{e}} = 10^{-2}\,\mathrm{cm^2/Vs}$. In fig. 2.11(b) one can see the output characteristics of a device with reduced electron mobility ($\mu_{\mathrm{h}} = 2\mu_{\mathrm{e}} = 10^{-2}\,\mathrm{cm^2/Vs}$). The hole-dominated linear and saturation regimes remain unchanged, but the slope of the ambipolar increase due to electron injection is reduced by the lower mobility.

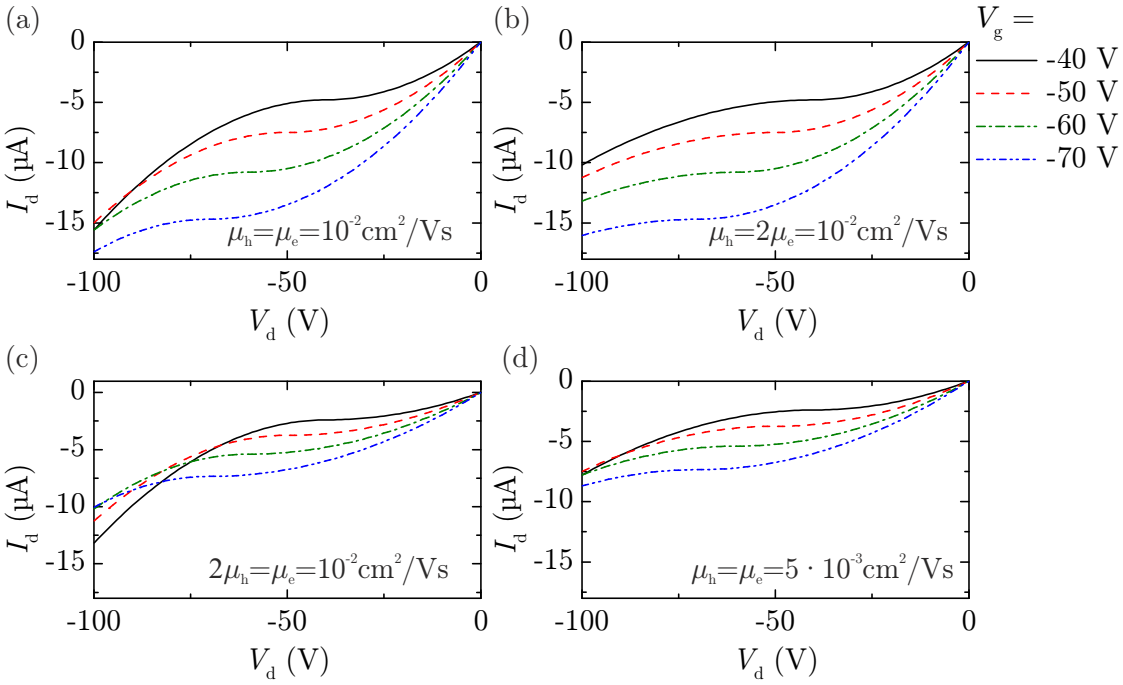


Figure 2.11: Comparison of output characteristics of the transistor used in fig. 2.10 for different mobility values.

On the other hand, for reduced hole mobility ($2\mu_h = \mu_e = 10^{-2}\,\mathrm{cm^2/Vs}$), shown in fig. 2.11(c), the slope of the linear regime is reduced and therewith also the saturation current whereas the electron transport is not affected. Finally, fig. 2.11(d) illustrates the case when electron and hole mobilities are reduced simultaneously ($\mu_h = \mu_e = 5 \times 10^{-3}\,\mathrm{cm^2/Vs}$). The resulting output curves have the same shape as in (a), but the corresponding currents are divided by a factor of two.

In general, there are various factors that contribute to non-ideal ambipolar transistor characteristics. Different threshold voltages for electron and hole transport or asymmetric charge carrier mobilities are just two examples, others might be contact resistances or impurities. The similarity of figs. 2.10 and 2.11 demonstrates that it is not possible to determine the exact reason for deviations from ideal characteristics only by measuring output curves. It is necessary to obtain more detailed information by measuring transfer curves and applying other techniques like the transfer-length method shown in the next chapter.

Overview of the transport regimes

Fig. 2.12 gives an overview of all possible transport regimes that can be found in an ambipolar OFET [43]. Regimes 1 and 4 correspond to unipolar electron or hole

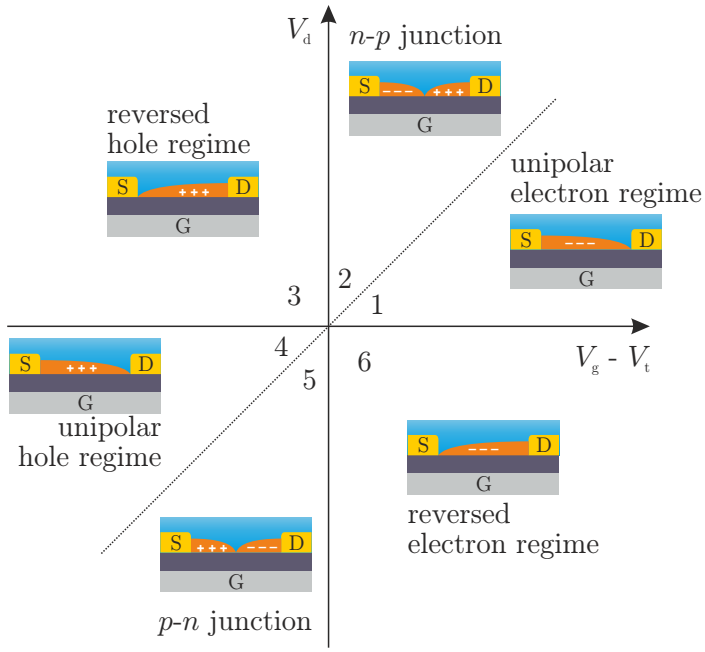


Figure 2.12: Overview of all possible transport regimes in an ambipolar OFET.

transport. When $|V_g - V_t| > |V_d|$ and both are positive the transistor operates in the electron-only regime 1, whereas when $|V_g - V_t| > |V_d|$ but both are negative, hole-only operation occurs (regime 4). Determination of transistor characteristics is usually done in these regimes, so that the device can be treated like a unipolar one.

Ambipolar operation takes place in regimes 2 and 5. When $V_d > V_g - V_t > 0$ is fulfilled (regime 2), the transistor operates in the electron accumulation but a n-p junction is formed with holes injected from the drain electrode. When $V_d < V_g - V_t < 0$ is valid, the situation is vice versa (regime 5) and a p-n junction is formed.

The other two regimes 3 and 6 are related to reversed unipolar operation where charge carriers are injected from the drain electrode: reversed hole-only operation (regime 3) occurs for $V_g - V_t < 0$, $V_d > 0$ and reversed electron-only operation (regime 6) occurs for $V_g - V_t > 0$, $V_d < 0$. Here, source and drain are exchanged, which has no effect in the case of symmetric electrodes but causes deviations in the transistor characteristics for asymmetric electrodes.

2.3 Density functional theory calculations of molecular orbitals in CuPc

Introduction

Density functional theory (DFT) is a method to calculate the electronic properties of quantum mechanical many-electron systems in the ground state. It is widely used in physics and chemistry. In 1998 the Nobel price was awarded to Walter Kohn for the development of DFT [44]. The method is based on the Born-Oppenheimer approximation, a technique to solve the Schrödinger equation that assumes the movement of all nuclei in a given system to be "frozen". Following the approach by Hohenberg and Kohn which supposes that the ground state energy of a system depends only on the electronic density, the ground state electronic density can be obtained by a variational principle [45]. Hence, all properties depending on the density can be calculated. The idea by Kohn and Sham was to use non-interacting particles to build a test wave function for the variational treatment [44]. This results in a set of nonlinear single-particle equations for three spatial coordinates, the so-called Kohn-Scham equations. They are solved iteratively in a self-consistent way. In contrast to other theoretical approaches it is not necessary to solve a many-particle Schrödinger equation for N electrons and $3N$ spatial coordinates but only a set of nonlinear single-particle equations. This simplification reduces the calculation time drastically, since the latter scales with 2^N for many-particle equations but only with N^3 in the case of DFT. In recent years, new methods have been presented that even provide a linear scaling [46].

In the early days of DFT, calculations were done with the so-called *local density approximation* (LDA), where all exchange correlations between the individual particles are approximated by those in an homogeneous electron gas. LDA usually underestimates bond lengths and overestimates binding energies. Taking into account also variations in the density, the *generalized gradient approximation* (GGA) improves the accuracy of the calculations [47].

With the help of DFT calculations on organic molecules it is possible to improve the understanding of charge carrier injection and transport properties in these materials. Here, DFT results are shown for the HOMO and LUMO levels of CuPc, the injection of charges from metal contacts into CuPc and for charge carrier transport from one CuPc molecule to the next. All calculations were done by Dr. Cosima Schuster from the chair "Theoretical Solid State Physics" of Prof. Dr. Ulrich Eckern in Augsburg. While details of the DFT calculations are beyond the scope of this thesis, the results are a helpful complement to the charge carrier transport measure-

ments shown later in this thesis. The predictions made by DFT can be compared directly to the experimental data and, as will be seen, explain some of the observed effects.

DFT results for CuPc

As a first step, the spatial extensions of the HOMO and the LUMO of a CuPc molecule, i.e. the charge density isosurfaces, are determined. The calculations were done for an isolated molecule and a CuPc monolayer with different orientations. It turned out that the charge density isosurfaces are nearly identical for all these cases. Thus, it can be concluded that the electronic structure of CuPc near the Fermi level is hardly modified by inter-molecular interactions [48]. The charge density isosurfaces are obtained by integration of the DOS calculated by DFT. They are depicted in fig. 2.13. The two images shown in (a) represent the HOMO, which has contributions from two different molecular orbitals. The LUMO is displayed in (b). The most important difference is the missing contribution from nitrogen in case of the HOMO. The spatial extensions are almost equal, thus, no conclusion about the overlap of different molecules can be drawn.

As will be discussed in more detail in the experimental section, the work function of a metal contact is a key parameter for the injection of holes into the HOMO or electrons into the LUMO. Therefore, DFT calculations of a CuPc molecule with metal contacts, which differ considerably with respect to their work function ϕ, were performed. Here, calcium and gold were used: $\phi_{\mathrm{Ca}} \approx 2.9\,\mathrm{eV}$ and $\phi_{\mathrm{Au}} \approx 5.1\,\mathrm{eV}$ [49]. The metal atoms are attached to the CuPc molecule in two different geometries shown in fig. 2.14(a): in the planar geometry the metal chain is connected to the outer phenyl ring, whereas in the perpendicular geometry the metal contacts the Cu atom directly. The charge density isosurfaces around the CuPc Fermi

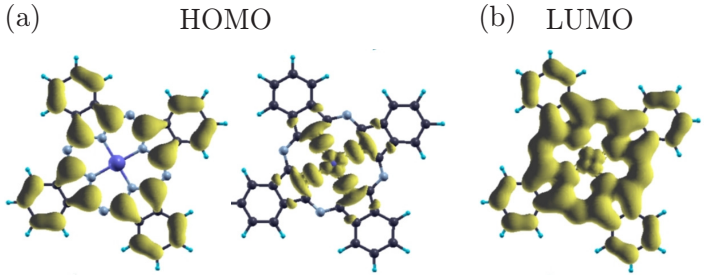


Figure 2.13: Illustrations of calculated charge density isosurfaces of CuPc. The two contributing molecular orbitals of the HOMO are shown in (a), the LUMO in (b) [48].

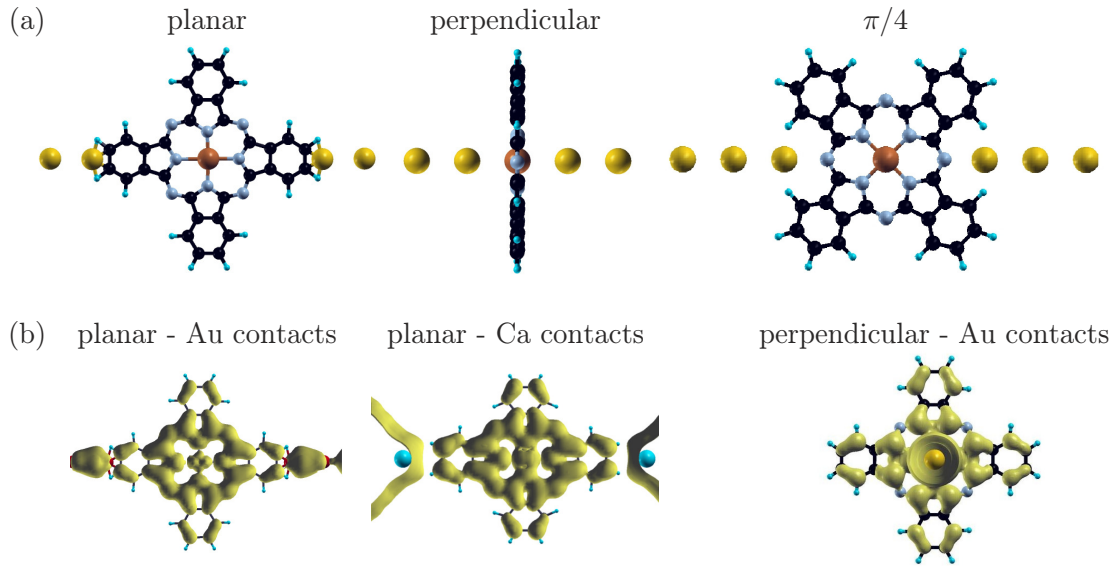


Figure 2.14: (a) Different contact geometries used for the DFT calculations: planar, perpendicular and $\pi/4$ geometry. (b) Charge density isosurfaces for CuPc with Au and Ca contacts [48].

level for a molecule contacted in the planar geometry with Au and Ca are shown in fig. 2.14(b), left hand side and center. They are comparable and the shape resembles the LUMO in fig. 2.13(b). This is a clear sign for electron transfer to the molecule. The injection properties are completely different in the perpendicular geometry. Here, the charge density isosurfaces near the Fermi level for Au contacts resembles the HOMO of the isolated molecule as depicted in fig. 2.14(b), right hand side. This indicates that holes can be injected. Ca was found to exhibit no overlap with the Cu atom. Therefore, no hole injection from Ca to CuPc is expected in the perpendicular geometry.

The results obtained for charge carrier injection can be summarized stating that Au contacts can inject electrons and holes, depending on the geometry, whereas Ca can only inject electrons in the planar geometry.

As a next step, the transmission of charge carriers through a Au/CuPc/Au model system is investigated. This is done for a single CuPc molecule contacted by Au chains in three different geometries. First, the planar and perpendicular configurations from fig. 2.14(a) are compared. It turns out that the perpendicular geometry exhibits a conductance that is more than one order of magnitude higher compared to the planar configuration, as can be seen in fig. 2.15. Here, the calculated current-voltage characteristics of a Au/CuPc/Au system for both contacts are shown. The difference between both configurations is due to an overlap of the Au and Cu or-

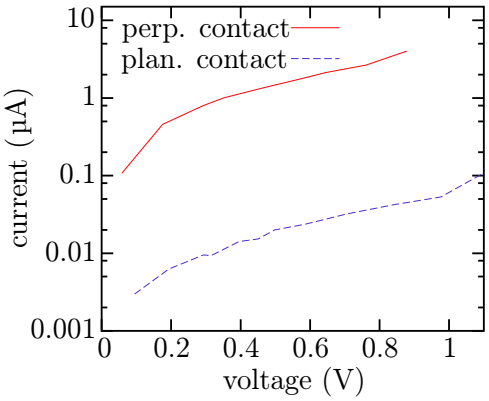


Figure 2.15: Calculated current-voltage characteristics of a Au/CuPc/Au model system for the perpendicular and planar geometries shown in fig. 2.14(a) [48].

bitals in the perpendicular configuration forming a transport path.

Moreover, a different planar configuration is introduced, displayed in fig. 2.14(a), right hand side. Here, the CuPc molecule is rotated by 45° and the gold chains are placed next to the N atoms between two benzene rings. This configuration should simulate the arrangement in a crystal and is referred to as "$\pi/4$-configuration" [48]. In comparison to the standard planar arrangement, this geometry features a considerably lower conductance although an overlap of Au and Cu orbitals is possible. The reduction is caused by the shift of one of the Cu orbitals below the Fermi level.

Finally, the intermolecular transport is studied for all three geometries. Therefore, two CuPc molecules are placed next to each other and each one is contacted by a Au chain on one side. Compared to the single-molecule results, the conductance of both planar contacts (standard and $\pi/4$) is reduced by a factor of 10^{-5} when a second molecule is added, whereas the conductance for the perpendicular case is only reduced by 10^{-2}. Hence, one can expect the planar conduction to be at least by a factor of $10^{-5}/10^{-2} = 10^{-3}$ lower than for the perpendicular case. These results, which will later be compared to experimental data for OFETs and MIS diodes, already demonstrate that differences in contact materials and molecular orientations can have a major influence on transport characteristics.

Chapter 3

Data analysis

3.1 Determination of mobility and contact resistance in OFET devices

In the preceding chapter, the working principles of OFETs have been introduced. The following section will demonstrate how data analysis of OFETs is done and how one obtains the key parameters like mobility, threshold voltage, contact resistance etc. out of the measured transistor curves. Output characteristics are useful to get a qualitative overview of a device and to determine the individual transport regimes explained in fig. 2.12. However, for a detailed quantitative analysis, transfer characteristics are more powerful: they provide information about charge carrier mobility, threshold voltage, switch-on voltage and on/off ratio. Three different analysis techniques will be presented in the following.

3.1.1 Data evaluation in the linear regime

Fig. 3.1(a) shows a typical transfer curve (straight line) in the linear unipolar hole transport regime ($|V_\mathrm{g} - V_\mathrm{t}| \gg |V_\mathrm{d}|$). According to eq. 2.19, the ideal curve can be described by

$$I_\mathrm{d} = \begin{cases} \dfrac{WC'\mu}{L}\,(V_\mathrm{g} - V_\mathrm{t})\,V_\mathrm{d} & \text{if } V_\mathrm{g} < V_\mathrm{t}, \\ \\ 0 & \text{else.} \end{cases} \tag{3.1}$$

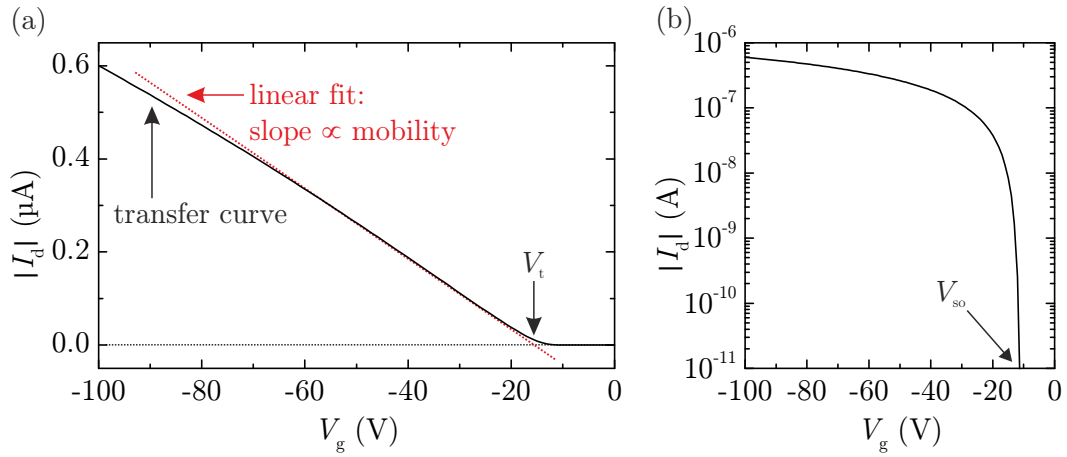


Figure 3.1: Transfer curve in the linear hole transport regime of a typical OFET (straight line). (a) Linear scale, mobility and threshold voltage are determined by the slope and the x-axis intercept of the linear fit (dotted line), respectively. The fit yields $V_t = -15.3\,\mathrm{V}$. (b) Logarithmic scale to determine the switch-on voltage $V_{so} = -11.3\,\mathrm{V}$ and the sub-threshold swing $S = 0.48\,\mathrm{V/dec}$.

W, C' and L are given by the geometry of the transistor, whereas μ and V_t have to be determined by the measurement. Comparing the measured transfer curve with the theoretical equation, several deviations become observable. The onset of the current does not occur sharply at the threshold voltage but there is a significant curvature of the line at low drain currents. It will be shown in chapter 10 that trap states can be responsible for this curvature. In order to be able to give a precise value for the threshold voltage one can perform a linear fit of the current (dotted line). V_t is defined as the intersection of the linear fit with the x-axis. The switch-on voltage V_{so} and the sub-threshold swing S can be determined from a logarithmic plot as shown in fig. 3.1(b) and described in sec. 2.2.2. One obtains $V_{so} = -11.3\,\mathrm{V}$ and $S = 0.48\,\mathrm{V/dec}$ for this example. When applying the linear fit, another deviation from the ideal curve becomes obvious: the drain current does not follow the linear equation but bends downwards for large negative values of V_g. This is a well-known feature of OFETs and can be attributed to a high contact resistance between the electrodes and the organic semiconductor [50]. The formation of a Schottky contact between metal and organic semiconductor is usually considered to be responsible for this contact resistance.

In the linear regime, the slope of the linear fit is directly proportional to the charge carrier mobility. Thus, μ can be calculated with the help of eq. 3.1:

$$\mu = \frac{g_m L}{W C' V_d} \tag{3.2}$$

with $g_\mathrm{m} = \frac{\mathrm{d}I_\mathrm{d}}{\mathrm{d}V_\mathrm{g}}$ being the slope of the linear fit.

3.1.2 Transmission line method

The nonlinearity in the transfer curve shown in fig. 3.1 demonstrates the necessity to consider contact resistance in the data analysis. The effect of contact resistance becomes especially pronounced in the linear regime where TFTs are operated in applications such as active matrix displays. Consequently, one has to deal with Schottky contacts at source and drain, which can be responsible for large injection barriers leading to non-vanishing contact resistances. A pronounced contact resistance and the related nonlinearity in the transfer curves can cause significant errors when the charge carrier mobility is evaluated using eq. 3.2. The *transmission line method* (TLM), sometimes also referred to as *transfer-length method*, is a technique to determine mobilities including the effects of contact resistance.

The idea of the TLM is to split the total measured resistance R_tot of the device into two parts: the channel resistance R_ch and the contact resistance R_c. The channel resistance is given by eq. 3.1:

$$R_\mathrm{ch} = \frac{V_\mathrm{d}}{I_{\mathrm{d,without\,R_c}}} = \frac{1}{WC'\mu(V_\mathrm{g} - V_\mathrm{t})} \cdot L, \tag{3.3}$$

whereas the contact resistance is the sum of the drain and source injection resistances $R_\mathrm{i,source}$ and $R_\mathrm{i,drain}$ and the bulk resistances R_bulk from the top electrodes to the channel [51–53]:

$$R_\mathrm{c} = R_\mathrm{i,source} + R_\mathrm{i,drain} + R_\mathrm{bulk}. \tag{3.4}$$

Fig. 3.2(a) shows a schematic sketch of the resistances inside the OFET. A TLM analysis requires a series of transistors on one substrate which differ only with respect to their channel length. It is useful to cover a wide range of channel lengths to obtain reliable results. For each of these channel lengths a transfer curve is measured using V_d in the linear regime. This is displayed in fig. 3.2 (b) for four different channel lengths between 50 µm and 110 µm. The total resistance of the device is given by

$$R_\mathrm{tot} = \frac{V_\mathrm{d}}{I_{\mathrm{d,with\,R_c}}} = R_\mathrm{ch} + R_\mathrm{c} = \frac{1}{WC'\mu(V_\mathrm{g} - V_\mathrm{t})} \cdot L + R_\mathrm{c}. \tag{3.5}$$

R_ch does not depend on the contacts and is proportional to the channel length L.

In order to obtain R_tot as a function of L one extracts I_d for fixed values of the effective gate voltage $V_\mathrm{eff} = V_\mathrm{g} - V_\mathrm{t}$ as shown in fig. 3.2(b). Then, the total resistance

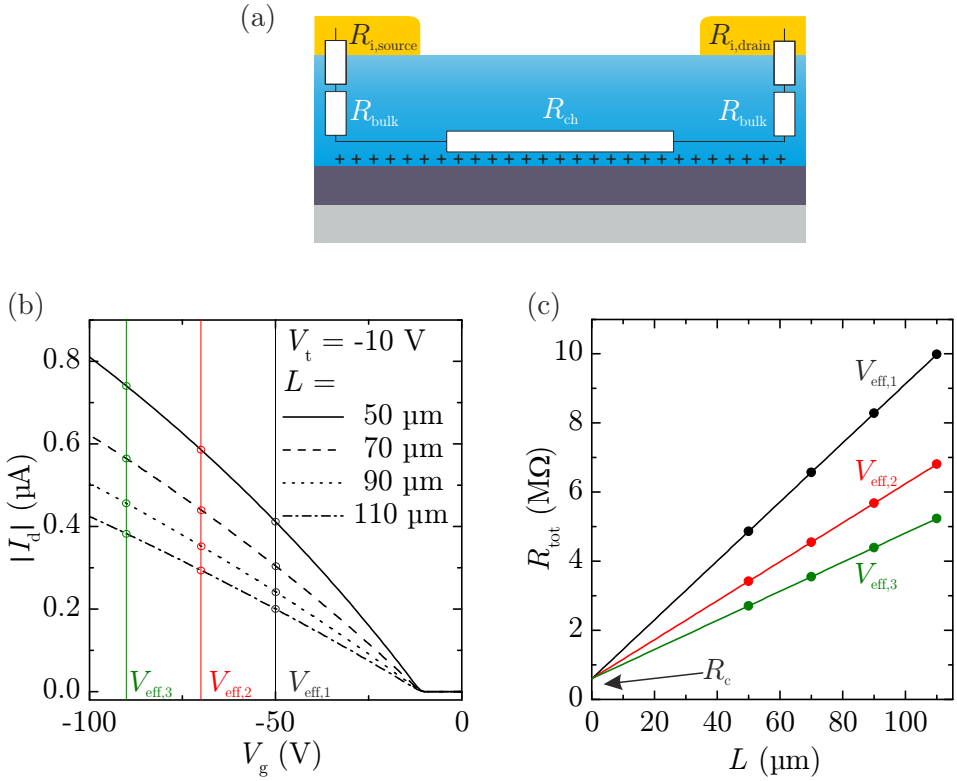


Figure 3.2: Demonstration of the TLM method to determine gate voltage-dependent charge carrier mobility and contact resistance. (a) Resistor model used for the analysis, (b) simulated transfer curves for four different channel lengths and (c) total resistance as a function of channel length for three different effective voltages.

is calculated for each value using $R_{\mathrm{tot}} = V_{\mathrm{d}}/I_{\mathrm{d}}$ and plotted as a function of L for each value of V_{eff}. This procedure is exemplarily done in fig. 3.2(c).

Following eq. 3.5, R_{tot} can be considered as a linear function of L with a slope of

$$m = \frac{1}{WC'\mu(V_{\mathrm{g}} - V_{\mathrm{t}})} \tag{3.6}$$

and a y-axis intercept of R_{c}. By linear fitting of the plotted data of R_{tot}, one obtains R_{c} directly from the y-axis intercept and the charge carrier mobility from the slope of the fitting line:

$$\mu = \frac{1}{WC'(V_{\mathrm{g}} - V_{\mathrm{t}})} \cdot \frac{1}{m}. \tag{3.7}$$

In real devices, μ and R_{c} can be gate voltage-dependent, which is not the case in this model example.

3.1.3 Single-curve analysis

The TLM requires measurements of transfer curves for a series of different channel lengths. The results obtained for the contact resistance are particularly sensitive to small errors in the linear fit. Problems can occur if there are not enough different channel lengths available or if the used channel lengths are too large (i.e. the data points are too far from the y-axis). Such problems can result in a negative determined value of R_c. Therefore, another method is demonstrated that allows for the determination of a gate voltage-dependent contact resistance and charge carrier mobility out of a single curve in the linear unipolar regime. This method has been developed by Horowitz *et al.* [54].

The additional voltage drop that occurs due to the contact resistance reduces the drain current given in eq. 3.1 as follows

$$I_\mathrm{d} = \frac{WC'\mu}{L}(V_\mathrm{g} - V_\mathrm{t})(V_\mathrm{d} - R_\mathrm{c}I_\mathrm{d}). \tag{3.8}$$

Solving this equation for I_d yields

$$I_\mathrm{d} = \frac{\frac{WC'\mu}{L}(V_\mathrm{g} - V_\mathrm{t})V_\mathrm{d}}{1 + \frac{WC'\mu}{L}R_\mathrm{c}(V_\mathrm{g} - V_\mathrm{t})} \ . \tag{3.9}$$

As a next step, the drain conductance or channel conductance g_d and transconductance g_m are calculated, which are defined as follows

$$g_\mathrm{d} = \left(\frac{\partial I_\mathrm{d}}{\partial V_\mathrm{d}}\right)_{V_\mathrm{g}=\mathrm{const.}} = \frac{\frac{WC'\mu}{L}(V_\mathrm{g} - V_\mathrm{t})}{1 + \frac{WC'\mu}{L}R_\mathrm{c}(V_\mathrm{g} - V_\mathrm{t})} = \frac{I_\mathrm{d}}{V_\mathrm{d}} \tag{3.10}$$

and

$$g_\mathrm{m} = \left(\frac{\partial I_\mathrm{d}}{\partial V_\mathrm{g}}\right)_{V_\mathrm{d}=\mathrm{const.}} = \frac{\frac{WC'\mu}{L}V_\mathrm{d}}{[1 + \frac{WC'\mu}{L}R_\mathrm{c}(V_\mathrm{g} - V_\mathrm{t})]^2} \ . \tag{3.11}$$

In practice, one differentiates the measured transfer curve numerically to determine $g_\mathrm{m}(V_\mathrm{g})$. In order to obtain an expression for μ one has to eliminate R_c by dividing eq. 3.10 by the square root of eq. 3.11, which yields

$$\frac{g_\mathrm{d}}{\sqrt{g_\mathrm{m}}}\sqrt{\frac{LV_\mathrm{d}}{WC'}} = \sqrt{\mu} \cdot (V_\mathrm{g} - V_\mathrm{t}). \tag{3.12}$$

Now, one derives eq. 3.12 with respect to V_g:

$$\frac{\partial}{\partial V_\mathrm{g}}\left(\frac{g_\mathrm{d}}{\sqrt{g_\mathrm{m}}}\sqrt{\frac{LV_\mathrm{d}}{WC'}}\right) = \sqrt{\mu}. \tag{3.13}$$

Squaring eq. 3.13 yields an expression for the gate voltage-dependent charge carrier mobility $\mu(V_\mathrm{g})$:

$$\mu(V_\mathrm{g}) = \left[\frac{\partial}{\partial V_\mathrm{g}}\left(\frac{g_\mathrm{d}}{\sqrt{g_\mathrm{m}}}\sqrt{\frac{LV_\mathrm{d}}{WC'}}\right)\right]^2. \tag{3.14}$$

Finally, solving eq. 3.10 for R_c leads to an expression for the contact resistance as a function of V_g:

$$R_\mathrm{c}(V_\mathrm{g}) = \frac{1}{g_\mathrm{d}} - \frac{L}{W\mu C'(V_\mathrm{g} - V_\mathrm{t})}. \tag{3.15}$$

Looking at eqs. 3.14 and 3.15, the question for the origin of the gate bias-dependent charge carrier mobility and contact resistance arises. In disordered organic semiconductors a gate voltage dependence of μ is predicted by models based on hopping of charge carriers in an exponential distribution of shallow traps [55]. The charge transport is assumed to be limited by shallow traps located close to the transport level. If the gate voltage increases the Fermi level at the insulator-semiconductor interface moves closer to the transport level and more traps are filled [56]. Hence, the mobility increases because trapping of charge carriers becomes less efficient. This behavior has been observed frequently in amorphous polymer FETs, where the hole mobility in OC_1C_{10}-PPV-based FETs increased by two orders of magnitude when varying V_g from 0 to $-20\,\mathrm{V}$ [57]. However, the variation is found to be significantly smaller for polycrystalline molecular OFETs due to a narrower distribution of traps [54].

3.2 Determination of doping and mobility in MIS diodes

3.2.1 Impedance Spectroscopy

Impedance spectroscopy has turned out to be a powerful, non-destructive technique to investigate the dynamics of charge transport processes in solids, e.g. charges at interfaces in MIS diodes or OLEDs [58]. In this thesis, impedance spectroscopy has been used to analyze the gate voltage dependence of accumulation and depletion regimes as well as charge carrier transport perpendicular to the substrate plane in ambipolar MIS diodes. This is a good complement to field-effect transistors which are the adequate devices to measure charge carrier transport parallel to the substrate.

The basic principles of impedance spectroscopy will be introduced in this section before the application to organic MIS diodes will be shown.

In impedance spectroscopy experiments, the top electrode of the MIS diode is grounded. At the gate electrode, a constant voltage V_g is applied, superimposed by a small AC voltage $\tilde{V}_\mathrm{AC}$, which can be written in complex notation [59]:

$$\tilde{V}_\mathrm{AC}(t) = V_\mathrm{AC} \cdot \exp\left(\mathrm{i}\, 2\pi f\, t\right). \tag{3.16}$$

Here, f denotes the frequency of $\tilde{V}_\mathrm{AC}$. The constant gate voltage is responsible for the regulation of the working-point of the diode (i.e. accumulation or depletion), whereas the physical information of the measurement is gained from the response of the sample with respect to the AC voltage. The modulus of the latter has to be small compared to V_g in order not to interact with it and thus not to change the working-point. The impedance spectroscopy setup measures the current response

$$\tilde{I}_\mathrm{AC}(t) = I_\mathrm{AC} \cdot \exp\left(\mathrm{i}\, 2\pi f\, t + \varphi\right) \tag{3.17}$$

with the general phase shift φ.

The complex impedance $\tilde{Z}$ is defined as the ratio of the applied alternating voltage and the current response and can be written as the sum of the real part $\mathcal{R}e(\tilde{Z})$, also referred to as effective resistance, and the imaginary part $\mathcal{I}m(\tilde{Z})$, also denoted reactance [60]:

$$\tilde{Z}(t) = \frac{\tilde{V}_\mathrm{AC}(t)}{\tilde{I}_\mathrm{AC}(t)} = \frac{V_\mathrm{AC}(t)}{I_\mathrm{AC}(t)} = \mathcal{R}e(\tilde{Z}) + \mathrm{i} \cdot \mathcal{I}m(\tilde{Z}). \tag{3.18}$$

Amongst other parameters, the capacitance C is a crucial quantity that can be measured by impedance spectroscopy. It is defined as

$$C(f) = \frac{1}{2\pi f} \cdot \frac{-\mathcal{I}m(\tilde{Z})}{\mathcal{R}e(\tilde{Z})^2 + \mathcal{I}m(\tilde{Z})^2}. \tag{3.19}$$

Another quantity that can be useful for the analysis of MIS diodes is the phase shift φ. It can be calculated via

$$\varphi = \arctan\left(\frac{\mathcal{I}m(\tilde{Z})}{\mathcal{R}e(\tilde{Z})}\right). \tag{3.20}$$

3.2.2 Gate voltage dependence of the capacitance

The field-effect in MIS structures was introduced in sec. 2.2.1. It was shown that, for a p-type semiconductor, accumulation of charge carriers at the semiconductor-insulator interface can be achieved for negative applied gate voltages, whereas the interface is depleted for positive values of V_g. In the case of an n-type semiconductor, the situation is vice versa. As already discussed in sec. 2.2.1, organic

semiconductors are not intentionally doped p- or n-type and often exhibit ambipolar characteristics where both charge carrier types can be accumulated. Thus, it is possible to obtain hole accumulation for negative V_g and electron accumulation for positive V_g in organic MIS diodes. For $V_g = 0$ the device is depleted if $V_{t,h} < V_{t,e}$, i.e. if there is a pronounced "off"-regime. This is the case for most devices analyzed in the course of this thesis. The width of the depletion regime depends on the respective threshold voltages. Typical values for the width of the depletion regime for devices used in this thesis are between $-10\,\mathrm{V}$ and $+10\,\mathrm{V}$. The measured capacitance as a function of the applied gate voltage for a typical ambipolar MIS diode with the accumulation and depletion regimes is plotted in the C-V-diagram fig. 3.3. For a better comparability, the capacitance per unit area C' is plotted.

The capacitance is calculated with the help of eq. 3.19 out of $\mathcal{R}e(\tilde{Z})$ and $\mathcal{I}m(\tilde{Z})$. These parameters are determined by the impedance spectroscopy measurement setup. The capacitance of the semiconductor depends strongly on the applied gate voltage. The MIS diode can be seen as a series of two resistance-capacitor circuits as shown in fig. 3.4(a). R_s and R_i stand for the resistance of the semiconductor and the insulator, respectively, whereas C'_s and C'_i denote the respective specific capacitances. Figs. 3.4(b)-(e) illustrate the gate voltage dependence of the capacitance schematically. In case of accumulation, (b) and (e), there is a conducting charge

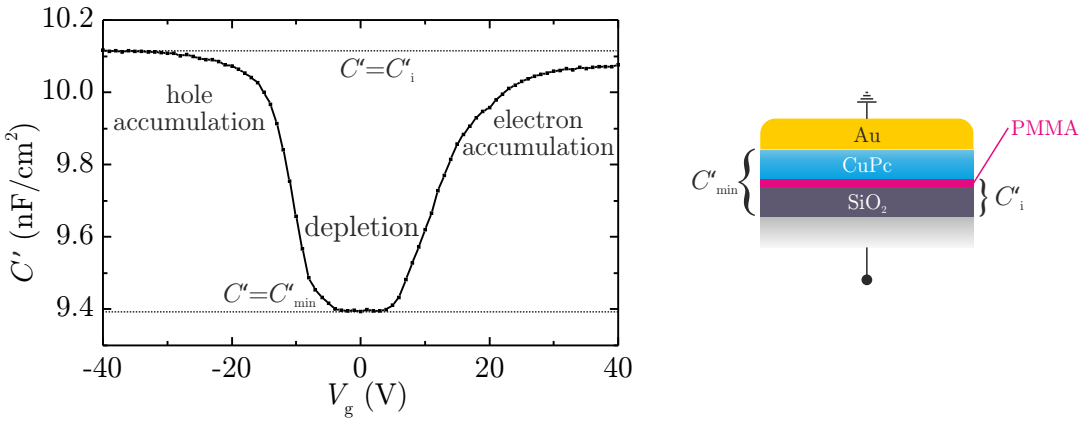


Figure 3.3: C-V diagram of an ambipolar CuPc MIS diode with Au contacts and PMMA passivation layer. In the accumulation regimes, the specific capacitance is given by the specific insulator capacitance C'_i. In the depletion regime it is determined by the geometric specific capacitance of the whole diode C'_{tot}. The layer thicknesses are: $d_{SiO_2} = 320\,\mathrm{nm}$, $d_{PMMA} = 20\,\mathrm{nm}$, $d_{CuPc} = 25\,\mathrm{nm}$. In the present case, it is assumed that the thickness of the CuPc layer is smaller then its depletion length l_{dep}, so that the device can be fully depleted.

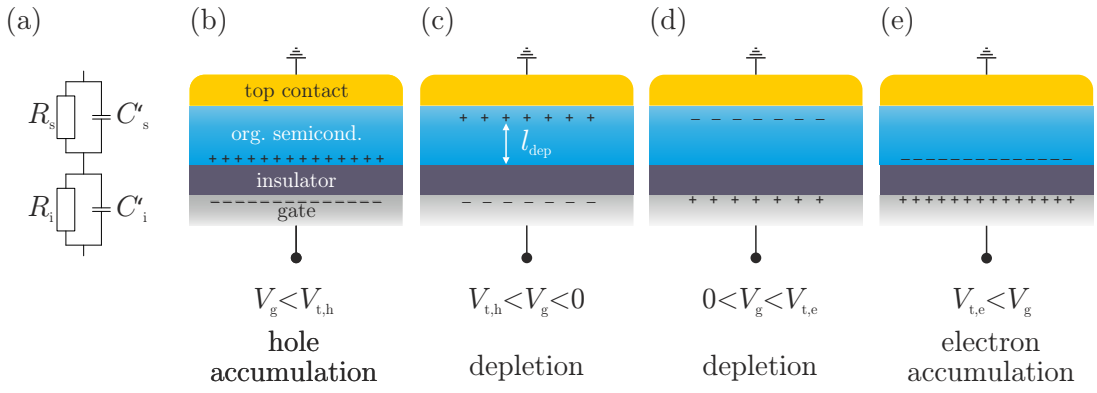


Figure 3.4: (a) Equivalent circuit for the description of an MIS diode, (b)-(e) schematic drawings to explain the different capacitances of an MIS diode in accumulation or depletion regimes. In the accumulation case, the insulator capacitance C'_i is measured, whereas in the depletion case, the resulting total capacitance corresponds to a series connection of the insulator capacitance and the depleted organic semiconductor with the depletion length l_{dep}.

carrier layer at the semiconductor-insulator interface, so that the semiconductor is short-circuited and the measured capacitance equals the geometric insulator capacitance C'_i given by

$$C'_i = \varepsilon_0 \varepsilon_i \frac{1}{d_i}. \tag{3.21}$$

Here, ε_0 is the vacuum permittivity, ε_i stands for the relative permittivity and d_i for the thickness of the insulator. We consider the quasi-static case of low measurement frequencies of the alternating voltage given in eq. 3.16. The case of higher frequencies will be discussed in the following section.

In case of depletion, depicted in figs. 3.4(c) and (d), the measured capacitance is lower due to the additional depletion layer. In the depletion regime, the total specific capacitance C'_{tot} is given by the series of the insulator capacitance and the depletion capacitance C'_{dep} [61]:

$$\frac{1}{C'_{tot}} = \frac{1}{C'_i} + \frac{1}{C'_{dep}} \tag{3.22}$$

If the thickness of the organic semiconductor d_s is smaller than its depletion length l_{dep}, the semiconductor will be depleted completely, if d_s is larger than its depletion length l_{dep}, the semiconductor will only be depleted up to l_{dep}. This results in two

different cases for the depletion capacitance C'_{dep}:

$$C'_{\mathrm{dep}} = \begin{cases} \varepsilon_0 \varepsilon_{\mathrm{s}} / l_{\mathrm{dep}} & \text{if } d_{\mathrm{s}} > l_{\mathrm{dep}}, \\ \varepsilon_0 \varepsilon_{\mathrm{s}} / d_{\mathrm{s}} & \text{if } d_{\mathrm{s}} \leq l_{\mathrm{dep}}, \end{cases} \tag{3.23}$$

with the relative permittivity of the semiconductor ε_{s}. The case $d_{\mathrm{s}} \leq l_{\mathrm{dep}}$ is assumed in fig. 3.3.

Mott-Schottky-Analysis

From fig. 3.3 it can be seen that there is no sharp transition between accumulation and depletion regimes but a pronounced transition region. The shape of the capacitance in this region can provide information about the doping concentration N_{d} of the organic semiconductor. Unintentional doping occurs due to chemical impurities in the semiconductor and should be as low as possible. The analysis of the $C(V)$-curve can be done by a technique developed by Schottky and Mott for inorganic semiconductors [32]. Following their approach, the capacitance in the transition region can be written as

$$\frac{1}{C'^2} = \frac{2\, V_{\mathrm{g}}}{\varepsilon_0 \varepsilon_{\mathrm{s}} e\, N_{\mathrm{d}}}. \tag{3.24}$$

One can obtain N_{d} by plotting $1/C'^2$ as a function of V_{g} and determining the slope of the graph in the transition region. The slope m is given by

$$m := \frac{\partial}{\partial V_{\mathrm{g}}} \left(\frac{1}{C'(V_{\mathrm{g}})^2} \right) = \frac{2}{\varepsilon_0 \varepsilon_{\mathrm{s}} e\, N_{\mathrm{d}}}. \tag{3.25}$$

Thus, the doping concentration can be calculated via

$$N_{\mathrm{d}} = \frac{2}{\varepsilon_0 \varepsilon_{\mathrm{s}} e} \cdot \frac{1}{m}. \tag{3.26}$$

For this analysis, it is important that the thickness of the semiconductor d_{s} is equal to or larger than its depletion length l_{dep}. Otherwise, the semiconductor layer is fully depleted and the measured capacitance is larger than the minimum depletion capacitance [61, 62]. In this case, one can only estimate an upper limit of the doping.

3.2.3 Frequency dependence of the capacitance

In addition to the gate voltage dependence there is also a frequency dependence of the capacitance of organic MIS diodes. The $C(V)$ characteristics in the preceding

section have been explained for the case of very low frequencies f of the external voltage $\tilde{V}_{\mathrm{AC}}$ given in eq. 3.16. The measured capacitance of the device will change drastically when the frequency is increased to higher values. This effect can again be illustrated with the help of the equivalent circuit shown in fig. 3.4(a).

The impedance of a parallel RC-circuit is given by

$$\tilde{Z}_{\mathrm{RC}} = \frac{1}{\frac{1}{R} + \mathrm{i}\omega C}. \tag{3.27}$$

With this, the frequency-dependent impedance of the whole circuit is

$$\tilde{Z} = \tilde{Z}_{\mathrm{R_sC_s}} + \tilde{Z}_{\mathrm{R_iC_i}}. \tag{3.28}$$

Calculation of $\mathcal{R}e(\tilde{Z})$ and $\mathcal{I}m(\tilde{Z})$ and substitution in eqs. 3.19 and 3.20 yield results for the capacitance and the phase shift as a function of the applied frequency [63]:

$$C(f) = \frac{R_{\mathrm{s}}^2 C_{\mathrm{s}} + R_{\mathrm{i}}^2 C_{\mathrm{i}} + 4\pi^2 f^2 R_{\mathrm{s}}^2 R_{\mathrm{i}}^2 \cdot C_{\mathrm{s}} C_{\mathrm{i}} \cdot (C_{\mathrm{s}} + C_{\mathrm{i}})}{(R_{\mathrm{s}} + R_{\mathrm{i}})^2 + 4\pi^2 f^2 R_{\mathrm{s}}^2 R_{\mathrm{i}}^2 \cdot (C_{\mathrm{s}} + C_{\mathrm{i}})^2} \tag{3.29}$$

and

$$\varphi = -\arctan\left(2\pi f \cdot \frac{R_{\mathrm{s}}^2 C_{\mathrm{s}} + R_{\mathrm{i}}^2 C_{\mathrm{i}} + 4\pi^2 f^2 R_{\mathrm{s}}^2 R_{\mathrm{i}}^2 \cdot C_{\mathrm{s}} C_{\mathrm{i}} \cdot (C_{\mathrm{s}} + C_{\mathrm{i}})}{R_{\mathrm{s}} + R_{\mathrm{i}} + 4\pi^2 f^2 R_{\mathrm{s}} R_{\mathrm{i}} \cdot (C_{\mathrm{s}}^2 R_{\mathrm{s}} + C_{\mathrm{i}}^2 R_{\mathrm{i}})}\right). \tag{3.30}$$

The capacitance and the phase shift versus frequency are plotted in fig. 3.5 (a) and (b) for different values of the semiconductor resistance R_{s}. The other parameters used for the simulation are given in the caption of fig. 3.5.

From fig. 3.5(a) it can be seen that each graph can be divided into two plateau regions separated by a transition region. The capacitance of the low-frequency plateau corresponds to the insulator capacitance C_{i}' whereas the capacitance of the high-frequency plateau corresponds to the capacitance of the whole device given by eq. 3.22 with

$$C_{\mathrm{tot}}' = \frac{C_{\mathrm{i}}' \cdot C_{\mathrm{s}}'}{C_{\mathrm{i}}' + C_{\mathrm{s}}'} = 11.3\,\mathrm{nF/cm^2}. \tag{3.31}$$

Thus, these two plateaus correspond to the same values as the capacitances determined for the accumulation and the depletion regime in sec. 3.2.2. This can be explained physically by the low charge carrier mobility of the organic semiconductor. For high applied gate voltages and low AC frequencies, the charge carriers can enter the semiconductor and accumulate at the interface: the insulator capacitance is measured. Upon increasing the frequency the charge carriers can follow the external electric field only up to a certain value, the relaxation frequency f_{r}. For higher values of f, the mobility of the carriers it too low to follow the AC field inside the semiconductor. Thus, the depletion capacitance is measured.

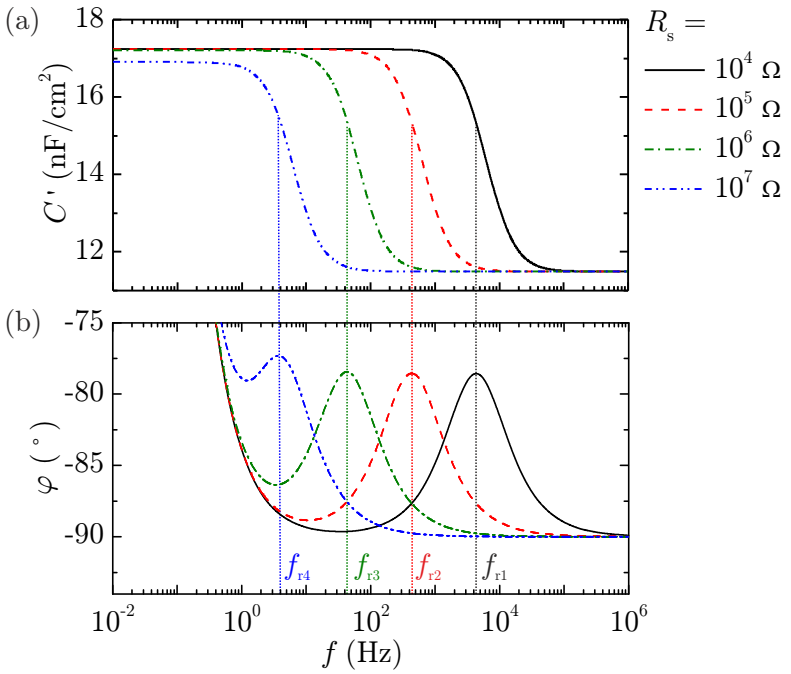


Figure 3.5: (a) Simulated C-f diagram of an MIS diode in the accumulation regime for different values of R_s. (b) Phase shift φ for the graphs shown in (a), the vertical lines highlight the respective relaxation frequencies f_r. The parameters used for the simulation are: $R_i = 10^9\,\Omega$, $C_s' = 34\,\mathrm{nF/cm^2}$ and $C_i' = 17\,\mathrm{nF/cm^2}$. This corresponds to layer thicknesses of $d_i = 200\,\mathrm{nm}$ and $d_s = 100\,\mathrm{nm}$ for dielectric constants of $\varepsilon_i = 3.9$ and $\varepsilon_s = 4$.

The position of the relaxation frequency is determined by the resistance of the semiconductor. This resistance is strongly correlated with the mobility: high values for R_s imply low values for μ. Consequently, the relaxation frequency is a measure for the mobility of the organic semiconductor perpendicular to the interface. The phase shift shown in fig. 3.5(b) has turned out to be useful for a precise determination of the relaxation frequency. For high frequencies, the capacitance is constant, the device acts as capacitor and the phase shift between real and imaginary part of the capacitance is $\varphi = -90°$. In analogy to the correlation between real and imaginary part of the dielectric function $\tilde{\varepsilon}$ in the case of Debye relaxation, a step of the capacitance C can be attributed to a peak of the phase shift φ. The peak position of φ can be identified as the relaxation frequency f_r, which in turn can now be used to determine the charge carrier mobility perpendicular to the substrate plane $\mu_\perp$. Alternatively, the dielectric loss $G(\omega)/\omega$, which has a similar line shape as φ is sometimes used to determine the relaxation frequency. Two possible approaches to extract $\mu_\perp$ will be explained in the following.

Determination of perpendicular mobility – doping approach

One approach to calculate the perpendicular mobility is to use the impurity doping concentration N_d given by eq. 3.26. Mathematically, the relaxation frequency can be written as [64]

$$f_\mathrm{r} = \frac{1}{2\pi\, A\, R_\mathrm{s}\, (C'_\mathrm{i} + C'_\mathrm{s})}, \tag{3.32}$$

where A denotes the area of the device. The semiconductor resistance R_s and the charge carrier mobility $\mu_\perp$ are related via

$$R_\mathrm{s} = \frac{d_\mathrm{s}}{eA\, N_\mathrm{d}\, \mu_\perp}. \tag{3.33}$$

The combination of these two equations finally leads to an expression for $\mu_\perp$:

$$\mu_\perp = \frac{2\pi\, d_\mathrm{s}\, f_\mathrm{r}\, (C'_\mathrm{i} + C'_\mathrm{s})}{e\, N_\mathrm{d}}. \tag{3.34}$$

If the thickness of the organic semiconductor is larger than the depletion length l_dep, one has to use $d_\mathrm{s} = l_\mathrm{dep}$ and $C'_\mathrm{i} = \varepsilon\varepsilon_0/l_\mathrm{dep}$ in eq. 3.34. This method is related to a variety of problems one being the Mott-Schottky analysis, which is done by a $C(V)$-measurement. As it has been discussed above, the thickness of the organic semiconductor must be larger than the depletion length. The depletion length is difficult to determine, it is assumed to be around 50 nm in our devices with $N_\mathrm{d} \approx 10^{17}\,\mathrm{cm}^{-3}$ [65]. Consequently, the organic semiconductor layer should be at least 50 nm thick. This can be counterproductive for the fabrication of devices with MIS diodes and OFETs on the same substrate since the film thickness of the organic semiconductor usually used in OFETs is only 25 nm and the bulk resistance between the top contacts and the channel increases for thicker semiconductor layers. Additionally, the Mott-Schottky analysis has been developed for inorganic semiconductors and the concept of doping cannot be adapted directly to organic semiconductors.

Other problems can be related to the determination of the relaxation frequency. Our model of the double RC-circuit is only an approximation. It has been suggested that a third RC-element for the accumulation layer should be included [61] or even more complex circuits have been proposed [64]. However, the deviations regarding f_r have turned out to be rather small [66, 67].

Determination of perpendicular mobility – diffusion approach

Stallinga *et al.* have developed an alternative approach to determine the perpendicular charge carrier mobility without using the Mott-Schottky analysis [68]. The

basic assumptions are equal to the previous approach: due to the low mobility of charge carriers in the organic layer the AC frequency must be low enough to ensure that the charge carriers have enough time to arrive at the interface. For higher frequencies they cannot follow the alternating electric field and the organic semiconductor layer becomes "insulating".

The model uses an equivalent circuit similar to the double RC-circuit used before but with $R_\mathrm{i} = \infty$. The key assumption of this approach is that the movement of the charge carriers is determined by diffusion and that the diffusion coefficient D of one charge carrier type and the mobility $\mu_\perp$ are linked by the Einstein relation:

$$D = \frac{\mu_\perp k_\mathrm{B} T}{e}. \tag{3.35}$$

A characteristic time τ is introduced, which is defined by the mean time the charge carriers need to reach the interface:

$$\tau = \frac{d_\mathrm{s}^2}{D} = \frac{e}{k_\mathrm{B} T} \cdot \frac{d_\mathrm{s}^2}{\mu_\perp}. \tag{3.36}$$

With the help of τ, a relaxation frequency $f_\mathrm{r} = (2\pi\tau)^{-1}$ can be defined. Hence, the perpendicular charge carrier mobility is given by

$$\mu_\perp = \frac{2\pi e f_\mathrm{r} d_\mathrm{s}^2}{k_\mathrm{B} T}. \tag{3.37}$$

This frequency is equivalent to the relaxation frequency and distinguishes the low-frequency regime ($C'_\mathrm{meas} = C'_\mathrm{i}$) from the high-frequency regime ($C'_\mathrm{meas} = C'_\mathrm{tot}$). The determination of the cut-off frequency is again identified with the maximum of the phase shift and enables the calculation of $\mu_\perp$ by using eq. 3.37.

Comparison of both approaches

Both approaches describe different charge transport processes. Whereas the first approach assumes all charge carriers to be moved by drift processes, the latter includes only diffusion processes. The doping method has been developed for the case of inorganic semiconductors with a single shallow acceptor [69]. This can cause problems when it is applied to organic semiconductors with an exponential distribution of trap states into the band gap. The diffusion model is not based on this assumption. In addition, it will be shown that in our experiments it is difficult to determine the doping concentration by the Mott-Schottky analysis in many cases. Due to these reasons, the diffusion approach turned out to be the preferential method as will be further discussed in chapter 9.

Chapter 4

Materials and experimental techniques

This chapter introduces all organic materials that were applied in the course of this thesis. The first part will present dielectric materials used as passivation layers or surface treatments for OFETs and MIS diodes while the second part covers the organic semiconductors. An alternative for conventional metals as top electrodes are organic metals which will be presented thereafter. Finally, the experimental techniques used for the fabrication of the samples and for the measurements will be explained.

4.1 Materials for organic field-effect devices

4.1.1 Dielectric passivation layers

A variety of different organic dielectric materials have been used as substrate treatments or additional dielectric layers. The purpose of these layers is to provide an insulator-semiconductor interface that is free of charge carrier traps and to enhance the device performance by improving the growth conditions of the organic semiconductor. Although they do not really passivate the trap states on the SiO_2 surface but only separate them spatially from the transport channel they are usually referred to as "passivation layers" in literature.

Octadecyltrichlorosilane

Octadecyltrichlorosilane (OTS) is a long-chain alkane molecule ($CH_3(CH_2)_{17}SiCl_3$) with a silicon anchor group at one end. The chemical structure of OTS is depicted in fig. 4.1(a). It is widely used as ultra-thin dielectric layer on various oxides to form a "self-assembled monolayer" (SAM), e.g. on silicon dioxide (SiO_2) as shown in fig. 4.1(b). These SAMs are highly chemically stable due to a bond between the silicon atom and an oxygen atom on the SiO_2 surface. The morphology of OTS-based SAMs depends strongly on the preparation conditions and can vary with respect to crystallinity and density [70]. Due to the highly hydrophobic character of an OTS monolayer the crystallization of the organic semiconductor deposited on top can be improved under certain conditions.

Poly(methyl-methacrylate)

Poly(methyl-methacrylate) (PMMA) is the polymer of the monomer methyl-methacrylate, $CH_2=C(CH_3)COOCH_3$. The chemical structure of PMMA is shown in fig. 4.1(c). PMMA can easily be dissolved in various organic solvents and spin-cast on many different kinds of substrates as will be described later. The molecular weight of the polymer used as a passivation layer in this thesis is 123,000 g/mol. Thin films of PMMA with a thickness of $18-20$ nm have been proven to provide a smooth, trap-free dielectric interlayer for OFETs [71, 72].

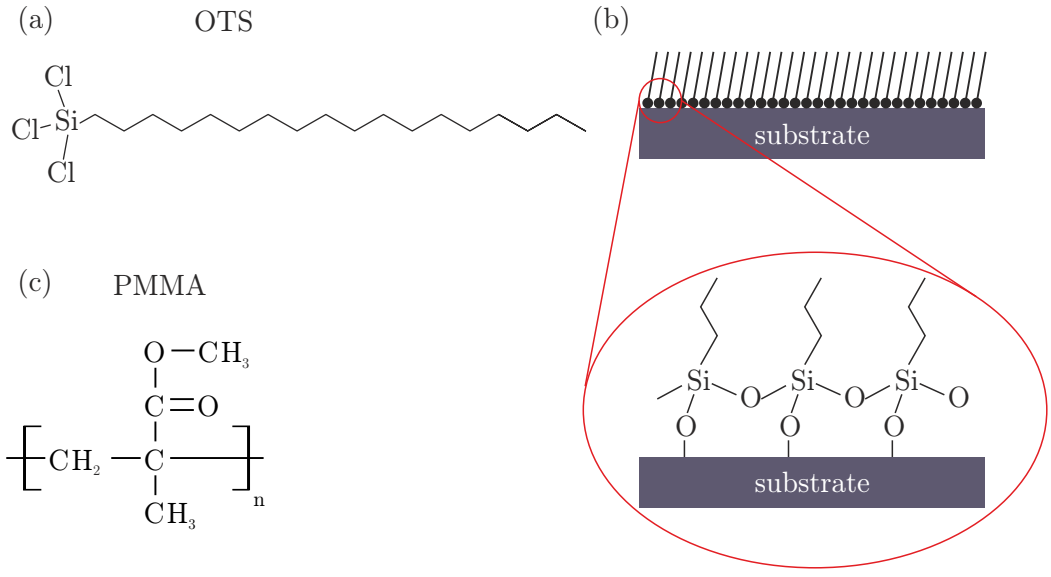


Figure 4.1: Chemical structure of OTS (a), formation of self-assembled monolayers on SiO_2 (b) and chemical structure of PMMA (c).

Tetratetracontane

Tetratetracontane (TTC) is a long-chain alkane molecule with the elemental formula $C_{44}H_{90}$. TTC is a good insulator with a band gap of $E_g = 9\,\text{eV}$ and an ionization potential of $I_P = 8.5\,\text{eV}$, which results in a LUMO positioned above the vacuum level [73]. A photograph of the white, waxy material and its molecular structure can be seen in fig. 4.2. The sublimation temperature of TTC is low ($T_{sub} \approx 100$℃), which enables the evaporation in vacuum deposition chambers. TTC is highly suitable as dielectric interlayer for field-effect devices because it provides a crystalline, trap-free interface and can furthermore enhance the crystallinity of the organic semiconductor grown on top [74, 75]. TTC is purchased from Sigma-Aldrich and used as received.

Figure 4.2: Appearance and chemical structure of TTC.

4.1.2 Organic semiconductors

The majority of the experiments discussed in this thesis are performed with copper-phthalocyanine (CuPc) already introduced in chapter 2. Officially, it is denoted as H_{16}CuPc due to its terminating hydrogen atoms. However, it is usually written as CuPc. Its molecular structure is again displayed in fig. 4.3(a) next to its perfluorinated counterpart, hexadecafluoro-copperphthalocyanine (F_{16}CuPc) shown in 4.3(b).

Copper-phthalocyanine

Phthalocyanines are a class of organic compounds with an alternating nitrogen-carbon ring structure. The most simple phthalocyanine molecule has two hydrogen

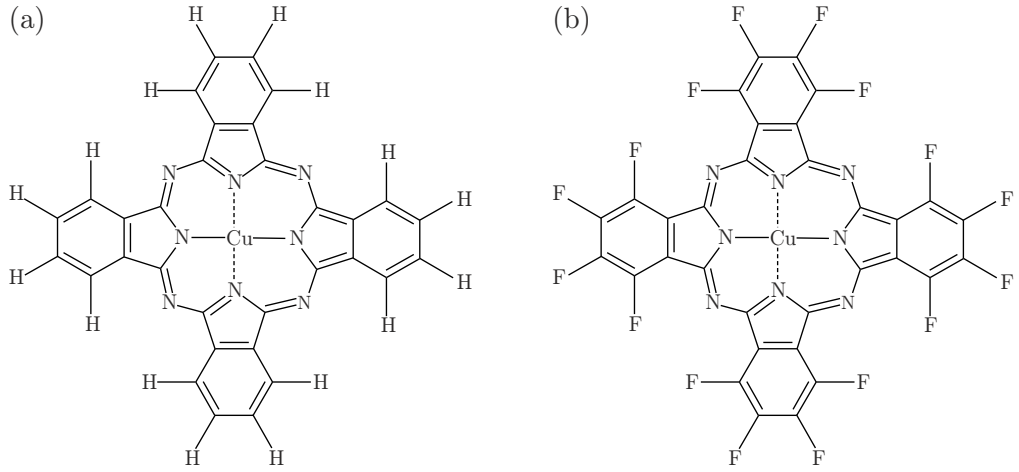


Figure 4.3: Molecular structure of H_{16}CuPc (a) and F_{16}CuPc (b).

atoms in the center, which can be replaced by various metal atoms, e.g. Fe, Zn, Pb or Cu.

CuPc is an intensely blue material that is widely used in industry, e.g. as dye for plastics. It features a high chemical stability, is non-degenerative in ambient air and non-toxic. Our material has been purchased from Sigma-Aldrich as sublimation grade and was additionally purified once by gradient sublimation. The resulting output material is shown in fig. 4.4(a). It consists of dark blue crystals that are insoluble to most conventional solvents but can be evaporated in vacuum effusion cells. CuPc can appear in several kinds of crystalline polymorphs, namely α-, β-,

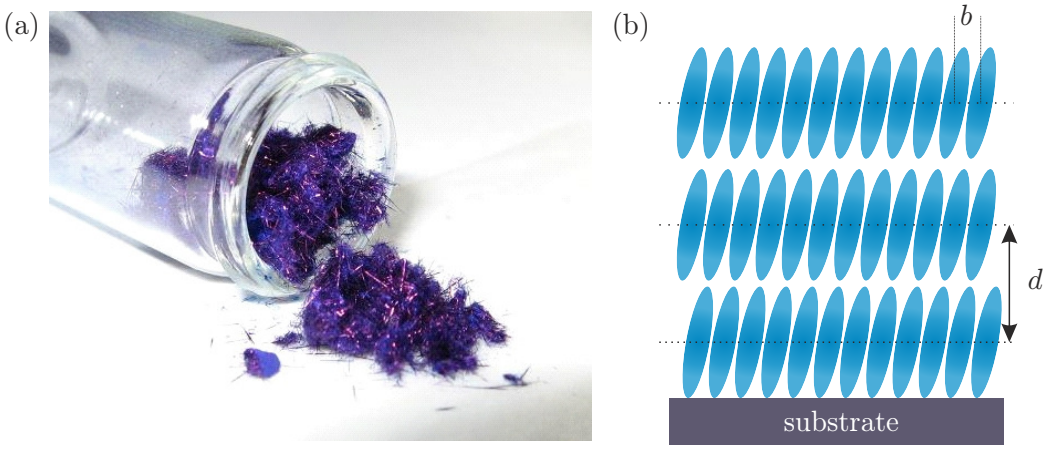


Figure 4.4: (a) Crystalline powder of gradient sublimated CuPc, (b) schematic sketch of α-phase CuPc. The distance between two neighboring molecules is $b = 3.8\,\text{Å}$, the lattice spacing is $d = 12.0\,\text{Å}$ [76].

γ-, and even more phases, but only α- and β-phases are usually obtained in thin films. [77].

The crystalline structure of α-phase CuPc has been subject of an intense debate for several years. Since most metal-phthalocyanines tend to form a herringbone structure, this was also assumed for α-CuPc [78]. However, more recent results indicate that this may be not the case. Hoshino *et al.* have performed thorough investigations and have concluded that the CuPc α-phase has a triclinic crystal structure with one molecule per unit cell and lattice constants of $a = 12.9\,\text{Å}$, $b = 3.8\,\text{Å}$ and $c = 12.0\,\text{Å}$. In the thin-film phase, the lattice spacing perpendicular to the substrate d corresponds to c, leading to $d = 12.0\,\text{Å}$ [76]. This is illustrated schematically in fig. 4.4(b). It can be seen that α-phase CuPc stands almost upright on most substrates like SiO_2 and that the molecular packing parallel to the substrate is significantly more dense than perpendicular to it. Consequently, the π-π-overlap is higher in parallel direction leading to better charge carrier transport properties in this direction, as will be seen later. Thin-films of CuPc on substrates that have not been heated during deposition are usually α-phase CuPc films. Since the α-phase is metastable, heating can lead to the stable β-phase.

The semiconducting properties of phthalocyanines have already been described in 1948 by Eley [79]. First applications of CuPc as active material for OFETs have been performed by Bao *et al.* and revealed good p-type characteristics with hole mobilities up to $2 \times 10^{-2}\,\text{cm}^2/\text{Vs}$ [80].

Recent studies suggest a transport gap of 1.8 eV and an ionization energy of 5.0 eV leading to the schematic energy diagram shown in fig. 4.5(a) [81, 82].

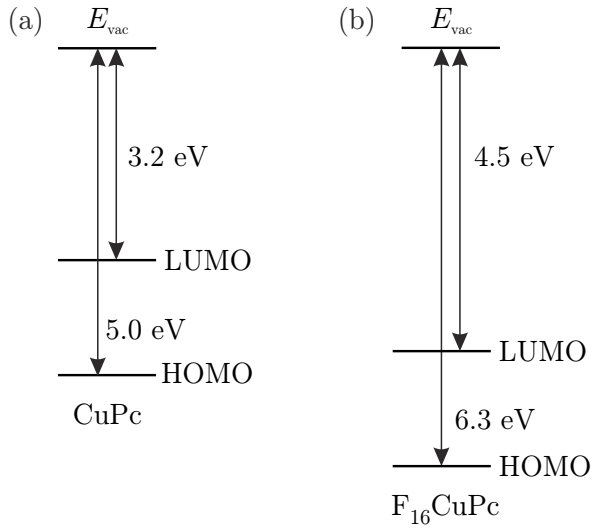


Figure 4.5: Schematic energy diagrams of CuPc (a) and F_{16}CuPc (b).

Hexadecafluoro-copperphthalocyanine

F_{16}CuPc is the perfluorinated variation of CuPc where all surrounding hydrogen atoms have been substituted by fluorine atoms, which changes the electrical properties of the material. F_{16}CuPc used for our experiments has also been purchased from Sigma-Aldrich and purified twice by gradient sublimation since fluorinated materials are known to be more contaminated, e.g. due to only partly fluorinated phthalocyanines. The result is a crystalline powder with blue color.

As with CuPc, the crystal structure of F_{16}CuPc is not completely clear. Some groups describe the appearance of two phases differing with respect to the orientation of the molecules and the packing density [83]. The β_{bilayer}-phase is supposed to be similar to the α-phase of CuPc with a lattice spacing of 14.6 Å, whereas the β-phase reveals a herringbone structure and a closer packing with a lattice constant of only 10.1 Å. X-ray measurements on F_{16}CuPc films deposited in our evaporation chamber exhibit a lattice spacing of $d = 14.3$ Å, implying that the β_{bilayer}-phase is formed [84].

OFETs with F_{16}CuPc as active material have been realized for the first time in 1998 [85]. In contrast to CuPc, F_{16}CuPc shows only unipolar n-type characteristics. Electron mobilities up to $2 \times 10^{-2}\,\text{cm}^2/\text{Vs}$ have been achieved for thin films deposited on heated substrates. As a consequence of the strong electron-withdrawing character of the flourine atoms the ionization potential is significantly increased compared to CuPc ($I_\text{P} = 6.3\,\text{eV}$), whereas the optical gap was found to be nearly identical to CuPc, leading to the schematic energy diagram given in fig. 4.5(b) [86, 87].

4.1.3 Organic metals

Organic metals are a class of molecular charge transfer compounds consisting of a strong electron donor and a strong electron acceptor. They can exhibit metal-like conductivity. Most of the materials are composed of a mixture of tetrathiafulvalene (TTF) or tetraselenafulvalene (TSF) and tetracyanoquinodimethane (TCNQ) or its fluorinated derivatives F_nTCNQ with $n = 1$, 2 or 4. The molecular structure of all these materials used in the course of this thesis are shown in fig. 4.6. The compounds TTF-TCNQ and TSF-F_2TCNQ have been used as top contacts for OFETs. The neutral molecules form alternatingly stacked crystals in these compounds [88, 89]. The compounds are relatively stable to ambient conditions and can be evaporated in vacuum effusion cells.

When using organic metals as top contacts for OFETs the work function of the

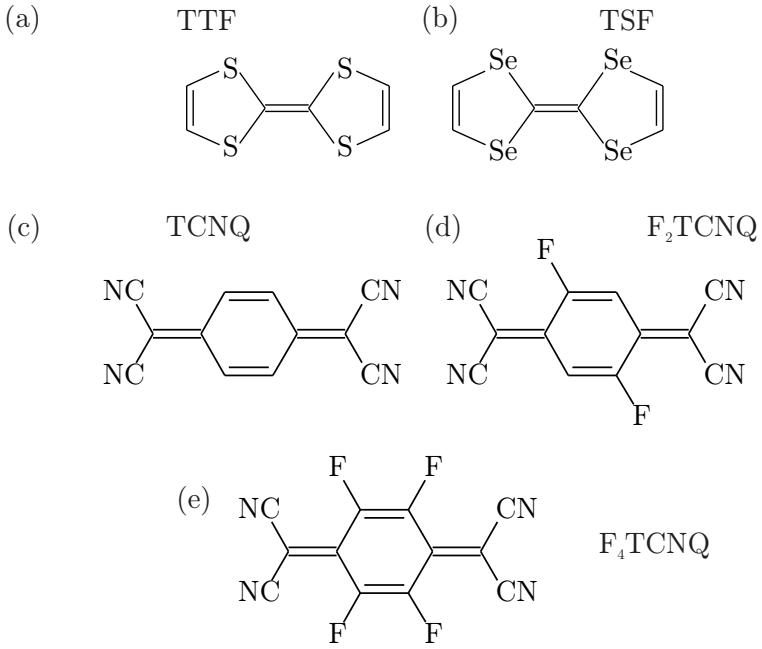


Figure 4.6: Molecular structure of (a) TTF, (b) TSF, (c) TCNQ, (d) F_2TCNQ and (e) F_4TCNQ.

metal ϕ_m is a key parameter that determines the injection of electrons or holes as will be discussed in more detail in sec. 6.1.1. In contrast to inorganic metals there is almost no data available regarding the work function of organic charge transfer compounds. Only the work function of TTF-TCNQ was estimated to be between 4.6 and 4.8 eV by Shibata *et al.* [90]. Grobman *et al.* determined a work function of 5.6 eV for TTF-TCNQ by photoemission spectroscopy [91]. Takahashi *et al.* developed a model to estimate the work function of charge transfer compounds as displayed schematically in fig. 4.7 [92]. The calculations are based on the ionization potential of the donor I_p^D and the electron affinity of the acceptor E_A^A. The diagram displays the positions of the respective values of the organic donors and acceptors. The work function of the metallic compound ϕ is supposed to be located at the center between the HOMO of the donor, given by I_p^D and the LUMO of the acceptor, given by E_A^A. Thus, it should shift by $(I_\mathrm{p}^\mathrm{D} + E_\mathrm{A}^\mathrm{A})/2$ along the vertical axis when the material combinations are varied. As a consequence, it is possible to tune ϕ by varying the material combinations. The approximate position of ϕ is given by the intersection of I_p^D and E_A^A of the respective materials. It is indicated by the dashed lines pointing to the ϕ axis. It has to be pointed out that the overall difference between TTF-TCNQ, which has the lowest value of ϕ and TSF-F_2TCNQ, which has the highest, is relatively small, approximately $0.3 - 0.4$ eV.

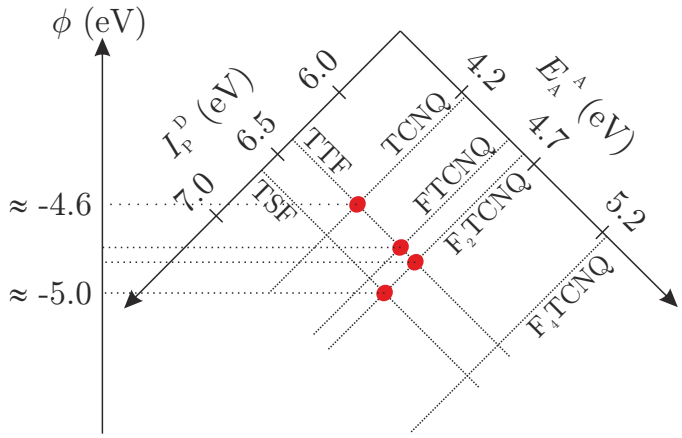


Figure 4.7: Diagram to estimate the work function differences for combinations of organic charge transfer compounds [92]. Ionization potentials are taken from [93], electron affinities from [94].

F_4TCNQ

F_4TCNQ is a strong organic acceptor with an ionization potential and electron affinity of $I_\mathrm{p} = 8.3\,\mathrm{eV}$ and $E_\mathrm{A} = 5.2\,\mathrm{eV}$, respectively [95]. Its molecular structure is shown in fig. 4.6(e).

This material is commonly used as *p*-type dopant in organic hole transporting layers to enhance performance or as a thin interlayer between metal top contacts and an organic semiconductor in order to enhance hole injection and suppress electron injection into the active layer [96, 97]. Since the electron affinity of F_4TCNQ is larger than the ionization potential of CuPc, a charge transfer can occur when F_4TCNQ is deposited on CuPc. This can lead to *p*-type doping of the CuPc layer, as will be seen later.

4.2 Sample preparation

4.2.1 Fabrication of transistors

Wafer preparation and cleaning

All transistors shown in this theses are built on substrates based on silicon (100)-wafers. The highly *p*-doped wafers ($\rho < 0.1\,\Omega\mathrm{cm}$) are covered with a 310 nm - 320 nm thick layer of SiO_2. Alternatively, wafers with only 120 nm SiO_2 are used for MIS diodes. The wafers are cut into $20 \times 20\,\mathrm{mm}^2$ pieces and subsequently cleaned.

Cleaning of the wafer pieces is performed in a clean room in an ultrasonic bath with highly-pure acetone and isopropanol successively. Thereafter, the substrates are dried in a nitrogen stream.

Self-assembled monolayers

The substrates that are treated with an OTS monolayer have to possess a hydrophilic surface with many hydroxyl groups prior to the deposition of the SAM. This is necessary to enable a reaction between the $SiCl_3$ anchor group of the OTS molecule and the SiO_2 surface, which ensures a chemically stable bond, as illustrated in fig. 4.1(b). In order to render the surface hydrophilic the cleaned wafer pieces are etched in an oxygen plasma for 120 s at a power of 400 W and an oxygen pressure of 500 mTorr. Thereafter they are stored in a solution of 9.4 µl OTS in 25 ml n-heptane for at least 12 hours. Subsequently, they are cleaned in an ultrasonic bath of highly-pure chloroform for 15 minutes. The OTS-treated substrates are strongly hydrophobic with water contact angles of ca. 100° in contrast to ca. 40° for cleaned untreated wafers.

PMMA passivation layers

As described in the preceding section, PMMA can be used as trap passivation layer on SiO_2. For this purpose, purified PMMA is dissolved in xylene to a 1.0 wt. % solution. The latter is stirred over night on a hotplate at 50°C. Finally, the solution is filtered. PMMA layers are fabricated by spin-coating with a rotation speed of 5000 rpm for a duration of 20 s. Thereafter, the substrates are dried on a hotplate at 50°C for several minutes. This procedure results in $18 - 20$ nm thick, smooth PMMA layers with water contact angles around 85°.

Evaporation of organic materials

Thermal evaporation is a common way for the deposition of molecular organic materials. Here, it is used to fabricate TTC passivation layers, organic semiconductor layers of CuPc and F_{16}CuPc and for organic metal top contacts. Fig. 4.8 shows a schematic sketch of an evaporation chamber. The chamber features two effusion cells, which can be used simultaneously to perform coevaporation of different materials for molecular blends or doping. The materials are filled into quartz crucibles and the chamber is evacuated to a pressure of $p < 10^{-7}$ mbar. The substrates are mounted onto a sample holder and brought from the glovebox into the chamber via a vacuum transfer system without exposure to air.

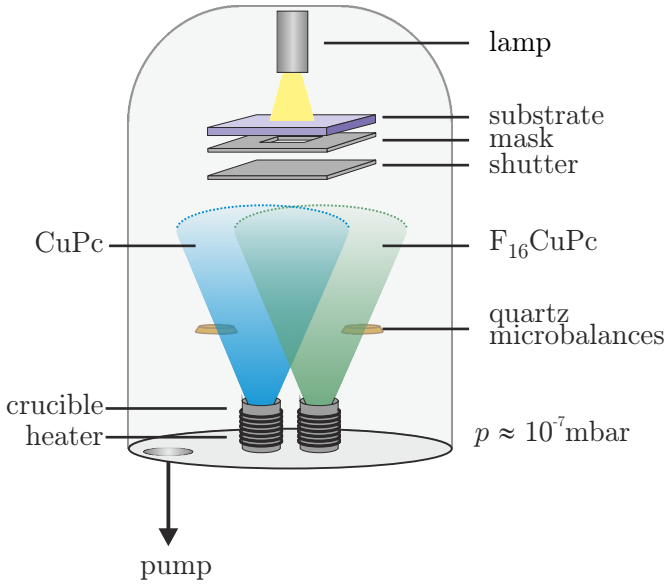


Figure 4.8: Schematic sketch of an evaporation chamber that can be used for the deposition of CuPc and F_{16}CuPc.

When the organic material is heated up to its sublimation temperature the molecules start to evaporate, forming a "molecular beam" which can adsorb on the surface of the substrate. The deposition rate and the deposited thickness are determined by a quartz microbalance by measuring the resonance frequency of a quartz crystal inside the vapor beam. Material is constantly deposited onto the crystal, which causes a reduction of its resonance frequency due to the increasing mass. The frequency shift can be related to the thickness of the deposited layer if some geometric and material parameters are known or determined by calibration measurements [98]. The deposition rate can be controlled via the temperature of the crucible. Shadow masks are usually placed underneath the sample to structure the deposited layers. With the help of a halogen lamp placed in a copper block above the sample holder it is possible to heat the substrate during evaporation. This enhances the diffusion of the adsorbed molecules on the surface and thus can change the morphology of the film.

For the fabrication of TTC layers, the cleaned wafer pieces are mounted to the sample holder inside the glovebox and transferred to the vacuum chamber. In contrast to most organic semiconductors, which sublimate directly, insulating TTC melts at $70 - 80$°C and subsequently evaporates at approximately 100°C. During deposition the temperature of the crucible has to be increased slowly up to 130°C in order to obtain a constant evaporation rate of ca. 0.1 Å/s. TTC films of various thicknesses from the sub-monolayer range up to 30 nm are fabricated. TTC layers

are deposited without using any shadow masks in FET structures. Some of the TTC-covered substrates are annealed after deposition. These substrates are placed in an oven inside the glovebox and annealed at 60℃ for 120 minutes in nitrogen atmosphere. As will be seen later, this treatment drastically reduces the surface roughness. Contact angle measurements exhibit a water contact angle of 105° for TTC-covered SiO_2, comparable to OTS-treated wafers.

Deposition of CuPc and F_{16}CuPc layers is performed in a chamber similar to the one shown in fig. 4.8. The cleaned, OTS-treated, PMMA- or TTC-covered substrates are transferred into the chamber. Evaporation temperatures are approximately 390℃ for CuPc and 350℃ for F_{16}CuPc. The deposition rate is kept constant at 0.2 Å/s, CuPc thickness is 25 nm for most of the investigated transistors. In some cases, the substrate is heated during deposition. In other cases, coevaporation of CuPc and F_{16}CuPc is performed, where the ratio between the two materials is determined by the respective deposition rates that can be monitored independently.

Metal top contacts with a thickness of 50 nm are deposited in a third chamber directly connected to the glovebox. The following metals are used: gold, silver, aluminum and calcium. Au and Ag are evaporated out of tungsten boat sources, for Al a boron nitride crucible heated by a tungsten coil is used, whereas Ca is sublimated directly from a tungsten basket.

Organic metals are deposited in the same chamber as TTC through a mask for the metal top contact. A significantly higher thickness is needed for organic metals to form a conducting layer, typically $150 - 300$ nm [99].

A schematic sketch of a complete OFET with passivation layer is given in fig. 4.9(a). There are two different transistor layouts used in this thesis. In layout 1, the semiconductor layer is unstructured and the corresponding metal mask provides a total of 20 transistors with channel lengths from 80 to 180 µm arranged in two separated arrays, depicted in fig. 4.9(c). This allows for the fabrication of two sets of transistors on the same substrate differing with respect to passivation layers, semiconductor or top contacts. Other advantages are the availability of more than one transistor of each channel length and the large channel width of 10 mm, which results in high drain currents. However, this layout exhibits two severe disadvantages, the main one being the unstructured semiconductor layer which leads to high gate leakage currents. The other disadvantage are the relatively large channel lengths, which hinder a precise TLM analysis. Therefore, layout 2 is used for the majority of experiments of this thesis, shown in fig. 4.9(d). Two masks are applied for transistors fabricated with this layout. One mask for the organic semiconductor and one for the metal contacts. It features channel lengths from 50 to 150 µm, which results in reduced errors for the TLM measurement. Additionally, the structured

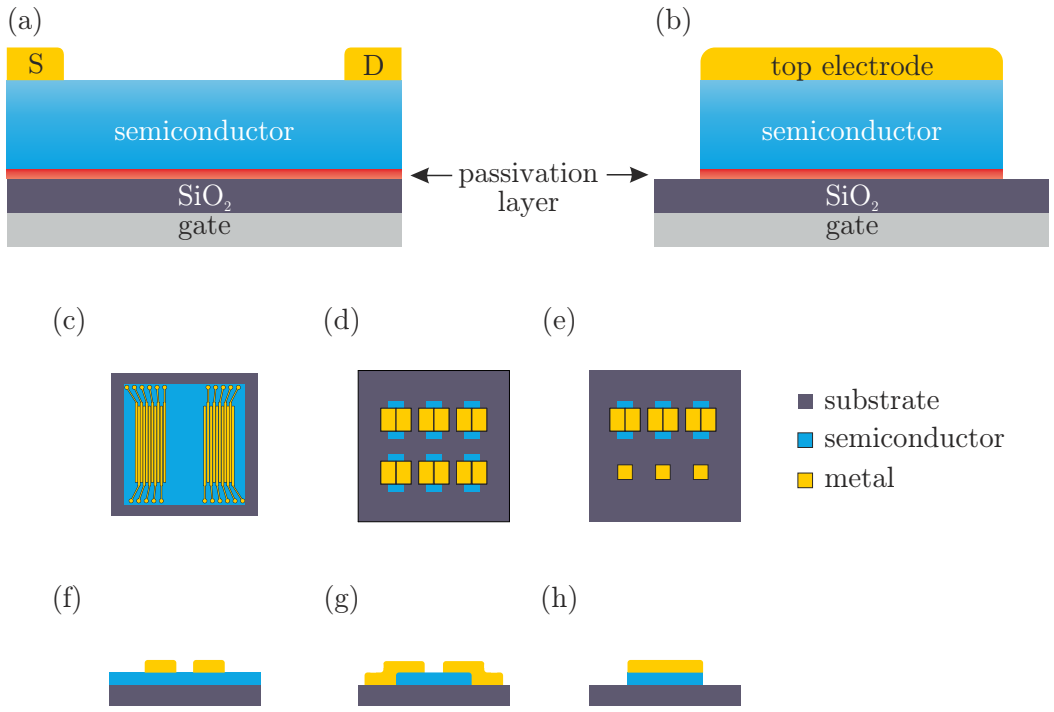


Figure 4.9: Device configurations of devices used in this thesis. Side view of an OFET (a) and an MIS diode (b), top views of OFET layout 1 with unstructured semiconductor layer and channel lengths between 80 µm and 180 µm (c), OFET layout 2 with structured semiconductor and channel lengths between 50 µm and 150 µm (d) and layout with OFETs and MIS diodes on the same substrate (e). (f)-(h) Cross sections of one device of (c)-(e).

semiconductor layer drastically reduces leakage currents through the gate insulator due to the separation of the individual transistors. Figs. 4.9(f) and (g) depict cross sections of one transistor of the layouts shown in (c) and (d), respectively.

4.2.2 Fabrication of MIS diodes

The individual fabrication steps of MIS diodes are similar to the ones described for OFETs with some minor differences. Since the constant DC gate voltage that can be applied during the impedance measurement is limited to values between −40 and +40 V, the threshold voltage has to be minimized in order to reach accumulation of holes and electrons. This can be done by increasing the capacitance of the gate insulator. Thus, wafers with only 120 nm SiO_2 are used for some experiments. Furthermore, it is important that the dimensions of the metal top electrode matches exactly the underlying organic semiconductor. Otherwise, parasitic capac-

itances due to metal touching the insulator would distort the measurement. Such an accurate alignment cannot be achieved by a multi-step shadow mask process. Consequently, a different structuring technique is applied for MIS diodes.

Substrates for MIS diodes are usually structured in a way that there are OFETs and MIS diodes on the same substrate to exclude any errors due to differences in preparation conditions when comparing the two devices. Therefore, one metal mask is cut into two pieces. Half of the cleaned substrate is masked with thin stripes of tape forming squares, of which the accurate size is determined with the help of a microscope after all measurements are done. Following the evaporation steps, the tape is removed and well-defined MIS structures as depicted in fig. 4.9(b) remain on the substrate. Thus, OFET structures are fabricated on one half of the samples whereas MIS diodes are on the other half, as displayed in fig. 4.9(e). The cross section of one diode is shown in (h).

4.3 Measurement techniques

Electrical transport measurements

Electrical transport measurements on OFETs and MIS diodes are done in a cryostat built by Cryovac displayed in fig. 4.10(a). All measurements are performed in high vacuum at a pressure of $p \approx 10^{-6}$ mbar. The samples are transferred to the cryostat without exposure to air. Source and drain electrodes are carefully contacted by needle probers, as depicted in fig. 4.10(b), whereas the gate is contacted by gluing the highly-doped wafer to the metal sample holder by silver paste. The source electrode is connected with the ground unit of the measurement system, a Keithley 4200 semiconductor parameter analyzer. Drain and gate electrodes are connected to individual source measure units of the system. Thus, it is possible to apply gate and drain voltages and measure gate and drain currents independently. The temperature in the cryostat can be controlled to investigate the temperature dependence of the electrical transport properties. This is done by cooling the sample holder with liquid nitrogen and simultaneously heating the sample holder to reach stable temperatures. The cryostat is equipped with four needle probers so that inverters can be contacted as well. Details about inverter measurements are given in chapter 11.

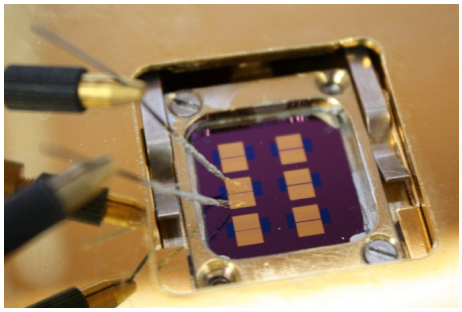
(a)  (b) 

Figure 4.10: (a) Cryostat in which the electrical characterizations of OFETs and MIS diodes are performed. (b) Contacting of an OFET with two needle probers inside the cryostat. The gate is contacted via the sample holder.

Impedance spectroscopy

Impedance spectroscopy measurements are also performed in the cryostat at high vacuum. Fig. 4.11 depicts a schematic overview of the setup. The gate and the metal top contacts are connected to "high" and "low" contacts of the measurement setup, respectively. The setup consists of a frequency response analyzer (Solartron SI 1260 Impedance/Gain-Phase Analyzer) combined with a dielectric interface (Solartron 1296). It features a frequency range from 10^{-2} to 10^{7} Hz for $C(f)$ and a voltage range from -40 to 40 V for $C(V)$ measurements. The amplitude of the AC voltage is set to 0.1 V. The frequency response analyzer measures the magnitude and the phase of the complex impedance and exports the real and imaginary parts of $\tilde{Z}$, out of which all other parameters can be calculated.

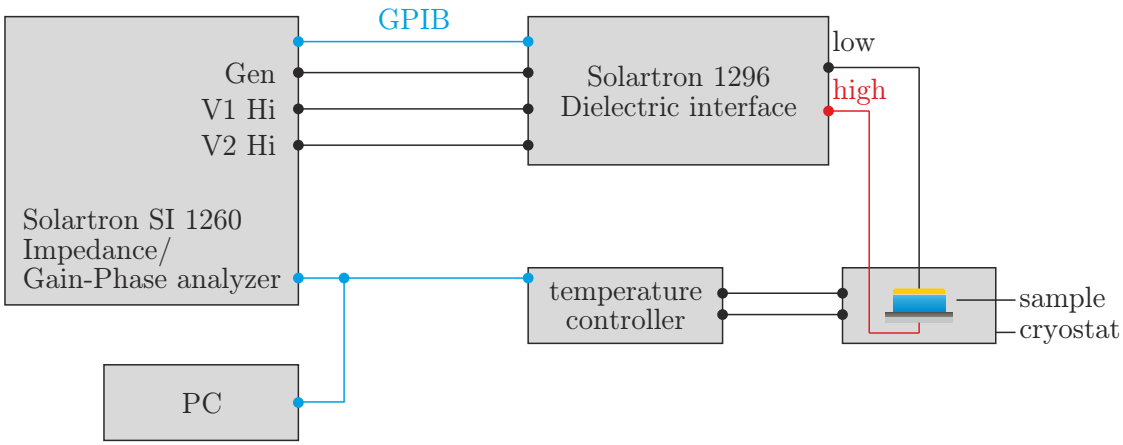


Figure 4.11: Schematic overview of the impedance measurement setup.

Atomic force microscopy

Atomic force microscopy (AFM) is a widespread technique to analyze the topography of surfaces with lateral dimensions in the micrometer range. Detectable height differences are in the nanometer regime. It has been developed in 1986 by Binnig *et al.* [100]. Sometimes it is also referred to as "scanning force microscopy". The basic principle of an AFM is the interaction between a small tip mounted on a cantilever and the sample surface. A systematic sketch of an AFM is given in fig. 4.12. An Autoprobe CP-Research microscope from Thermo-Microscopes is used for the experiments discussed in this thesis. The mechanical forces between the surface atoms and the tip depend on their relative distance. Thus, by detecting the deflection of the cantilever due to these forces, it is possible to obtain information about the height of a certain point on the surface. A convenient method to measure the deflection is to use a laser beam pointing onto the cantilever where it is reflected and detected by a 4-quadrant photo detector. The movement of the cantilever in all three space directions is done by a piezo stage. An AFM can be operated in several different modes, whereas the "tapping mode" is usually chosen for soft organic materials. The cantilever oscillates close to its resonance frequency. When the tip is moved across the surface the interactions with the surface atoms shift the resonance frequency further away from the driving frequency and the amplitude is decreased. This information can be used by a regulation circuit to construct a two-dimensional height profile with the help of a measurement software. The root mean square roughness R_{RMS} is often used to characterize a given surface. R_{RMS} is defined as the standard deviation of the average surface height. While it can be a useful parameter to compare different surfaces, it has to be used with care. Very smooth surfaces with only one major distortion (e.g. due to dust) can exhibit higher values for R_{RMS} than constantly rough surfaces. This underlines that the

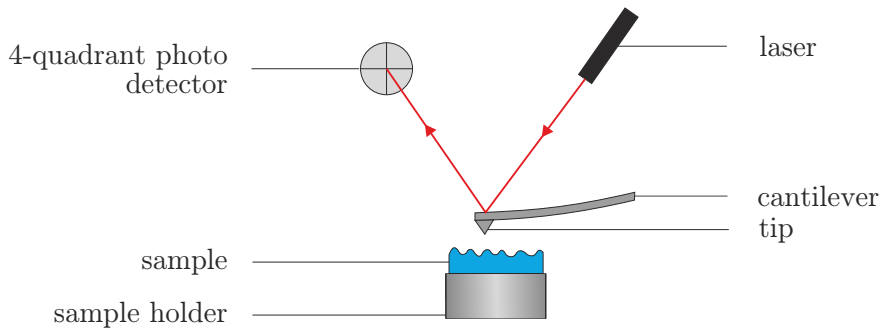


Figure 4.12: Schematic sketch of an AFM. The height profile of a sample can be obtained by measuring the interaction between the tip and the atoms on the surface of the specimen.

RMS roughness is only useful when it is shown together with the measured AFM image to check if it is representative for the whole film. Additionally, since charge carrier transport is limited to the first few nanometers of the organic semiconductor in OFETs, the roughness is not a crucial parameter for the transport as long as the films are closed but the roughness of the dielectric surface is a key limiting factor to charge carrier transport as will be seen in chapter 7.

X-ray diffraction

AFM can also give information about the crystallite size of polycrystalline layers. However, the crystalline phase of a material cannot be determined by AFM. That is why X-ray diffraction (XRD) is used for this purpose. XRD is a common technique to analyze the structural properties of all kinds of specimens, inorganic or organic. A schematic drawing of an XRD setup is shown in fig. 4.13(a). The X-ray tube is mounted on one side of the setup, the turnable sample holder at the center and the detector, which can be moved along a circle around the sample holder, is on the opposite side. Monochromatic X-rays hit the sample at the angle Θ. In case of a crystalline sample the radiation can be reflected if the Bragg condition

$$2\,d_{\mathrm{hkl}} \cdot \sin\Theta = n \cdot \lambda, \quad \text{with } n = 1, 2, 3, ... \tag{4.1}$$

is fulfilled. Here, d_{hkl} denotes the distance between the lattice planes, shown in fig. 4.13(b).

The reflected radiation can be measured if the detector is located at 2Θ relative to the incident beam. d_{hkl} can be determined by the angular positions of the maxima of the spectrum. In our polycrystalline films it is only possible to obtain information

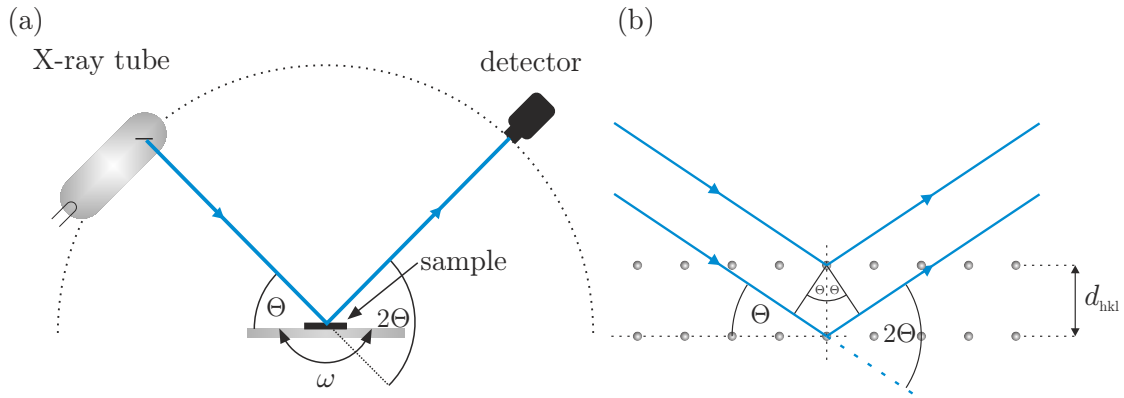


Figure 4.13: (a) Schematic drawing of an XRD setup, (b) illustration of Bragg reflection.

about the lattice constant perpendicular to the substrate plane since all individual crystallites are randomly oriented. The average tilt angle of the crystallites (also referred to as mosaicity) can be determined by an ω-scan or "rocking curve". Here, sample and detector are adjusted to a resonance position. Subsequently, the sample holder is tilted by a small angle ω while the reflected intensity is measured. The width of the peak is related to the average tilt of the crystallites. Usually, the *rocking width*, i.e. the full-width at half-maximum (FWHM) of a peak is determined when a rocking scan is performed.

XRD measurements presented in this thesis are performed on a Seifert XRD 3003 PTS in Augsburg or on a GE/Seifert setup in Tübingen. In both cases, Cu-K_α radiation with $\lambda = 1.54\,\text{Å}$ is used.

Chapter 5

Unipolar *p*-type transistors based on CuPc

The first experimental chapter covers unipolar *p*-type transistors with CuPc as active material. The morphology of CuPc thin films on SiO_2 substrates with different substrate treatments will be investigated and related to the properties of corresponding OFETs.

5.1 Morphology

5.1.1 AFM measurements

The morphology of the organic semiconductor is crucial for the characteristics of an OFET. It is indispensable to analyze its morphology to be able to understand and improve the device performance. The most simple OFET structure used in this thesis consists of 25 nm CuPc on 310 nm SiO_2 and 50 nm metal top contacts, displayed in fig. 5.1(a). Here, CuPc is grown directly on SiO_2. Consequently, one has to investigate the growth of CuPc on SiO_2. Since CuPc tends to grow in a polycrystalline way, the size of the crystallites is a key parameter of the film. Fig. 5.1(c) depicts an AFM image of a $2 \times 2\,\mu m^2$ section of 25 nm CuPc on SiO_2. The substrate was kept at room temperature during semiconductor deposition. The height of an individual point is given by its color. Black color symbolizes the lowest-lying parts of the surface whereas white color symbolizes the most elevated

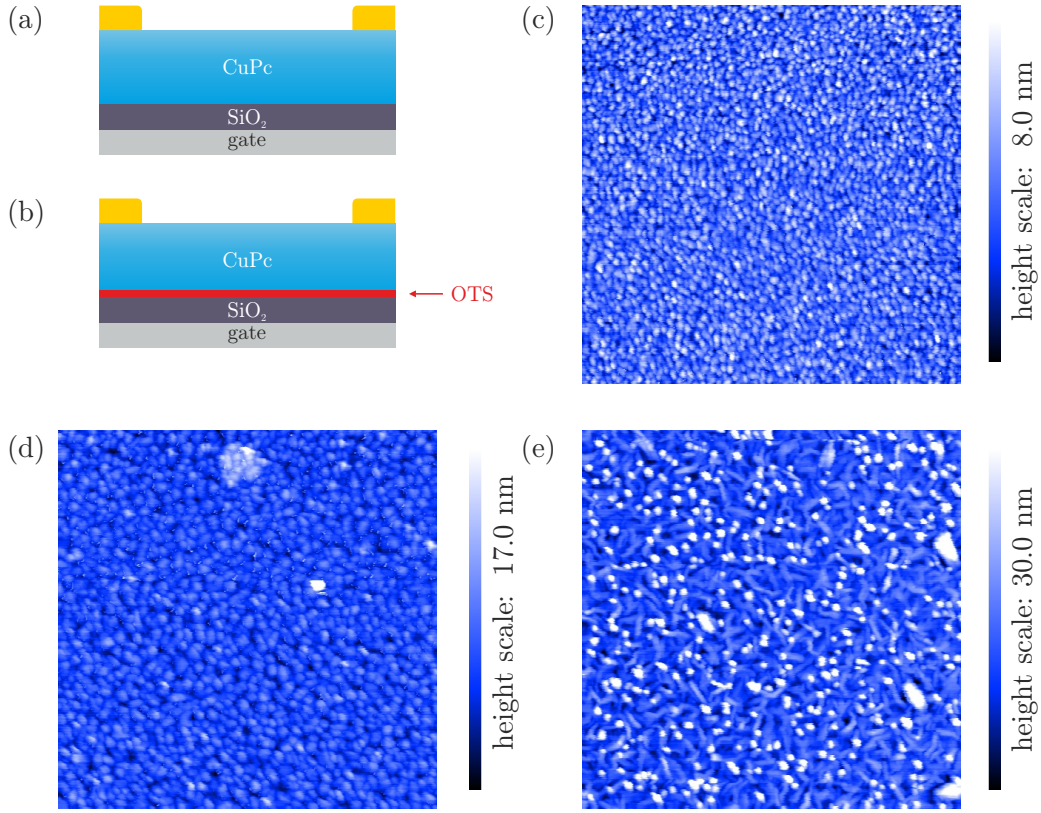


Figure 5.1: Schematic layout of the OFET without any passivation layer (a) and with OTS-treated SiO_2 (b). AFM images of a polycrystalline layer of 25 nm CuPc on SiO_2 (c), on OTS-treated SiO_2 (d) and on OTS-treated SiO_2 at a substrate temperature of 100°C (e). All sizes are $2 \times 2\,\mu m^2$.

parts. The total height difference is given by the height scale, which is 8.0 nm in this case. A granular structure can be seen, which reflects the individual grains of the polycrystalline layer. The surface is smooth and regularly patterned with an RMS roughness of $R_{RMS} = 1.0\,nm$ and a typical lateral crystallite diameter of $d_{cryst} = 40 - 50\,nm$.

In polycrystalline OFETs, charge carrier transport is predominantly limited by the low inter-grain mobility of the charge carriers, i.e. transport from one grain to another [31]. Therefore, a semiconductor layer with large crystallites and few grain boundaries is desirable. In order to increase the crystallinity of organic semiconductor layers, organosilane SAMs like OTS are known to be highly suitable [101]. The surface of the OTS layer is very hydrophobic due to the aliphatic tails of the SAM. Thereby, the interaction between the substrate and the molecules of the organic semiconductor is reduced whereas the intermolecular interaction is enlarged. This leads to an increase of the grain size of the organic semiconductor and, con-

sequently, higher charge carrier mobilities can be achieved [101, 102].

A CuPc layer deposited on an OTS-treated SiO_2 substrate (depicted schematically in fig. 5.1(b)) while the substrate was kept at room temperature is depicted in fig. 5.1(d). Again, round shaped grains can be observed but the grain size is increased significantly compared to (c). A typical lateral grain diameter of $80 - 90\,\text{nm}$ can be determined. Thus, the average crystallite size is by a factor of 3.6 larger than in the case of bare SiO_2. This leads to the assumption that the charge carrier transport parallel to the substrate will be enhanced. On the other hand, the RMS roughness increases compared to the growth on SiO_2: $R_{\text{RMS}} = 2.0\,\text{nm}$ on OTS. However, this is not supposed to be a problem for the performance of OFETs since the charge carrier transport is limited to the first few nanometers of the organic semiconductor layer. Hence, OTS is a suitable surface treatment to enlarge the size of the semiconductor crystallites.

Another way to increase the crystallinity is to heat the substrate during deposition of the organic semiconductor [103]. An elevated substrate temperature increases the mean free path of the adsorbed semiconductor molecules on the substrate. Hence, the molecules are more mobile and can accumulate in larger crystallites. An AFM image of 25 nm CuPc on OTS-treated SiO_2 grown at a substrate temperature of $T_{\text{sub}} = 100°\text{C}$ is displayed in fig. 5.1(e). The crystallinity is significantly increased and worm-like crystallites with typical lateral dimensions of $150 \times 50\,\text{nm}^2$ are formed with an RMS roughness of $R_{\text{RMS}} = 4.7\,\text{nm}$, similar to previously observed data [104].

5.1.2 XRD measurements

X-ray diffraction is used to determine the crystal structure of the layers. Therefore, 25 nm of CuPc are deposited on the respective substrate without using any shadow masks in order to maximize the reflected intensity. Θ-2Θ-scans were performed in Augsburg using Cu K_α radiation with $\lambda = 1.54\,\text{Å}$. The recorded XRD spectra are shown in fig. 5.2. The red line corresponds to a CuPc layer on OTS-treated SiO_2 with $T_{\text{sub}} = 100°\text{C}$. A clear peak at $2\Theta_{\text{max}} = 6.8 - 6.9°$ can be observed. Using the Bragg relation in eq. 4.1 with $n = 1$, a lattice spacing of $d = 12.9 - 13.0\,\text{Å}$ can be calculated, which is in agreement with $d_{(100)} = 12.0\,\text{Å}$ of α-phase CuPc found in literature [76, 77]. This proves that the crystallites in the thin film are formed by α-phase CuPc. In case of CuPc on OTS grown at room temperature, the dotted green line in fig. 5.2 is measured. There is also a pronounced peak of α-phase CuPc but the signal-to-noise ratio is significantly worse which is related to a lower crystallinity. This makes it difficult to determine a clear peak position but it seems that the peak is shifted to higher values implying a slightly reduced lattice

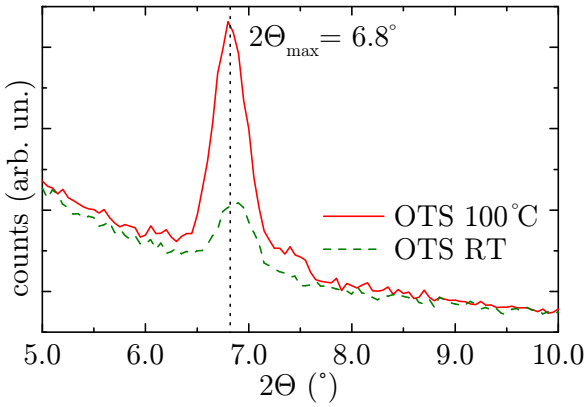


Figure 5.2: Θ-2Θ-scans of CuPc on OTS-treated SiO_2 substrates with and without elevated substrate temperature. The peak at $2\Theta_{max} = 6.8°$ corresponds to a lattice spacing of $d = 13.0\,\text{Å}$, which agrees well with α-phase CuPc.

constant. The latter can be due to a different tilting angle of the CuPc molecules in non-heated films. The signal-to-noise ratio is even worse for CuPc on bare SiO_2 (not shown here), but a reflex of α-phase CuPc is still observable.

5.2 Transistor characteristics

5.2.1 Measurements

AFM and XRD measurements reveal the polycrystallinity of the CuPc layer for all substrate treatments shown above. However, the size of the crystallites depends strongly on the treatment. CuPc on bare SiO_2 has the lowest grain size and consequently a high number of grain boundaries. Additionally, SiO_2 is known to exhibit many trap states for charge carriers, especially for electrons [105]. Thus, the performance of an OFET consisting of CuPc grown on bare SiO_2 is supposed to be limited.

Nevertheless, this OFET works well in the hole accumulation mode, as can be seen from the transfer characteristics displayed in fig. 5.3(a) and the output characteristics in fig. 5.3(b). A significant increase of the current is observable for negative gate voltages, whereas the current remains of the order of magnitude of the noise for positive gate voltages (not shown here). This proves a unipolar p-type behavior. Switch-on and threshold voltages are $V_{so} = -4\,\text{V}$ and $V_t = -14\,\text{V}$, respectively. On/off ratio and charge carrier mobility determined in the linear regime are $I_{on}/I_{off} \approx 10^4$ and $\mu_{TLM} = 2.0 \times 10^{-3}\,\text{cm}^2/\text{Vs}$. Additionally, a hysteresis between

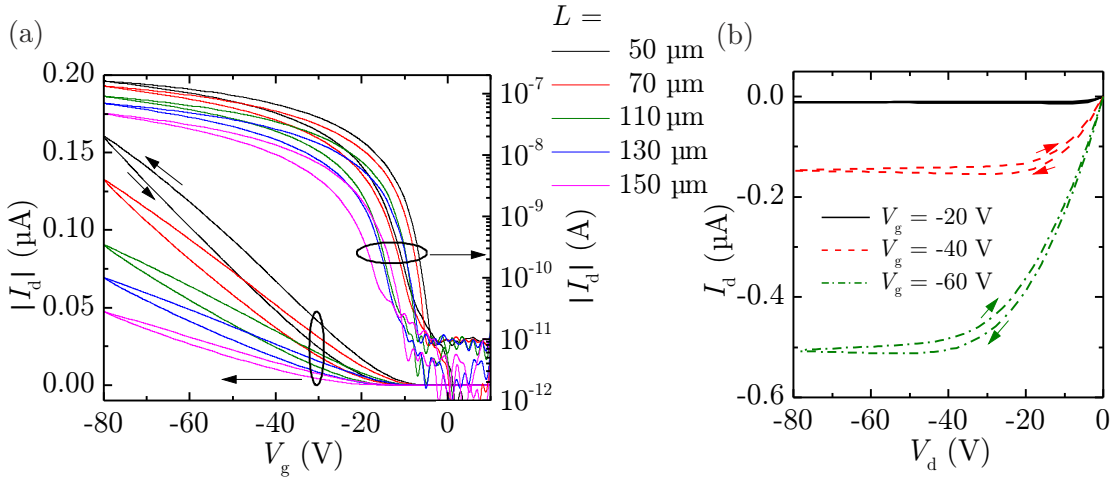


Figure 5.3: (a) Transfer characteristics in the linear regime ($V_\mathrm{d} = -2\,\mathrm{V}$) of *p*-type CuPc OFETs with bare SiO_2 substrate for various channel lengths and a channel width $W = 3.0\,\mathrm{mm}$. (b) Output characteristics of the device with $L = 130\,\mu\mathrm{m}$ shown in (a).

forward and backward scan is observable. This is a clear sign for the presence of charge carrier traps at the insulator/semiconductor interface [61]. A low off-current of the order of $I_\mathrm{off} \leq 10^{-11}\,\mathrm{A}$ underlines the high purity of the organic semiconductor.

Morphology data obtained by AFM and XRD predict an improvement of the device performance when OTS is used as substrate treatment. Indeed, this can be seen from fig. 5.4(a), where the device on bare SiO_2 discussed above is compared to CuPc OFETs fabricated on OTS-treated wafers with the substrate kept at room temperature and with $T_\mathrm{sub} = 100\,^\circ\mathrm{C}$. Both OTS-treated OFETs exhibit comparable characteristics with an on/off ratio of 4×10^4 and a linear mobility of $1.2 \times 10^{-2}\,\mathrm{cm^2/Vs}$. Thus, the on-off ratio and the hole mobility are increased by factors of four and eight, respectively. Threshold voltages are increased to $V_\mathrm{t} = -30\,\mathrm{V}$ for CuPc deposited on OTS at room temperature and $V_\mathrm{t} = -23\,\mathrm{V}$ for $T_\mathrm{sub} = 100\,^\circ\mathrm{C}$. The characteristic parameters of all different *p*-type OFETs are summarized in table 5.1. No electron transport can be observed in any of the devices.

In order to obtain a more precise evaluation of the measurement data, the TLM method is used. Fig. 5.4(b) shows the total resistance of the sample with bare SiO_2 and the OTS-treated sample with $T_\mathrm{sub} = 100\,^\circ\mathrm{C}$ as a function of the channel length. For clarity, the data of CuPc on OTS deposited at room temperature is not shown here. As described in sec. 3.1.2, the charge carrier mobility corrected by the contact

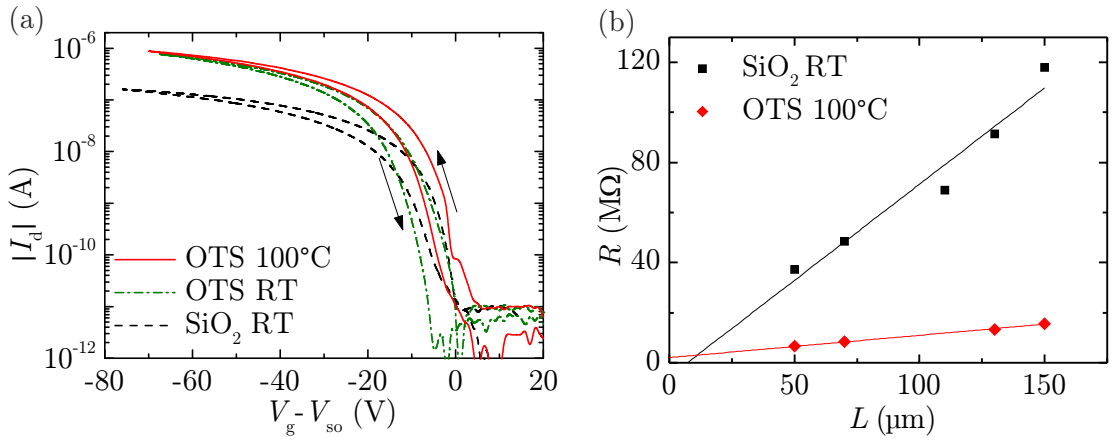


Figure 5.4: (a) Transfer characteristics of OFETs with CuPc deposited on bare and OTS-covered SiO_2 with substrate kept at room temperature and on OTS-covered SiO_2 with a substrate temperature of 100°C. The channel lengths are $L = 50\,\mu m$. The measurement is performed in the linear regime with $V_d = -2\,V$. (b) Corresponding TLM analysis curves for an effective gate voltage of $V_{eff} = -20\,V$. The lines are linear fits to determine the charge carrier mobility.

resistance can be calculated from the slope of the linear fits. They are given in table 5.1. The contact resistance cannot be calculated from the TLM data because the linear fit of the electron curve exhibits a negative y-axis offset, as depicted in fig. 5.4(b). To avoid this problem it would be necessary to have more channel lengths available, especially for smaller values of L. Consequently the single-curve analysis described by Horowitz *et al.* is used [54]. Charge carrier mobility μ_{sc} and contact resistance as a function of effective gate voltage determined by single-curve analysis are displayed in fig. 5.5(a) and (b), respectively. The corresponding values for μ_{sc} and R_c are listed in table 5.1.

5.2.2 Discussion

On bare SiO_2, stable hole transport with pronounced linear and saturation regimes can be achieved with hole mobilities in the range of $\mu = 2.0 \times 10^{-3}\,cm^2/Vs$. This is a comparable value to data found in literature for CuPc on SiO_2 deposited at room temperature [80]. The mobility increases by approximately one order of magnitude when OTS-treated SiO_2 is used as substrate. An increase is already expected from AFM and XRD measurements and can be attributed to the higher crystallinity of the CuPc layer deposited on OTS. However, OTS is not suitable to passivate the

substrate	μ_{lin} ($\mathrm{cm}^2/\mathrm{Vs}$)	μ_{TLM} ($\mathrm{cm}^2/\mathrm{Vs}$)	μ_{sc} ($\mathrm{cm}^2/\mathrm{Vs}$)	$R_{\mathrm{c,sc}}$ ($\mathrm{M}\Omega$)	V_{t} (V)
bare SiO_2	2.0×10^{-3}	2.0×10^{-3}	1.8×10^{-3}	37	-14
OTS, RT	1.2×10^{-2}	1.6×10^{-2}	1.0×10^{-2}	6.0	-30
OTS, 100°C	1.2×10^{-2}	1.7×10^{-2}	1.0×10^{-2}	6.5	-23

Table 5.1: Transistor characteristics of CuPc OFETs with $L = 50\,\mu\mathrm{m}$ on bare SiO_2 and OTS-treated SiO_2 (with and without substrate heating) and Au contacts. Charge carrier mobilities for holes and electrons are determined by a simple linear fit (μ_{lin}), by TLM at $V_{\mathrm{eff}} = -20\,\mathrm{V}$ (μ_{TLM}) and by gate bias-dependent single-curve analysis at $V_{\mathrm{eff}} = -20\,\mathrm{V}$ (μ_{sc}). $R_{\mathrm{c,sc}}$ is determined by single-curve analysis at $V_{\mathrm{eff}} = -20\,\mathrm{V}$ and V_{t} by a linear fit of the transfer curves.

electron traps at the interface since no n-type characteristics are observed for any OTS-treatment. The density of the OTS layer is supposed to be not high enough to provide a closed, trap-free surface. Such high-density, crystalline SAMs are known to require Langmuir-Blodgett techniques [70].

It is remarkable that the charge carrier mobility does not improve further when the OTS-treated SiO_2 substrate is heated at 100°C during deposition of the organic semiconductor, although the grain size is further increased. Several aspects can be responsible for this behavior. On the one hand, the roughness of the CuPc layer increases when the individual crystallites are enlarged. At a certain crystallite size, it is possible that discontinuities appear which can cause "holes" in the film, as it has already been described in literature [80]. Thus, some of the transport paths become interrupted and the effective mobility levels off or even decreases.

Another effect contributing to the saturation of the mobility in the case of heated OTS can be polaronic interactions between the charge carriers in the channel and the SiO_2 substrate. It has been shown that the charge carrier mobility in organic single-crystal FETs depends strongly on the dielectric constant of the insulator [106]. This is explained by the formation of Fröhlich polarons, i.e. quasiparticles consisting of a charge carrier surrounded by a polarization cloud that moves along the channel with the charge carrier and extends into the insulator. The higher the dielectric constant of the insulator, the more difficult is it to move the polarization cloud along the interface. Hence, μ decreases with increasing ε. Experiments presented in chapter 8 show that the influence of the substrate decreases with increasing distance d between the SiO_2 substrate and the channel and vanishes at $d \approx 15\,\mathrm{nm}$, which is considerably larger than the thickness of the OTS monolayer. Thus, hole mobilities are considerably lower than values reported for CuPc single crystals, which are in the range of $0.5 - 1\,\mathrm{cm}^2/\mathrm{Vs}$ [107–109].

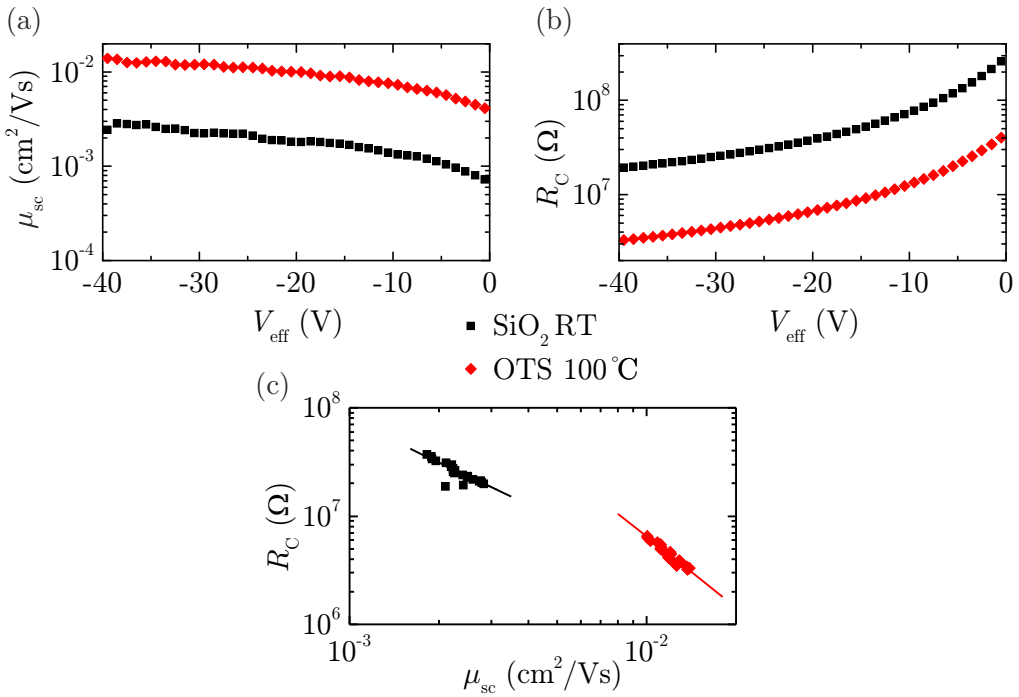


Figure 5.5: Single-curve analysis of CuPc OFETs with CuPc deposited on bare SiO_2 without substrate heating and on OTS-covered SiO_2 with substrate heating. The gate bias dependent charge carrier mobilities are given in (a) and the contact resistances in (b). (c) Correlation between charge carrier mobility and contact resistance for both devices. The data points follow the behavior $R_c \propto \mu^{-\alpha}$ with $\alpha \approx 1.3$ for SiO_2 substrate and $\alpha \approx 2.0$ for heated OTS.

It is also noticeable that all individual hole mobilities are comparable for each sample, regardless of which analysis technique is used. This demonstrates that the charge carrier transport is not limited by the contact resistance or by the injection but by the transport in the film. The fact that μ_{TLM} and μ_{sc} do not differ significantly although the contact resistance determined by TLM exhibits negative values, is a clear sign that TLM provides reliable values for the mobility and probably only a slight error in the effective channel lengths occurs. This error can be a systematic deviation of all channels due to a diffuse film edge resulting from the distance between shadow mask and substrate during the deposition of the top contacts. If the channel length of every transistor is reduced by a very small constant value, the mobility remains constant but the true contact resistance is significantly larger than the determined value.

For a further investigation, the contact resistances of both samples shown in fig. 5.5(b) are plotted as a function of the mobility on a double logarithmic scale

in fig. 5.5(c). The data points follow an exponential behavior

$$R_c \propto \mu^{-\alpha} \tag{5.1}$$

with $\alpha \approx 1.3$ for bare SiO_2 and $\alpha \approx 2.0$ for heated OTS as determined by a linear fit on a double logarithmic scale. A dependence with $\alpha = 1$ has been observed in the case of unipolar P3HT transistors or ambipolar $CuPc/C_{60}$ blends [110, 111]. This effect is called *diffusion limited injection* and means that the charge carrier mobility is the limiting factor for the contact resistance. The charge carriers cannot diffuse quickly enough away from the contact, so that the amount of injected charge carriers is limited [32, 112]. The model described by Scott *et al.* assumes that the injection current from the metal electrode into the organic semiconductor is proportional to the mobility and decreases exponentially with the Schottky barrier between the two layers. Our data shows that the injection behavior is close to diffusion limited injection for bare SiO_2 substrates but the dependence of R_c on μ is more pronounced for heated OTS substrates. Up to now, the reason for this behavior is unknown. However, it could be an indication that the increase of the mobility leads to the effect that the contact resistance is not dominated by the low mobility any more and that other parameters, like the hole injection barrier, have a stronger influence on R_c.

A problem concerning the determination of the contact resistance using the single-curve analysis is the fact that R_c is calculated with the help of μ (see eqs. 3.14 and 3.15). Hence, there is *per se* a correlation between these two parameters. In order to realize an independent analysis of R_c and μ, four point measurements would be necessary, where the current is measured independently on the applied voltage.

5.3 Summary

The growth of CuPc directly on SiO_2, on OTS-treated SiO_2 and on OTS-treated SiO_2 with substrate heating was investigated in this chapter. The morphology of the CuPc film is characterized by small round-shaped crystallites with an average diameter of ca. 50 nm on SiO_2. The grain size increases when OTS-treated SiO_2 substrates are used and grain diameters of ca. 90 nm are reached. The deposition of CuPc on OTS-treated substrates with substrate heating at 100°C results in even larger, worm-like crystallites with typical dimensions of $150 \times 50\,nm^2$. CuPc was found to crystallize in the α-phase on all of these substrate treatments.

OFETs with Au top contacts revealed stable unipolar *p*-type characteristics with hole mobilities of $\mu \approx 2.0 \times 10^{-3}\,cm^2/Vs$ on bare SiO_2 and $\mu \approx 1.2 \times 10^{-2}\,cm^2/Vs$ on OTS-treated SiO_2. This increase was attributed to the larger grain size of CuPc

on OTS. Despite the elongated grains on heated OTS-treated substrates, no further increase of the hole mobility is observed, which indicates that some morphological optimum for thin films is achieved. This assumption is supported by the data shown later in chapter 8.

Chapter 6

Ambipolar transistors with polymeric passivation layer

Up to now, only unipolar hole transport was observed in CuPc because the electron traps at the dielectric-semiconductor interface are not passivated efficiently by OTS. In order to overcome these traps, a different passivation layer is required. For this purpose, PMMA will be introduced in this chapter.

6.1 Ambipolar field-effect transistors

6.1.1 Conditions for ambipolar transport

Generally, there are three major requirements that have to be fulfilled to realize ambipolar charge carrier transport in OFETs: A trap-free dielectric surface, high purity of the organic semiconductor and low injection barriers [28, 113, 114]. As demonstrated in chapter 5, OTS has turned out to be not suitable to provide an interface that is free of electron traps in our case. In literature, there are reports of electron transport on OTS but it is known that the density of an OTS monolayer can vary drastically. Closely packed crystalline OTS layers were only achieved by Langmuir-Blodgett fabrication techniques [70]. In all other cases, the packing density of the molecules was lower. Thus, electron traps can remain on the interface. To circumvent this problem, PMMA can be used as a passivation layer. Benson *et al.* have already demonstrated that spin-cast layers of PMMA can

provide smooth, trap-free interfaces allowing for electron transport in pentacene [71].

A high purity of the organic semiconductor is crucial for ambipolar charge carrier transport since impurities or dopants can act as traps for one of the charge carrier types. Oxygen is known to perform a *p*-type doping for many organic semiconductors, which results in an enhancement of hole transport combined with a suppression of electron transport as will be shown later [27, 115]. These problems can be circumvented by using highly pure materials and avoiding exposure of the devices to ambient air.

Injection barriers at the top electrodes can hinder the injection of one of the charge carrier types. This is demonstrated schematically in fig. 6.1. Here, the energy diagram of CuPc (already introduced in fig. 4.5) is shown in relation to the work functions of two exemplary contact materials ϕ_{c1} and ϕ_{c2}. Since ϕ_{c1} is energetically comparable to the HOMO of CuPc, holes can be injected easily from contact 1, but there is a large injection barrier for electrons. On the other hand, ϕ_{c2} fits well to the LUMO, which results in good electron injection for contact 2, whereas the hole injection barrier is high. Thus, one would expect unipolar *p*-type characteristics for contact 1 and unipolar *n*-type behavior for contact 2. To realize ambipolar transport, two combinations of ϕ_{c1} and ϕ_{c2} are imaginable. One possibility is to deposit different contact materials for source and drain electrodes. Holes can be injected from contact 1 and electrons from contact 2. This technique has the advantage of low injection barriers for both charge carrier types. For example, the

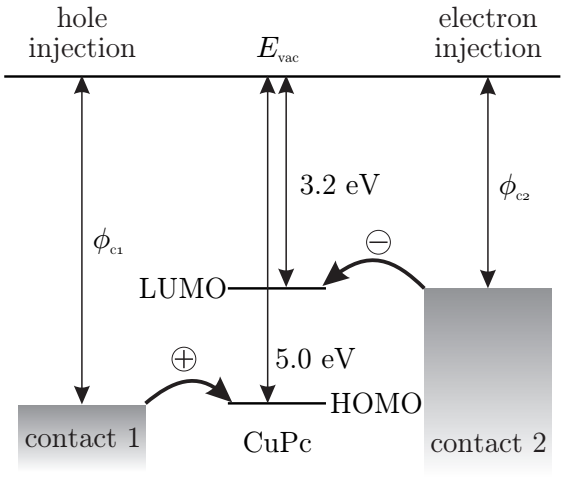


Figure 6.1: Schematic energy diagram illustrating the importance of the work function of the contacts for the injection of holes or electrons into the HOMO or LUMO of the organic semiconductor, respectively.

parallactic shadow mask displacement technique can be applied to fabricate asymmetric contacts [38]. In this case, the material sources for the different materials in an evaporation chamber are located on different places, so that each metal beam hits the sample under a different angle. However, in practice, several problems concerning the evaporation with shadow masks can occur, like diffuse contacts or even a short-circuit between source and drain. A different approach is to choose a metal with a work function ϕ_{m} located energetically between HOMO and LUMO of the organic semiconductor. Injection of both charge carrier types can be realized, even though injection barriers will be present.

As will be seen in sec. 6.2.2, electron injection is observed although the nominal work function of the metal electrode is energetically comparable to the HOMO of the semiconductor. This can be attributed to the deposition of metals (Au and Ag) as top contacts on the CuPc film. The effective work function of the metal can be changed drastically in this configuration compared to a free surface. Vacuum deposition of metals does not lead to a well defined interface between semiconductor and contact layer but can cause diffusion of metal atoms into the organic layer. Scharnberg *et al.* reported on the diffusion of Ag atoms through a diindenoperylene (DIP) layer [116]. Additionally, studying the diffusion of Au into DIP, Dürr *et al.* observed the formation of metal clusters in the organic semiconductor layer with the help of transmission electron microscopy (TEM) images [117]. The high energy of the metal atoms is also known to cause damages in the uppermost organic layers. Parthasarathy *et al.* sputtered indium tin oxide (ITO) on CuPc which resulted in the formation of midgap states that enhanced electron injection although the work function of ITO is close to the HOMO of CuPc [118]. All these effects can cause a significant reduction of the effective work function of the metal and enable electron injection, as will be shown later.

6.1.2 Realization of ambipolar OFETs

There are three different approaches for the realization of ambipolar OFETs: *single-component*, *bilayer* and *blend* OFETs. The most intuitive one is to take an organic semiconductor that is capable to transport electrons and holes and choose the metal contacts in a way that both charge carrier types can be injected, as it is described in the previous section. These devices are referred to as single-component OFETs and will be the subject of this thesis [10]. However, this is a rather recent approach to ambipolar OFETs since the high-purity organic semiconductors that are required to exhibit ambipolar characteristics could not be realized until a couple of years ago. Previously, ambipolar transistor characteristics have been obtained by bilayer or blend OFETs.

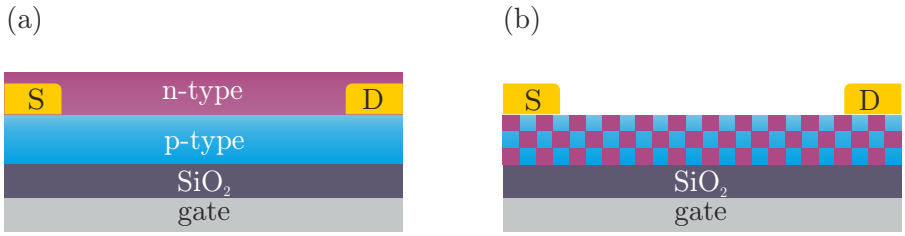


Figure 6.2: Schematic drawings of two different concepts of ambipolar transistors: (a) bilayer and (b) blend OFET.

The idea of bilayer OFETs, sometimes also referred to as *planar heterojunction* OFETs is to build a stack of a *p*- and an *n*-type organic semiconductor, as shown in fig. 6.2(a). Depending on the applied gate voltage, holes can be transported in the *p*-type semiconductor and electrons in the *n*-type semiconductor. The first ambipolar bilayer OFET has been fabricated by Dodabalapur *et al.* in 1995 with a combination of *p*-type α-6T and *n*-type C_{60} [119]. Using CuPc as *p*-type material, this technique has been applied successfully by several groups, e.g. with F_{16}CuPc as electron conductor [120]. Disadvantages of this design are lower mobilities than in unipolar OFETs built with the individual materials and sometimes the formation of a conducting layer at the interface between the two semiconductors originating from a charge transfer. This leads to high off-currents and a normally-on behavior of the transistor [121, 122].

Organic blend FETs—depicted schematically in fig. 6.2(b)—posses only one active layer which consists of a mixture of *p*- and *n*-type organic semiconductors. Thus, they are also referred to as *bulk heterojunction* FETs. For soluble organic semiconductors, the active layer can be processed from a solution containing two materials or, for non-soluble materials, by coevaporation of two molecular semiconductors. Rost *et al.* observed ambipolar field-effect characteristics even with emission of light for a blend of PTCDI-$C_{13}H_{27}$ and α-5T [11]. In these devices, charge carrier transport occurs through interpenetrating networks of *n*- and *p*-channel materials [10, 111]. This approach results in a dilution of each material and thus a decrease of the individual charge carrier mobilities.

6.1.3 Preliminary work of our group

Preliminary work on ambipolar OFETs in our group was focused on organic blend FETs based on CuPc as *p*-type semiconductor and the buckminster fullerene C_{60} as *n*-type semiconductor. These experiments were done by Markus Bronner in the course of his PhD thesis [123]. C_{60} exhibits an ionization potential of $I_p = 6.4\,\mathrm{eV}$

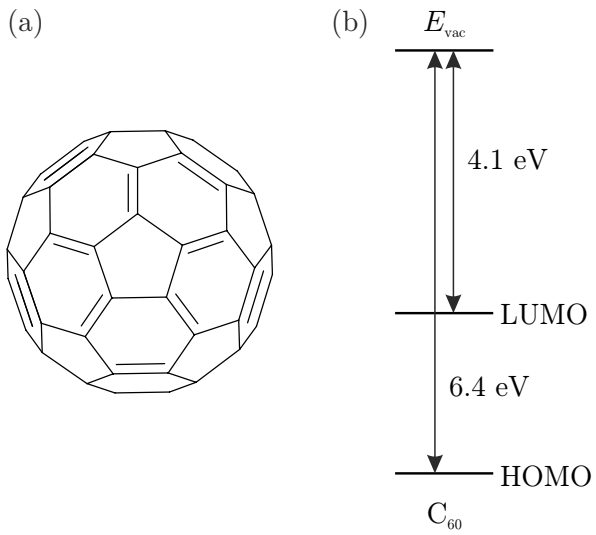


Figure 6.3: (a) Molecular structure and (b) schematic band diagram of C_{60}.

and an electron affinity of $E_A = 4.1\,\text{eV}$ [124, 125]. The molecular structure and a schematic energy diagram of C_{60} are depicted in fig. 6.3.

Because of the high values of I_p and E_A, C_{60} is a unipolar electron conductor for usual electrode materials like Ag or Au. High-mobility electron transport can be observed in C_{60} layers deposited directly on bare or OTS-treated SiO_2 not requiring any additional passivation layer [126]. This can be explained by the high electron affinity of C_{60}. It has been shown that the electron-trapping effect of hy-

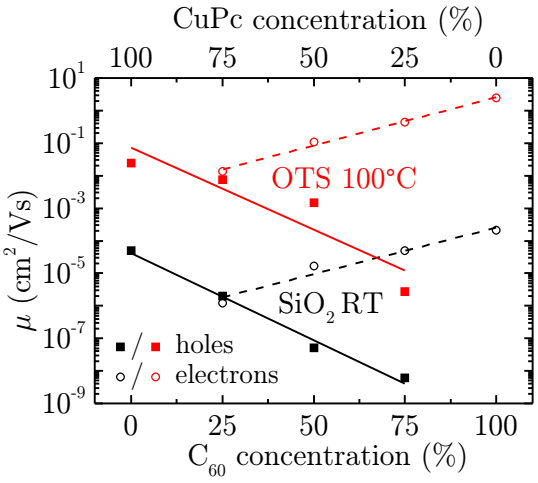


Figure 6.4: Hole and electron mobilities as a function of the mixing ratio for blend OFETs grown on bare SiO_2 at room temperature (black) and on OTS at $T_{sub} = 100\,°\text{C}$ (red). The data are replotted from ref. [123].

droxyl groups at the semiconductor-insulator interface diminishes with increasing electron affinity of the organic semiconductor [10, 127]. Unipolar hole transport with saturation mobilities of $\mu_h \approx 4 \times 10^{-5}\,cm^2/Vs$ on bare SiO_2 with $T_{sub} = RT$ and $\mu_h \approx 2 \times 10^{-2}\,cm^2/Vs$ on OTS with $T_{sub} = 100\,°C$ was observed for pure CuPc OFETs (see chapter 5). All transistors studied in conjunction with the investigation of blend OFETs were fabricated in bottom contact geometry with Au contacts structured by photolithography. Unipolar electron mobilities for neat C_{60} films were determined as $\mu_e \approx 2 \times 10^{-4}\,cm^2/Vs$ on bare SiO_2 with $T_{sub} = RT$ and $\mu_e \approx 2.4\,cm^2/Vs$ on OTS with $T_{sub} = 100\,°C$ [104, 123]. Ambipolar transport can be realized by coevaporation of CuPc and C_{60}. Each material provides transport percolation paths for the respective charge carrier type in the blend. Consequently, the charge carrier mobilities depend on the mixing ratio of the two semiconductors. Fig. 6.4 shows hole and electron mobilities (closed squares and open circles, respectively) of blend OFETs as a function of the CuPc : C_{60} mixing ratio. The black color stands for active layers deposited on bare SiO_2 at room temperature, whereas red symbolizes deposition on heated, OTS-treated substrates. The lines are linear fits of the data. The charge carrier mobilities of the neat films cannot be reached with blends because of the dilution of the charge carrier paths. As an important result, balanced electron and hole mobilities are only achieved with $\mu_h \approx \mu_e \approx 1 \times 10^{-2}\,cm^2/Vs$ at a mixing ratio of CuPc : $C_{60} = 3 : 1$ for heated substrates.

6.2 Single-component CuPc transistors with PMMA

In the preceding section, three different realizations of ambipolar OFETs have been explained: bilayer, blend and single component OFETs. As explained in sec. 6.1.2, highly-pure organic semiconductors are available nowadays and ambipolar charge carrier transport can often be realized in single layers of one material. It will be shown in the following, that ambipolar charge carrier transport is possible in polycrystalline CuPc films if a trap-free dielectric-semiconductor interface and low injection barriers are provided.

6.2.1 Morphology

AFM measurements

A smooth dielectric-semiconductor interface is important to guarantee an unhindered charge carrier transport along the channel in an OFET [128]. For this reason, the morphology of the spin-cast PMMA passivation layers is analyzed by AFM. Fig. 6.5(a) shows an AFM image of 18 nm PMMA on SiO_2. PMMA forms a very smooth surface with $R_{RMS} = 0.25$ nm without any substructure as usually found for amorphous polymers. Thereupon, 25 nm of CuPc are deposited while the substrate is kept at room temperature. The corresponding AFM data are given in fig. 6.5(b). As already observed for bare and OTS-treated SiO_2 substrates in chapter 5, a clearly polycrystalline CuPc film is formed. An average grain diameter of 50 nm and a roughness of $R_{RMS} = 1.4$ nm can be determined. These parameters are almost identical to the growth of CuPc on bare SiO_2. Substrate heating during deposition of CuPc is not possible since the PMMA passivation layer will be destroyed at elevated temperatures. Although the glass-transition temperature of PMMA is known to be between 100°C and 120°C, even samples heated at lower temperatures do not show reasonable transistor characteristics. A possible reason for this can be a significantly lower glass transition temperature of PMMA in the case of thin films.

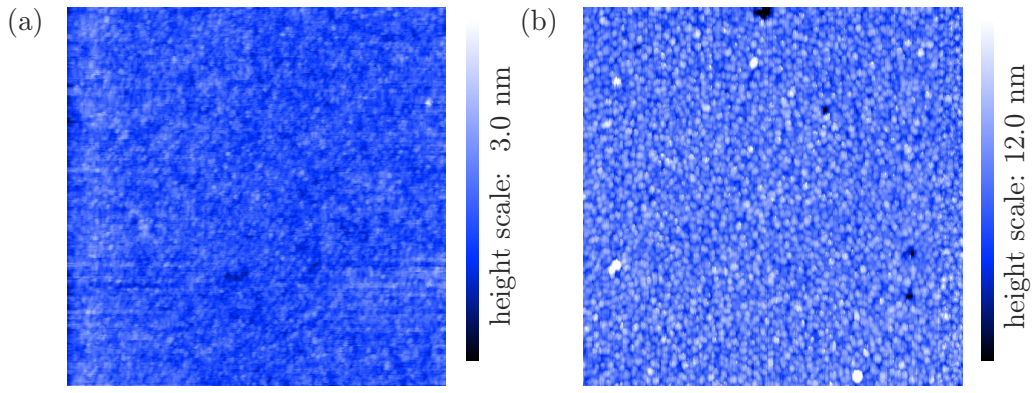


Figure 6.5: AFM images of a spin-cast layer of 18 nm PMMA on SiO_2 (a) and of 25 nm of CuPc on the PMMA passivation layer (b). Both images are $2 \times 2\,\mu m^2$ in size.

XRD measurements

AFM images suggest that the morphology of CuPc on PMMA is identical to that on bare SiO_2. This assumption is confirmed by XRD measurements shown in fig. 6.6. The α-phase of CuPc is detected with relatively low intensity resulting from small crystallites comparable to bare SiO_2.

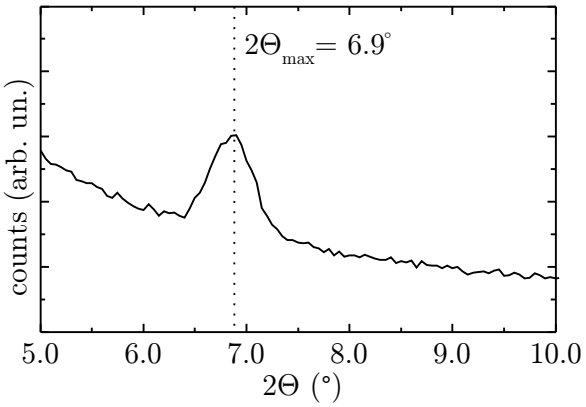


Figure 6.6: Θ-2Θ-scan of CuPc on PMMA-coated SiO_2 substrates. The peak at $2\Theta_{max} = 6.9°$ corresponds to a lattice spacing of $d = 12.8\,\text{Å}$ which belongs to α-phase CuPc.

6.2.2 Ambipolar characteristics

Measurements

Fig. 6.7 shows output characteristics of a CuPc OFET on PMMA-passivated SiO_2 with Au top electrodes. The hole transport regime is displayed in fig. 6.7(a), whereas the electron transport regime in fig. 6.7(b). Clearly ambipolar characteristics with negligible hysteresis are observed. These facts prove that PMMA provides a surface that is free of electron traps. The OFET exhibits well pronounced linear, saturation and ambipolar regimes. Due to the large difference of hole and electron threshold voltage, the ambipolar electron injection is hardly observable in the hole transport output curves. Only a very small current increase can be seen for $V_g = -20\,\text{V}$ and $V_d < -70\,\text{V}$ (black curve). Transfer characteristics of five OFETs on the same substrate with channel lengths ranging from $L = 80\,\mu\text{m}$ to $L = 160\,\mu\text{m}$ are measured to determine the TLM-charge carrier mobilities of the sample. The corresponding transfer curves in the linear regime can be seen in fig. 6.7(c) for the hole transport regime ($V_d = -10\,\text{V}$) and in fig. 6.7(d) for the electron transport

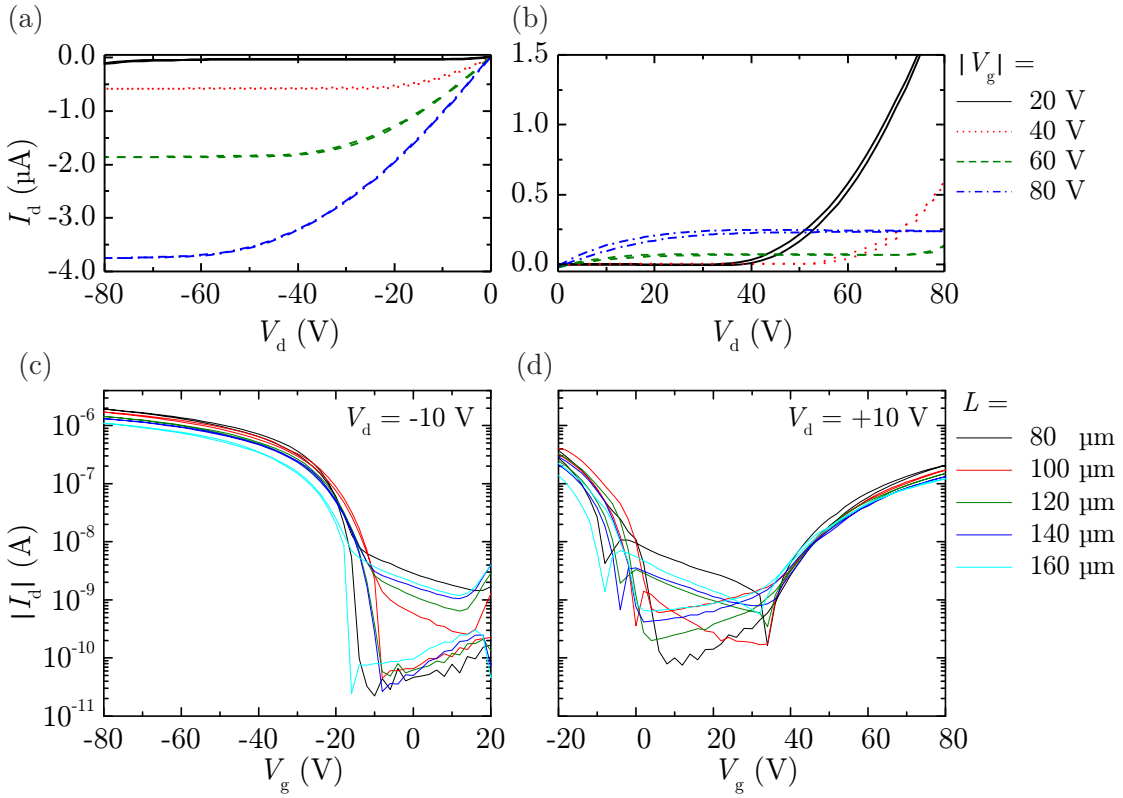


Figure 6.7: (a) and (b) Output characteristics of an OFET with 25 nm CuPc on PMMA-passivated SiO_2, a channel length of $L = 160\,\mu m$ and a channel width of $W = 10\,mm$. The hole transport regime is shown in (a), the electron transport regime in (b). (c) and (d) Transfer characteristics of OFETs with different channel lengths on the same substrate. The hole transport regime is shown in (c), the electron transport regime in (d).

regime ($V_d = +10\,V$). All transistors on PMMA exhibit stable ambipolar characteristics with an on/off ratio of approximately 2×10^4. For the TLM analysis, the total resistance as a function of L is displayed in fig. 6.8. The data for hole transport ($V_{eff} = -20\,V$) is represented by the closed squares, whereas the open circles stand for electron transport ($V_{eff} = +20\,V$). The lines are linear fits of the data to determine charge carrier mobilities μ_{TLM}. Again, TLM analysis yields negative values for the contact resistance R_c. Hence, R_c is evaluated by single-curve analysis. Charge carrier mobility μ_{sc} and contact resistance as a function of effective gate voltage determined by single-curve analysis are displayed in fig. 6.9(a) and (b), respectively. The corresponding values for μ_{lin}, μ_{TLM}, μ_{sc}, $R_{c,sc}$ and V_t are displayed in table 6.1. μ_{lin} denotes the charge carrier mobility determined by a linear fit of the transfer curve of an OFET with $L = 160\,\mu m$.

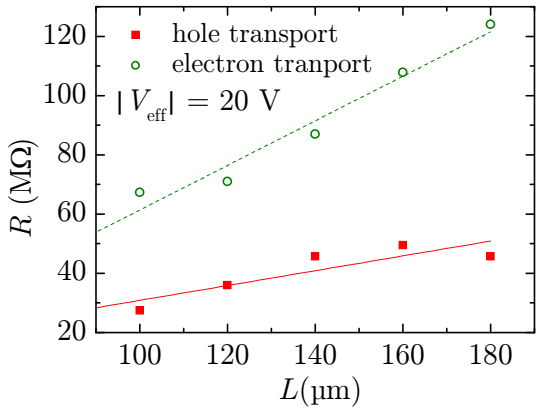


Figure 6.8: TLM analysis at $|V_{\text{eff}}| = 20\,\text{V}$ of the data displayed in fig. 6.7(c) and (d) for holes (red squares) and electrons (green circles). The lines are linear fits of the data to determine the charge carrier mobility and the contact resistance.

Discussion

It can be seen from table 6.1 that the hole mobility in CuPc on PMMA is slightly higher than on bare SiO_2 but not as high as on OTS. The reason for this is the better crystallinity of CuPc on OTS than on PMMA, as demonstrated by AFM and XRD measurements. PMMA works well as a passivation layer for electron traps, which is expressed by stable electron transport and low hysteresis. Both mobilities determined by the different methods are comparable: $\mu_{\text{h}} \approx 2 \times 10^{-3}\,\text{cm}^2/\text{Vs}$ and $\mu_{\text{e}} \approx 5 \times 10^{-4}\,\text{cm}^2/\text{Vs}$. However, the electron mobilities are approximately by a factor of four lower than the hole mobilities. The fact that the linear and the contact-corrected values do not differ drastically demonstrates that charge carrier injection is not the limiting factor for charge carrier transport. It will be shown

	μ_{lin} (cm^2/Vs)	μ_{TLM} (cm^2/Vs)	μ_{sc} (cm^2/Vs)	$R_{\text{c,sc}}$ (MΩ)	V_{t} (V)
holes	2.7×10^{-3}	1.5×10^{-3}	2.0×10^{-3}	50	−22
electrons	5.7×10^{-4}	5.7×10^{-4}	4.9×10^{-4}	96	+52

Table 6.1: Transistor characteristics of a CuPc OFET with $L = 160\,\mu\text{m}$ on PMMA-passivated SiO_2 with Au contacts. Charge carrier mobilities for holes and electrons are determined by a simple linear fit (μ_{lin}), by TLM at $V_{\text{eff}} = \pm 20\,\text{V}$ (μ_{TLM}) and by gate bias-dependent single-curve analysis at $V_{\text{eff}} = \pm 20\,\text{V}$ (μ_{sc}). $R_{\text{c,sc}}$ is determined by single-curve analyis at $V_{\text{eff}} = \pm 20\,\text{V}$ and V_{t} by a linear fit of the transfer curve.

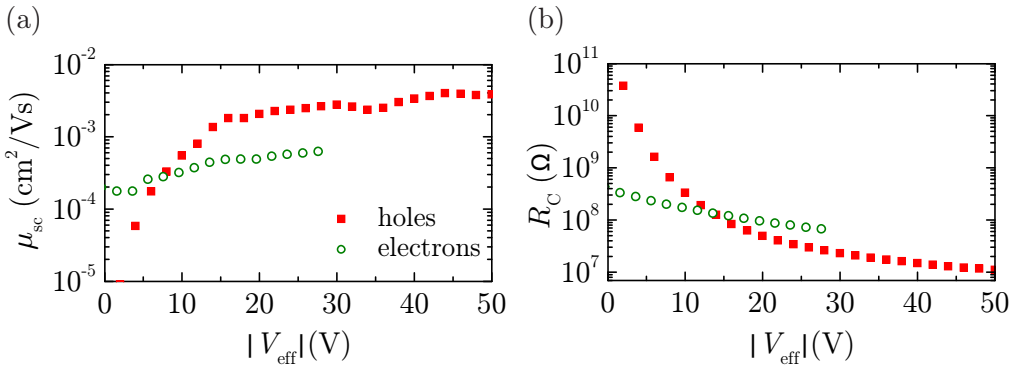


Figure 6.9: Single-curve analysis of a CuPc OFET with $L = 160\,\mu m$ on PMMA-passivated SiO_2 with Au contacts. The gate bias dependent charge carrier mobilities are given in (a) and the contact resistances in (b).

later that the morphology of the CuPc film limits the performance.

The results of the single-curve analysis given in fig. 6.9 demonstrate that there is only a weak dependence of charge carrier mobility on gate bias. Only a small increase is observable, which is in good agreement with the expectations for polycrystalline molecular organic semiconductors, as already discussed in sec. 3.1.3.

As it is explained in sec. 6.1.1, the effective work function of the Au electrodes is reduced due to top contacts and electron injection is enabled although the nominal work function of Au is around 5.1 eV, which is almost equivalent to the HOMO of CuPc [49]. It has to be investigated if the asymmetry between hole and electron mobility is an intrinsic property of the CuPc layer or if it is caused by poor electron injection properties of the Au contact due to the energetic mismatch. This will be done in the following section.

6.2.3 Control of charge carrier type by contact modification

Measurements

A straight-forward method to investigate the charge carrier injection of electrons and holes is to use various electrode materials differing with respect to their work function ϕ_m. Since Au, although it exhibits one of the highest work functions of all metals, can inject holes and electrons into the active CuPc layer, it is likely that other metals with lower work function will enhance electron injection, but unipolar hole transport is not supposed to be feasible for CuPc with metal top contacts.

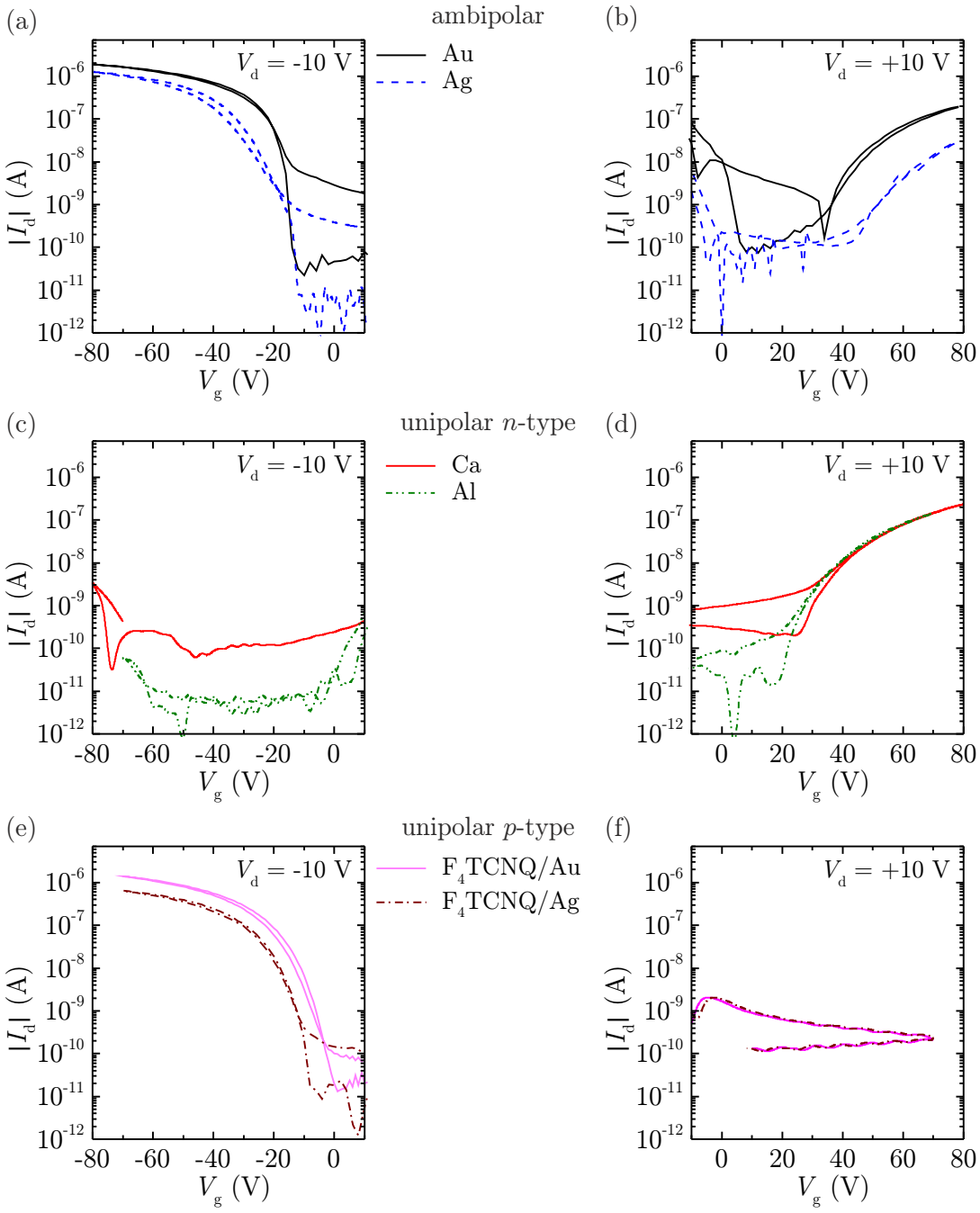


Figure 6.10: Transfer characteristics of CuPc OFETs on PMMA-passivated SiO_2 wafers with $L = 100\,\mu m$ and $W = 10\,mm$ for various electrode materials. Ambipolar devices are shown in (a) and (b), unipolar n-type OFETs in (c) and (d) and unipolar p-type devices in (e) and (f).

Indeed, this assumption is confirmed by measurements on PMMA-passivated CuPc OFETs shown in fig. 6.10 for Au, Ag, Ca and Al top contacts. All devices are identical except for the top contact material. Only Au and Ag electrodes, shown in (a) and (b), provide injection of both holes and electrons, whereas OFETs with Al and Ca contacts, depicted in (c) and (d), show unipolar *n*-type behavior. A small current increase can be observed in the hole transport regime of Ca and Al electrodes for large gate voltages (fig. 6.10(c)). This is a sign for a weak hole injection. However, the hole currents are of the order of magnitude of the leakage current and the OFETs can be considered as unipolar *n*-type, consequently. The charge carrier mobilities of all devices as well as the work function of the metal electrodes are listed in table 6.2. ϕ_{m} is determined by Kelvin probe measurements performed on the free surface of metals prepared under the same conditions [72]. Thus, these values can only be taken as approximate values and can differ significantly from the effective work function of the top contact, as already explained in sec. 6.1.1. With all above-mentioned metal electrodes, it is not possible to achieve unipolar *p*-type characteristics. However, this would be crucial for the realization of complementary inverter structures on one single substrate. Conventional metals cannot be used for this purpose, since only Pt exhibits a higher work function than Au with $\phi_{\mathrm{Pt}} = 5.65\,\mathrm{eV}$ [49]. However, Pt cannot be evaporated by resistive heating but only by electron beam evaporation or sputtering due to its high melting point: $T_{\mathrm{melt,Pt}} \approx 1770°\mathrm{C}$ vs. $T_{\mathrm{melt,Au}} \approx 1064°\mathrm{C}$. In these techniques, the sample is exposed to very high temperatures that would cause serious damages to the CuPc and PMMA layers. Consequently, an alternative material for the realization of a high-work function electrode has to be used. In our case, hybrid electrodes consisting of a combination of a thin layer ($\approx 1-2\,\mathrm{nm}$) of the strong organic acceptor F_4TCNQ and 50 nm Au or Ag are used (see also sec. 4.2.1). The resulting transfer characteristics are shown in fig. 6.10(e) and (f), demonstrating the successful realization of hole-only devices.

Single-curve analysis is used to determine the gate bias dependence of the charge carrier mobility and the contact resistance for the devices with Au, Ca, Al and F_4TCNQ/Au and F_4TCNQ/Ag contacts. The results are plotted in fig. 6.11(a)-(d).

Discussion

Table 6.2 provides an overview of all used contact materials, the respective work functions, charge carrier mobilities determined by TLM and contact resistances determined by gate voltage dependent single-curve analysis. The behavior of CuPc OFETs on PMMA with Au contacts has already been discussed in sec. 6.2.2. Ag,

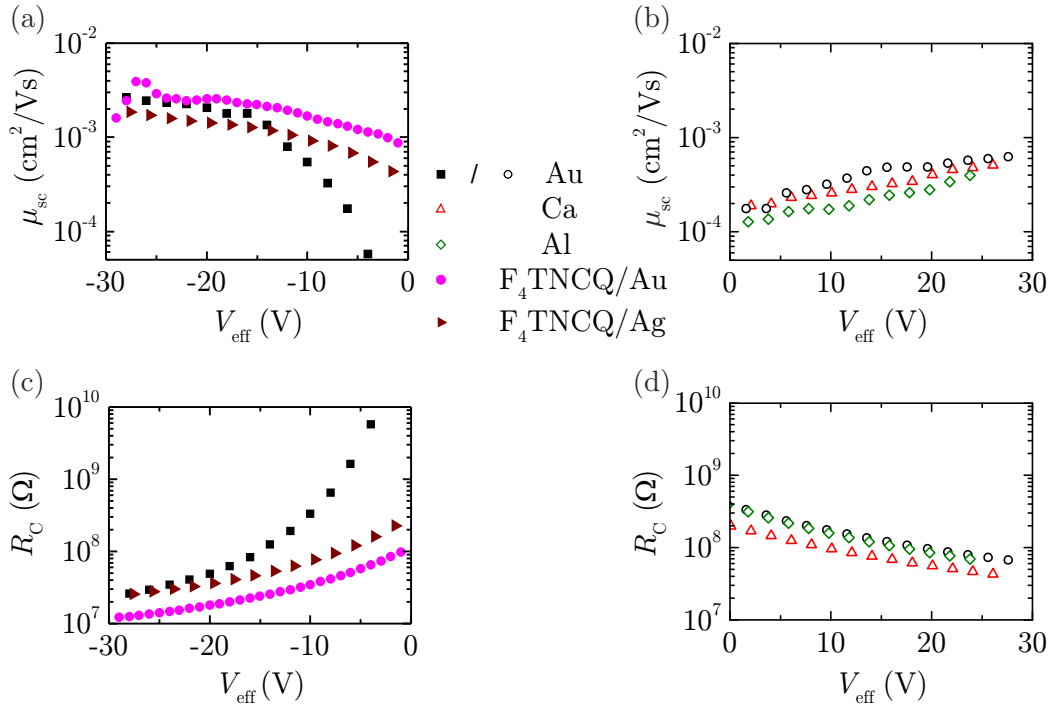


Figure 6.11: Single-curve analysis of CuPc OFETs on PMMA-passivated SiO_2 wafers with $L = 100\,\mu m$ and $W = 10\,mm$ for various electrode materials. The charge carrier mobility is given in (a) and (b) and the contact resistance in (c) and (d). Closed symbols stand for hole transport shown in (a) and (c), whereas open symbols stand for electron transport, shown in (b) and (d).

which exhibits a slightly lower work function is also able to inject both holes and electrons. Ca and Al can only inject electrons since their Fermi levels are significantly lower and fit well to the CuPc LUMO. Thus, the expected correlation between ϕ_m and the charge carrier injection behavior of the metal electrodes is confirmed. Concerning the hole-only injecting properties of F_4TCNQ/Au and F_4TCNQ/Ag contacts, several aspects have to be considered. On the one hand, the work function of the hybrid electrodes is even higher than that for Au, as determined by Kelvin probe measurements. This enhances the injection of holes into the CuPc HOMO. On the other hand, it has been discussed in the preceding sections that the effective value of ϕ_m can be drastically lowered in top contact configurations due to the formation of metal clusters or damages by the metal atoms. In this case, it is possible that the thin F_4TCNQ interlayer can act as a protection layer for the underlying CuPc and prevent the diffusion of metal atoms into the CuPc layer. This effect could avoid clusters and damages in the active material and thus result in a better alignment of the work function of the electrode

contact material	ϕ_m (eV)	$\mu_{h,TLM}$ (cm^2/Vs)	$\mu_{e,TLM}$ (cm^2/Vs)	$R_{c,h}$ (MΩ)	$R_{c,e}$ (MΩ)
Au	5.0	1.5×10^{-3}	5.7×10^{-4}	50	96
Ag	4.9	2.0×10^{-3}	2.0×10^{-4}	—	—
Al	3.6	—	4.0×10^{-4}	—	85
Ca	3.3	—	7.6×10^{-4}	—	56
F_4TCNQ/Au	5.6	3.5×10^{-3}	—	18	—
F_4TCNQ/Ag	5.3	2.0×10^{-3}	—	36	—

Table 6.2: Transistor characteristics of CuPc OFETs with $L = 100\,\mu m$ and $W = 10\,mm$ on PMMA-passivated SiO_2 for various metal top contacts. The work function of the electrodes ϕ_m is determined by Kelvin probe measurements [72]. Charge carrier mobilities for holes μ_h and electrons μ_e are determined by TLM at $V_{eff} = \pm 20\,V$. The contact resistance R_c is determined by single-curve analysis at $V_{eff} = \pm 20\,V$.

and the HOMO of CuPc. F_4TCNQ is also used as *p*-dopant or hole injecting layer because of its strong electron-accepting properties, e.g. in OLEDs [96]. Regardless of which effect is predominant, the effective work functions of F_4TCNQ/Au and F_4TCNQ/Ag contacts are larger than the corresponding values of the neat metals, which leads to the suppression of electron injection.

These results can be compared with the DFT calculations discussed in sec. 2.3. The calculations predicted electron and hole injection into CuPc from Au contacts but only electron injection from Ca contacts, which is confirmed by our experiments.

Comparing the respective charge carrier mobilities, all hole mobilities are of the order of $10^{-3}\,cm^2/Vs$, whereas all electron mobilities are of the order of $10^{-4}\,cm^2/Vs$. It has to be mentioned that deviations by a factor of two can occur from one sample to another. Taking this into account, it can be stated that hole and electron mobilities are independent of the electrode material and, consequently, can be considered to be intrinsic properties of the CuPc films with the given morphology.

The contact resistance of hole injection is significantly lower than that for electron injection. This observation reveals that the energetic mismatch between Fermi level and HOMO or LUMO cannot be the only factor contributing to R_c because Ca exhibits a higher contact resistance for electrons than Au or Ag for holes although ϕ_{Ca} is comparable to the LUMO of CuPc. In order to investigate the correlation between contact resistance and charge carrier mobility, the different values for R_c and μ from table 6.2 are plotted in fig. 6.12. The data points follow the equation

$$R_c \propto \mu^{-\alpha} \tag{6.1}$$

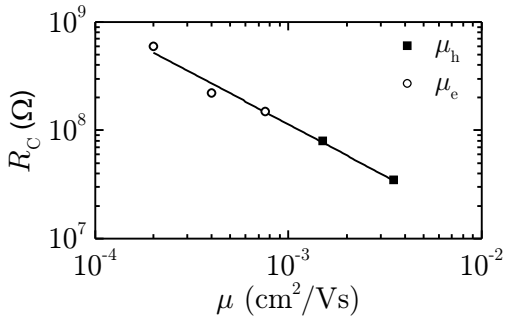


Figure 6.12: Correlation between charge carrier mobility and contact resistance for electron and hole transport in CuPc on PMMA. The data points taken from table 6.2 follow the behavior $R_c \propto \mu^{-0.95}$. This almost reciprocal dependence of R_c on μ corresponds to diffusion limited injection.

with $\alpha = 0.95$ in this case. Thus, the charge carrier injection can be considered as diffusion limited, as described in sec. 5.2. α is similar to the case of unipolar hole transport on bare SiO_2, where a comparable CuPc grain size is determined. However, there are two factors interacting in this case: the variation of the Schottky barrier height ϕ_b due to different metal electrodes and the variation of μ, which is assumed to be only of minor significance from one sample to another. The model developed by Scott *et al.* assumes that the injection current from the metal electrode into the organic semiconductor is proportional to the mobility and decreases exponentially with the Schottky barrier between the two layers [112]. Thus, it is difficult to apply this model since the origin of the variation of R_c can be either of the two factors.

The sample with F_4TCNQ/Au contacts exhibits by far the highest hole mobility and the lowest contact resistance. Principally, it would be imaginable that F_4TCNQ reduces the contact resistance, which implies an increase of μ. However, this is not supposed to be the case in the CuPc OFETs presented here, as will be shown later with the help of organic metal top contacts, where R_c is decreased significantly, but μ remains constant. Hence, a doping of the CuPc film by F_4TCNQ is likely since the F_4TCNQ layer is unstructured and covers the CuPc completely. F_4TCNQ molecules can diffuse through the CuPc layer and act as *p*-type dopants which enhances the conductivity. Since mobility and contact resistance are strongly correlated, R_c is reduced by this effect. Similar results with clearly reduced contact resistances were also reported for F_4TCNQ/Au top contacts on *p*-type pentacene OFETs [97]. This might also be an explanation for the slightly reduced switch-on voltage of F_4TCNQ-covered OFETs, which has also been reported in literature [129].

6.2.4 Influence of oxygen doping

As mentioned before in this chapter, the exposure of ambipolar OFETs to ambient air leads to oxygen doping of the active material. Oxygen is known to be a *p*-type dopant for most organic semiconductors and can thus enhance hole transport but suppress electron transport [27, 115]. The effect of oxygen doping on an ambipolar CuPc OFET on PMMA with Au contacts can be seen in fig. 6.13. The hole transport regime is shown in (a), the electron regime in (b) for the device directly measured after fabrication (black lines) and after a storage in ambient air for three months (red lines). The threshold voltage for hole transport is shifted from $V_{\mathrm{t,h}} = -21\,\mathrm{V}$ for the as-fabricated device to $V_{\mathrm{t,h}} = -12\,\mathrm{V}$ after exposure to air. The hole mobility determined in the linear regime increases from $\mu_{\mathrm{h}} = 1.8\times10^{-3}\,\mathrm{cm^2/Vs}$ to $\mu_{\mathrm{h}} = 2.5\times10^{-3}\,\mathrm{cm^2/Vs}$. However, electron transport completely vanishes after storage in ambient air. The shift of $V_{\mathrm{t,h}}$ can be attributed to an increased hole density due to *p*-type doping of the organic semiconductor. This effect has also been observed for oxygen-doped nickel-phthalocyanine films [130]. The oxygen molecules act as electron acceptors which leads to a suppression of *n*-channel operation, as already described for a variety of different ambipolar transistor materials [115].

In the following, the process of oxygen doping is further investigated. For this purpose, an ambipolar CuPc transistor with Au contacts is fabricated and the transfer characteristics are measured as usually in high vacuum ($p \approx 10^{-6}\,\mathrm{mbar}$) in the cryostat. Afterwards, a valve is opened which allows for the insertion of ambient air into the cryostat. Thus, a pressure of $10^{-3}\,\mathrm{mbar}$ is adjusted and the

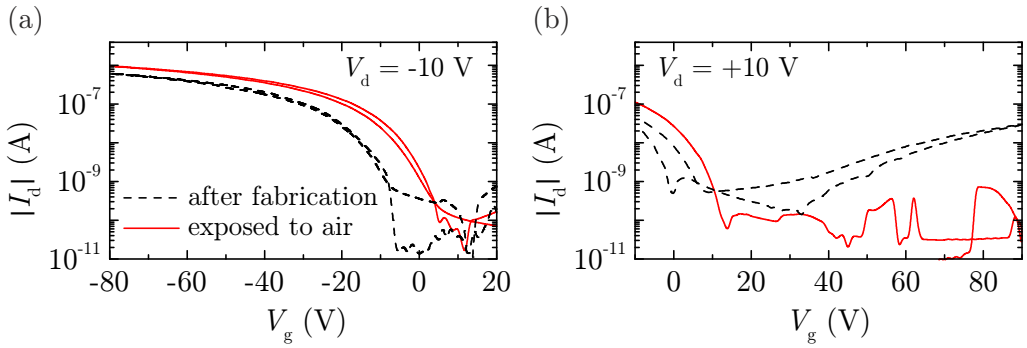


Figure 6.13: Influence of exposure to air on the performance of CuPc OFETs. The graphs show transfer characteristics of an ambipolar CuPc OFET on PMMA-passivated SiO_2 wafers with $L = 180\,\mu\mathrm{m}$, $W = 10\,\mathrm{mm}$ and top Au contacts directly after fabrication (black lines) and after storage in ambient air for three months (red lines). (a) Hole transport is enhanced by oxygen doping, (b) electron transport is suppressed.

transistor is measured again immediately after flooding and after waiting times of 6, 18 and 36 h. This procedure enables the observation of a very slow doping process due to the reduced oxygen concentration compared to ambient conditions. It has to be mentioned that this particular device exhibits higher initial charge carrier mobilities than the devices discussed above due to its surface passivation layer of TTC, which will be introduced in the next chapter. However, at the moment, no further explanations are necessary since only the development of the charge carrier mobilities and the threshold voltages will be discussed.

Fig. 6.14 illustrates the process of slow oxygen doping for the charge carrier mobilities (a) and the threshold voltages (b) of holes (red squares) and electrons (green circles). The observed data is in good agreement with the effect discussed above. Hole mobility is slightly increased, whereas electron mobility is decreased [131]. Both threshold voltages are shifted to more positive values. As a summary, it can be stated that oxygen doping is no instantaneous effect but a rather slow process, where *p*-channel operation is enhanced continuously, whereas *n*-channel operation is suppressed simultaneously. Scheinert *et al.* have developed a correlation between the shift of the threshold voltage ΔV_t and the bulk doping of the organic semiconductor [61]. One obtains

$$\Delta V_\mathrm{t} = \frac{e \cdot N \cdot d_\mathrm{s}}{C'} \tag{6.2}$$

with the dopant concentration per unit volume N, the thickness of the semiconductor $d_\mathrm{s} = 25\,\mathrm{nm}$ and the capacitance of the gate insulator per unit area

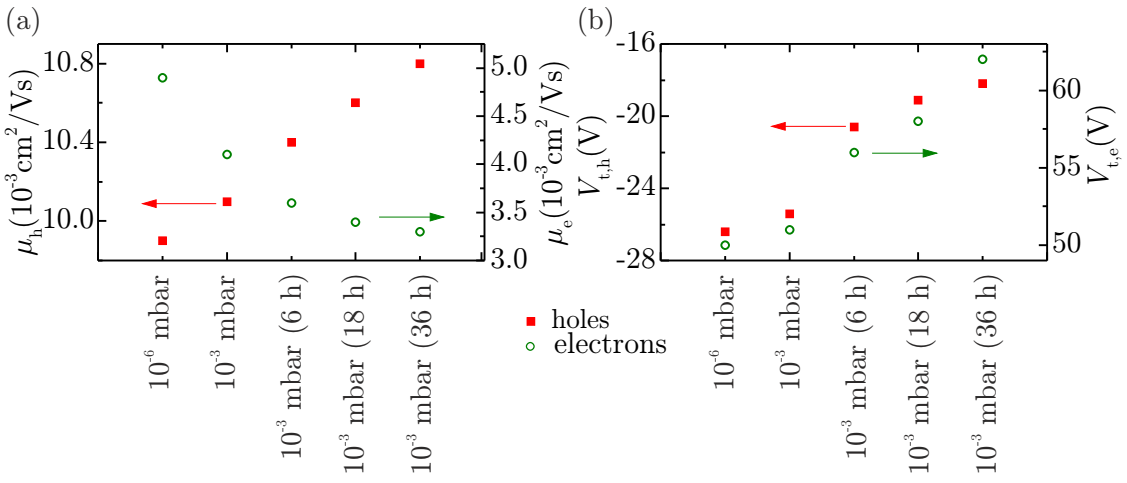


Figure 6.14: Effects of oxygen doping due to a storage of an ambipolar CuPc OFET in air at a pressure of 10^{-3} mbar. Charge carrier mobilities are plotted in (a) and threshold voltages in (b) [131].

$C' = 1.0 \times 10^{-4}\,\mathrm{F/m^2}$. After 36 hours of exposure to oxygen, the total shift of the hole threshold voltage has reached $\Delta V_{\mathrm{t,h}} = 8.2\,\mathrm{V}$. Hence, one calculates a concentration of p-dopants of $N = 2.1 \times 10^{17}\,\mathrm{cm^{-3}}$. This value is of the same order of magnitude as doping concentrations calculated by MIS measurements in chapter 9 and as data shown in literature [61].

From the experiments discussed above it can clearly be seen that CuPc does not degrade upon exposure to air but is only p-doped. Organic semiconductors behave differently when brought in contact with oxygen and moisture. Generally, n-type OFET devices are much more sensitive to atmosphere because oxygen can act as radical anion in organic materials [132]. The situation is more manifold for hole transport. In most cases, the effects of doping are most visible in the subthreshold region because energetic states are appearing within the band gap which leads to an increase of conductivity. Thus, a large positive shift of V_{t} is observable [21, 133]. "Normally-off" devices are often turned into "normally-on" so that positive gate bias is required to deplete the channel as reported for polymer OFETs with P3MT [134]. This situation is very similar to CuPc in our case. However, other molecular materials are known to degrade upon exposure to air. Pannemann *et al.* present a systematic degradation study of p-type pentacene OFETs, which have been stored in dark ambient conditions for nine months. Here, the hole mobility decreased from $2 \times 10^{-3}\,\mathrm{cm^2/Vs}$ for as-prepared devices to $1.2 \times 10^{-5}\,\mathrm{cm^2/Vs}$ after storage [135]. In contrast to the cases described above, V_{t} is shifted towards more negative values. Thus, hole transport in pentacene is steadily suppressed. The reason why some organic semiconductors—like CuPc or DIP—are air-stable, whereas other materials like pentacene or rubrene are air-sensitive is the polyaromatic hydrocarbon structure of many unstable organic semiconductors. There are numerous reports in literature that describe the tendency of these polyaromatics to oxygenize, e.g. due to the formation of pentacenequinone in the case of pentacene [114, 136, 137].

6.3 Summary

In this chapter, it was shown that ambipolar charge carrier transport can be achieved in CuPc OFETs when the SiO_2 gate dielectric is passivated by a spin-cast layer of PMMA. CuPc films are polycrystalline with a grain size similar to the growth on bare SiO_2. Au and Ag electrodes turned out to enable injection of both electrons and holes, whereas devices with Al and Ca electrodes exhibit unipolar n-type characteristics. The experimental data confirms the prediction obtained by DFT calculations. Unipolar p-type transistors can be real-

ized with hybrid electrodes consisting of a thin layer (approximately 1 nm) of F_4TCNQ covered by 50 nm Au. Regardless of the electrode material, all hole mobilities are about $\mu_h \approx 2 \times 10^{-3}\,cm^2/Vs$, whereas all electron mobilities are about $\mu_e \approx 5 \times 10^{-4}\,cm^2/Vs$. Hence, there is a significant asymmetry between hole and electron transport that does not depend on the electrode material and can thus be considered as an intrinsic property of the CuPc film with the given morphology. The contact resistance is found to be strongly correlated to the charge carrier mobility with the dependence $R_c \propto \mu^{-1}$, which is a sign for diffusion limited injection.

CuPc does not degrade when exposed to ambient air but is *p*-doped by oxygen which leads to a suppression of electron transport whereas hole transport is stabilized. This is in contrast to other molecular materials like pentacene but similar to some polymer materials like P3MT.

The problem of all devices presented in this chapter is the poor crystallinity of the CuPc layer affiliated with low charge carrier mobilities. In the case of unipolar transistors on OTS, the CuPc grain size can be increased by substrate heating. This is not possible with PMMA due to the thermal instability of PMMA.

Chapter 7

Ambipolar transistors with aliphatic TTC passivation layer

In the present chapter, the long-chain alkane molecule tetratetracontane ($C_{44}H_{90}$, TTC) will be introduced as alternative organic passivation layer instead of PMMA. In contrast to amorphous PMMA, TTC grows in a highly crystalline way, which can promote a more ordered growth of CuPc. TTC has already been known as a chemically stable insulator for a long time. The growth of TTC on various metal substrates has been described by Seki *et al.* in 1986 [138]. Ogawa *et al.* demonstrated that TTC is suitable as passivation layer for OFETs with pentacene as active material [74]. However, hole mobility turned out to be significantly lower than without TTC due to smaller pentacene grains on TTC than on SiO_2. In the following, it will be demonstrated that TTC is suitable as passivation layer for CuPc and the resulting field-effect mobilities are significantly higher than those on PMMA.

7.1 Morphology

7.1.1 Morphology of TTC passivation layers

AFM measurements

TTC passivation layers are deposited on clean SiO_2 as described in sec. 4.2.1. In order to analyze the growth mechanism of TTC on SiO_2, various TTC thicknesses are deposited. The corresponding AFM images are shown in fig. 7.1 for TTC layers between 2 nm and 12 nm. It has to be noted that the numbers indicate a "nominal" TTC thickness obtained from the deposited amount on the quartz monitor during evaporation. Because of the inhomogeneous growth of TTC, the actual thickness might deviate, as will be discussed in the following.

The growth of TTC can be distinguished in three different growth regimes [139]. Regime I represents the sub-monolayer range, i.e. nominal thicknesses between 2 and 4 nm of TTC (fig. 7.1(a) and (b)) and describes the growth of TTC islands on SiO_2. These islands are not connected to each other. The height profile along the red line in fig. 7.1(a) is displayed in fig. 7.2(a). It can be concluded that the flat terraces of constant height consist of a monolayer of TTC molecules standing upright on the SiO_2 surface because the length of a TTC molecule is approximately 6 nm [140, 141] and the lattice spacing is $d = 5.86$ nm as shown by XRD measurements in the subsequent section. The formation of a second layer can already be seen on some islands.

Regime II represents nominal TTC thicknesses between one and about two monolayers (fig. 7.1(c) and (d)), where the TTC islands grow until the underlying SiO_2 is completely (or almost completely) covered and additional TTC layers are formed. As can be seen from the height profile of the 6 nm sample displayed in fig. 7.2(b), the terraces are still flat but some high TTC columns are appearing in between. The columns can reach up to 60 nm. Thus, the growth mechanism of TTC on SiO_2 can be described by a Stranski-Krastanov scenario. This is a widely observed growth mode of thin films, also referred to as *layer-plus-island growth*. It is an intermediate process between a full two-dimensional *layer-by-layer growth* (Frank-van der Merwe growth) and a three-dimensional *island growth* (Volmer-Weber growth). The Stranski-Krastanov growth is determined by two different growth processes: first, a layer-by-layer growth is dominant up to a critical thickness which depends on the interaction between substrate and adsorbate. Subsequently, for higher thicknesses, the nucleation of adsorbate islands takes place which form the columns in our case.

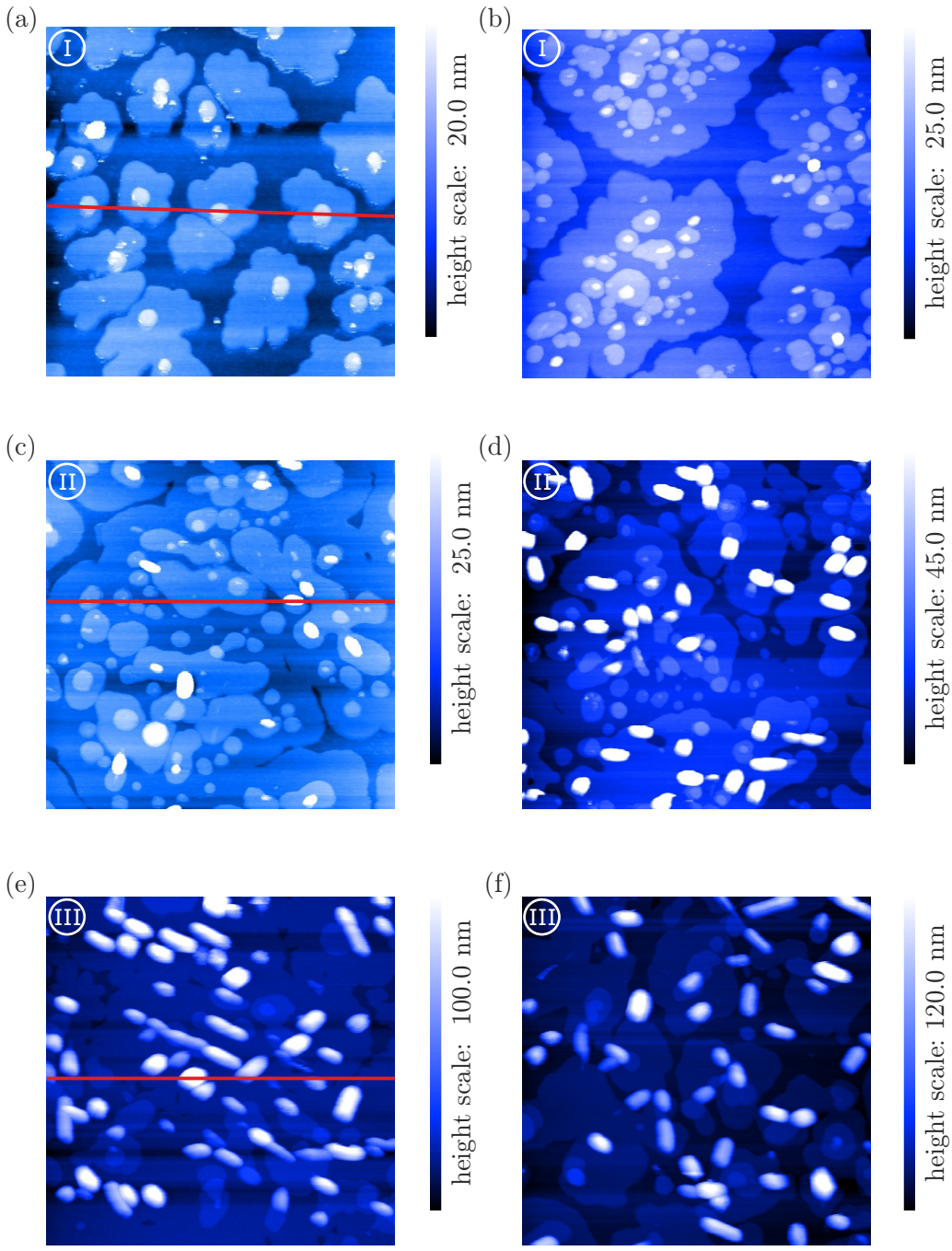


Figure 7.1: AFM images of nominally (a) 2 nm, (b) 4 nm, (c) 6 nm, (d) 8 nm, (e) 10 nm and (f) 12 nm TTC on SiO_2. Regime I ((a) and (b)) corresponds to the sub-monolayer regime, regime II ((b) and (c)) to a closed surface with some TTC columns appearing and regime III ((d) and (e)) to the domination of high columns. All images are $5 \times 5\,\mu m^2$. The numbers in circles represent the growth regimes I, II and III [139].

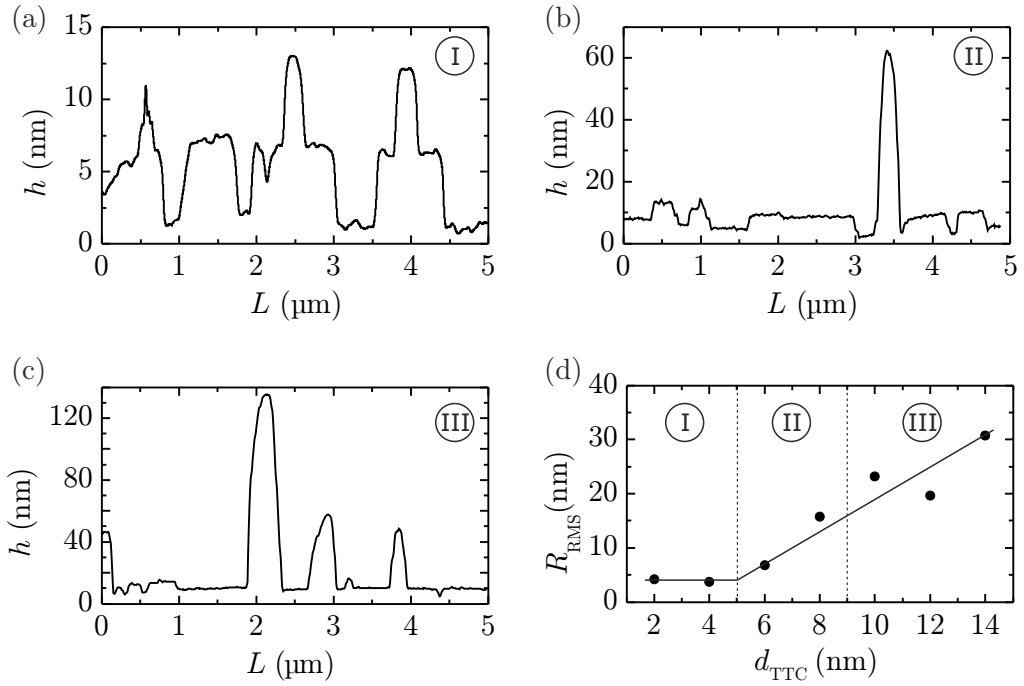


Figure 7.2: Height profiles of 2 nm TTC (a), 6 nm TTC (b) and 10 nm TTC (c) on SiO_2 along the red lines in fig 7.1. (d) RMS roughness as a function of the TTC layer thickness, the line is a guide to the eye [142]. The numbers in circles represent the growth regimes I, II and III.

In regime III, i.e. TTC layers beyond two monolayers, very high columns appear. An AFM profile of the 10 nm sample is displayed in fig. 7.2(c). Although the initial flat terraces are still visible, the number and height of the columns increase steadily. They can already reach up to 140 nm for nominal 10 nm of TTC. For TTC thicknesses larger than 14 nm, the height and the density of the columns and thus the roughness of the sample is too high to obtain analyzable AFM images.

Fig. 7.2(d) depicts the RMS roughness of a series of TTC thicknesses between 2 nm and 14 nm. Whereas it is constant in regime I, which is characterized by layer-by-layer growth, the roughness increases continuously with increasing TTC thickness as soon as island growth begins [142].

XRD measurements

With the help of XRD analysis, it can be investigated if the TTC layers are crystalline and if the lattice spacing corresponds to the length of the molecule as suggested by the AFM data. XRD measurements of TTC and of CuPc on TTC have

been performed by Alexander Hinderhofer from the group of Prof. Frank Schreiber at the University of Tübingen.

Fig. 7.3(a) shows a Θ-2Θ-scan of nominal 20 nm TTC deposited on cleaned SiO_2 (black line). A very clear crystalline spectrum can be observed with Bragg peaks up to the ninth order. The first Bragg peak is located at $2\Theta_{(100)} = 1.48°$. To minimize errors, the lattice spacing is calculated from $2\Theta_{(500)} = 7.54°$, which corresponds to a distance between two lattice planes parallel to the substrate of $d = 5.86$ nm. This parameter can be compared to data from literature: TTC crystallizes in an orthorhombic phase, where the TTC molecules are standing upright without any tilting on the substrate [140]. The distance between two

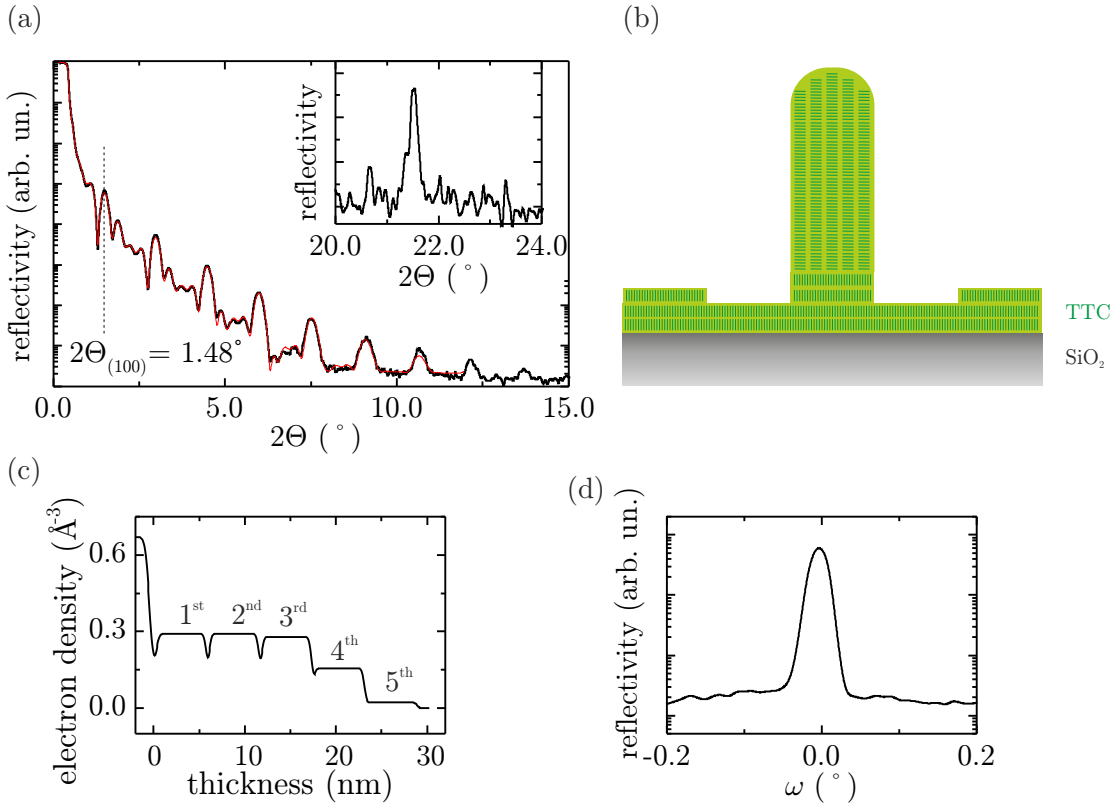


Figure 7.3: (a) Θ-2Θ-scan of nominal 20 nm TTC deposited on cleaned SiO_2 (black line). TTC forms crystalline layers with a layer spacing of $d = 5.86$ nm. Inset: Θ-2Θ-scan of in the range of an additional Bragg peak that corresponds to flat-lying TTC molecules resulting from the high columns. (b) Schematic sketch of the growth of TTC on SiO_2. The red line in (a) is a fit with the Parrat-formalism used for the extraction of the electron density profile of the first to fifth monolayer shown in (c). (d) Rocking scan of the first Bragg reflex to determine the mosaicity of the TTC layer.

neighboring molecules parallel to the substrate is $a_O = 7.5\,\text{Å}$ in this phase. The inset of fig. 7.3(a) depicts data of the same Θ-2Θ-scan for an angular range of $20° \leq 2\Theta \leq 24°$, where an additional peak is observable at $2\Theta = 21.51°$. This peak can be attributed to flat-lying TTC molecules, which are, as will be shown later, concentrated in the high columns appearing at larger TTC thicknesses. Assuming that this peak is a first-order Bragg reflex, one obtains a lattice spacing of $d' = 4.1\,\text{Å}$, which is in good agreement with the molecular distance $a_T = 4.27\,\text{Å}$ of the triclinic phase T [140]. It is also possible that this reflex is already the second order of a peak at $2\Theta = 10.76°$, which would not be visible because of an overlap with the (700) peak of upright-standing TTC. In this case, the molecular distance of the flat-lying molecules would be $d' = 8.2\,\text{Å}$, which would agree with the monoclinic phase M with $a_M = 8.02\,\text{Å}$. However, this cannot be clarified since the XRD data does not allow for a discrimination of these two cases. Fig. 7.3(b) depicts a schematic sketch of the growth of TTC on SiO_2.

The red line in fig. 7.3(a) is a fit of the data with the Parrat-formalism using the MOTOFIT analysis software [143, 144]. This technique allows for the extraction of the electron density as a function of the distance from the substrate surface. In our case, the fit of the Θ-2Θ scan agrees well with the measured spectrum and the resulting electron density profile is shown in (c) [75]. In the case of nominally 20 nm TTC on SiO_2, the shape of the electron density profile reflects the layer-by-layer growth of the first TTC layers. Each plateau can be attributed to a TTC monolayer. The first three monolayers are completely filled, whereas the fourth monolayer is only partially filled and the fifth is almost empty. The high columns cannot be seen in this graph since they form a different crystal phase.

Fig. 7.3(d) depicts the rocking scan of the first Bragg peak, which exhibits a mosaicity of FWHM $\leq 0.03°$. This demonstrates that the average tilt angle of the crystallites is very low.

7.1.2 Growth of CuPc on TTC

In contrast to PMMA, TTC does not provide a smooth, unstructured surface, but its morphology depends strongly on the deposited thickness. When used as a passivation layer in field-effect transistors, the growth of CuPc and thus the transistor characteristics are supposed to be affected by this dependence. Additionally, the influence of the almost 6 nm high terraces of TTC on the charge carrier flow has to be investigated.

AFM measurements

Since charge carrier transport takes place in the first couple of nanometers of the organic semiconductor layer, it is useful to investigate the growth of CuPc on TTC with the help of very thin CuPc films. Thus, only 5 nm of CuPc are deposited on a TTC layer in the sub-monolayer regime. Figs. 7.4(a) and (b) depict the corresponding AFM images for $5 \times 5\,\mu m^2$ (a) and $2 \times 2\,\mu m^2$ (b). Smooth, flat TTC islands are clearly observable. CuPc forms a closed, polycrystalline layer on top of these terraces. In contrast to PMMA-passivated substrates, where the crystallites are round-shaped with a diameter of $40 - 50\,nm$, elongated grains with typical lateral dimensions of $100 \times 40\,nm^2$ are observed on the first TTC monolayer. This morphology looks similar to the situation on heated OTS-treated substrates and can probably be attributed to the hydrophobic character of TTC which reduces the interaction between the CuPc molecules and the surface and leads to a higher diffusion of the CuPc molecules.

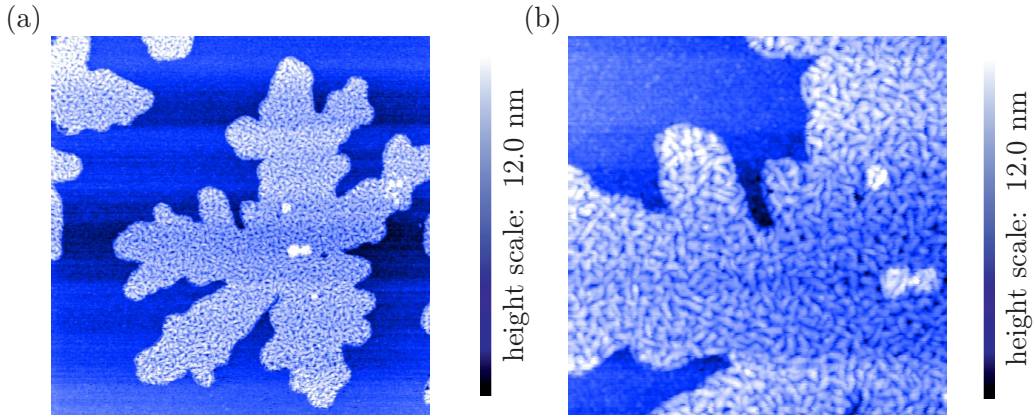


Figure 7.4: AFM images of 5 nm CuPc on a sub-monolayer TTC film. The size is $5 \times 5\,\mu m^2$ for (a) and $2 \times 2\,\mu m^2$ for (b).

XRD measurements

Fig. 7.5(a) shows Θ-2Θ-scans of 25 nm CuPc deposited on top of nominally 5.5 nm TTC (dashed line) and on nominally 20 nm TTC (solid line). Several CuPc reflexes are superimposed to the TTC spectrum already discussed in the preceding section. Typical α-phase (100)- and (200)-peaks of CuPc are distinguishable at $2\Theta^{\alpha}_{(100)} = 6.85°$ and $2\Theta^{\alpha}_{(200)} = 13.7°$. Thus, CuPc crystallizes in the α-configuration with a lattice spacing of $d_{\alpha} = 12.9\,Å$. This phase is also formed on bare and OTS-treated SiO_2 and on PMMA. A rocking scan of the (100)-peak of the sample

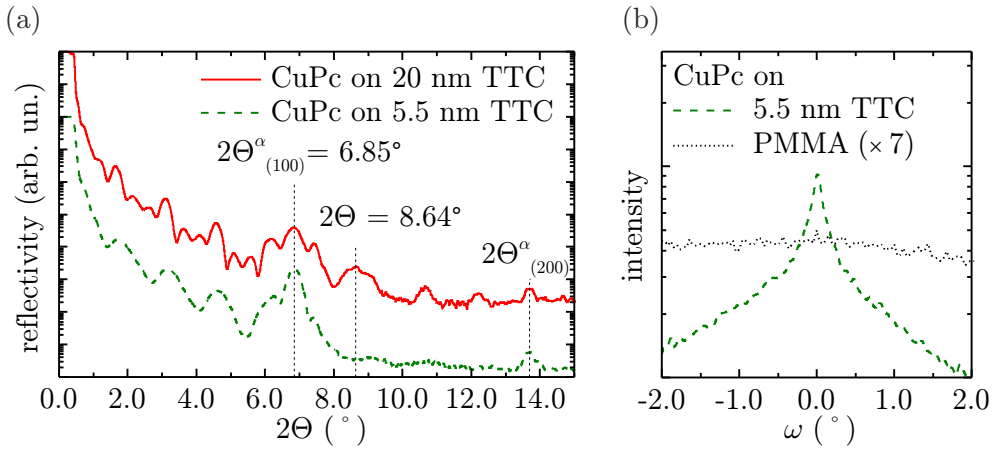


Figure 7.5: (a) Θ-2Θ-scans of 25 nm CuPc deposited on top of nominally 5.5 nm TTC and on nominally 20 nm TTC. The Bragg reflex at 6.85° is the (100)-reflex of α-phase CuPc, the peak at 8.64° cannot be assigned to a common CuPc phase. (b) Rocking scans of the CuPc-(100)-peak of the specimen with 5.5 nm TTC and, for comparison, of CuPc on PMMA multiplied by a factor of 7.

with 5.5 nm TTC is displayed in fig. 7.5(b) (solid line). The FWHM of this peak is approximately 0.26°. For comparison, the dotted line shows the rocking scan of the (100)-reflex of CuPc on PMMA shown in fig. 6.6 multiplied by a factor of 7. The FWHM is larger than 2°. This demonstrates that the average tilt angle of the CuPc crystallites perpendicular to the substrate is considerably lower on TTC than on PMMA. Thus, it can be stated that CuPc on TTC does not only form larger crystallites than on PMMA but TTC causes additionally a better horizontal alignment of the crystallites.

In addition to the expected CuPc α-reflexes, a further peak appears at $2\Theta = 8.64°$ only in the spectrum of the sample with 20 nm TTC. Using the Bragg relation, this peak corresponds to a lattice spacing of $d = 10.2\,\text{Å}$. This reflex cannot be attributed to a known CuPc polymorph, because the lattice spacing of the β-phase given in literature is $d_\beta = 7.3\,\text{Å}$ and all other phases are generally believed to occur only in powder [76, 145]. The roughness of the TTC films hinders a more detailed investigation of the given CuPc films. This will be done in the next chapter, where annealed TTC layers are discussed.

7.2 Transistor characteristics

7.2.1 Comparison to PMMA as passivation layer

Measurements

Fig. 7.6 shows output characteristics of a device with a TTC passivation layer of nominally 8 nm, an active layer of 25 nm CuPc and Au top contacts. The hole transport regime is displayed in (a), the electron transport regime in (b). Clear ambipolar characteristics with well defined linear, saturation and ambipolar regimes are observed. Hysteresis are negligibly small.

In fig. 7.7, transfer curves of this sample (red) and of a specimen with an identical geometry but with PMMA passivation layer (black) are displayed. The corresponding data for the threshold voltages, charge carrier mobilities and contact resistances determined by TLM are given in tabular 7.1.

Discussion

The nominal thickness of the TTC passivation layer of the presented device is 8 nm. This corresponds to growth regime II as discussed in sec. 7.1.2. The ambipolar characteristics clearly confirm that the SiO_2 substrate is fully covered by TTC and the electron traps are passivated. Comparing the transistor characteristics of devices with PMMA and TTC as passivation layer given in fig. 7.7 and table 7.1, it is obvious that the OFET with TTC-passivated substrate exhibits a significantly

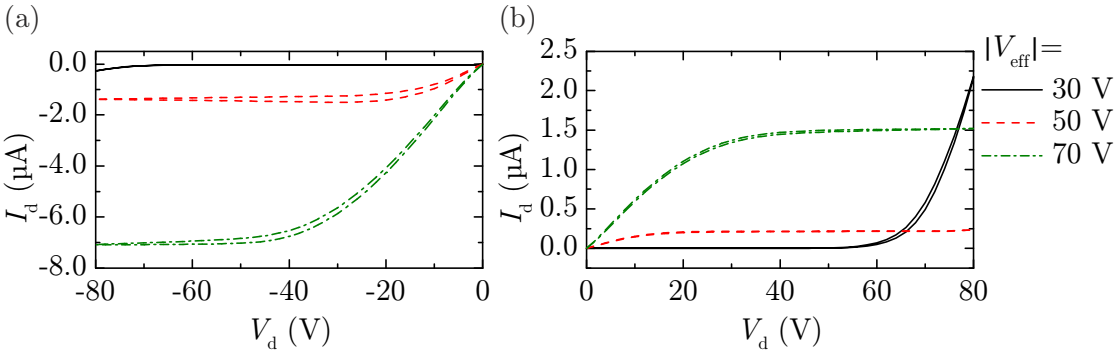


Figure 7.6: Output characteristics of a transistor with a passivation layer of nominally 8 nm TTC, 25 nm CuPc and Au contacts. The transistor geometries are $L = 50\,\mu m$ and $W = 3.0\,mm$. The hole transport regime is displayed in (a), the electron transport regime in (b).

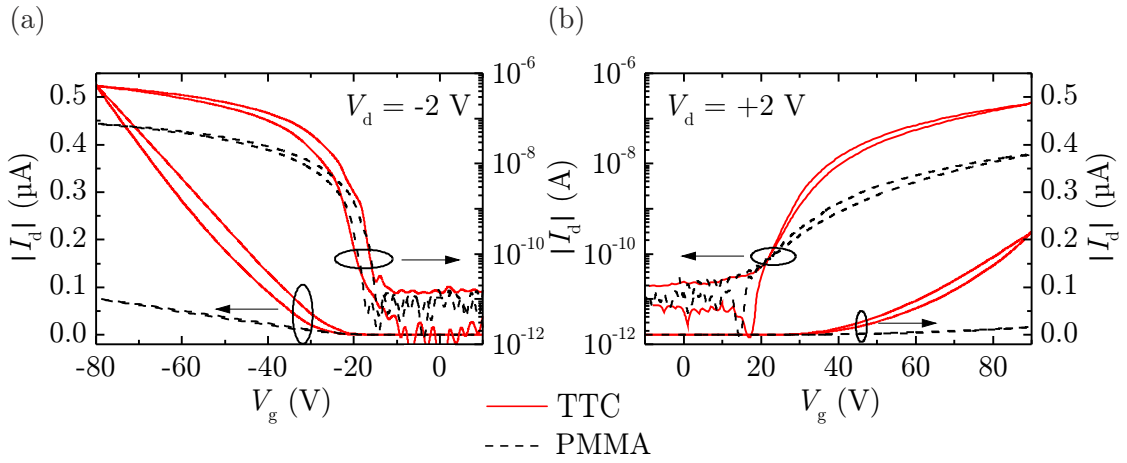


Figure 7.7: Transfer characteristics of the device with 8 nm TTC as passivation layer from fig. 7.6 and a comparable OFET with PMMA passivation layer. The hole transport regime is displayed in (a), the electron transport regime in (b).

improved device performance with an increase in electron mobility by more than one order of magnitude and an increase in hole mobility by almost one order of magnitude. These improvements are in good agreement with the increased grain size of the CuPc crystallites deposited on TTC compared to PMMA. The hole mobility is in the same range as on OTS-treated substrates, where a comparable grain size is observed. Thus, the better crystallinity of CuPc on TTC is reflected directly in higher charge carrier mobilities. Threshold and switch-on voltages are almost identical for the devices with TTC and PMMA since Au contacts are used in both cases. Additionally, the switch-on voltages of electron and hole transport are comparable ($|V_{so}| \approx 20\,V$), but the threshold voltages for electron transport are drastically larger than those for hole transport. This is an indication for the presence of electron traps which cause a strong curvature of the transfer curve close to V_t. As will be discussed in sec. 10.2, these traps are supposed to be located at the grain boundaries.

passivation layer	$V_{so,h}$ (V)	$V_{so,e}$ (V)	$V_{t,h}$ (V)	$V_{t,e}$ (V)	μ_h (cm^2/Vs)	μ_e (cm^2/Vs)	$R_{c,h}$ (MΩ)	$R_{c,e}$ (MΩ)
8 nm TTC	-18	+19	−27	+48	1.3×10^{-2}	7.4×10^{-3}	4.8	7.4
PMMA	-18	+19	−21	+50	2.3×10^{-3}	5.8×10^{-4}	44	79

Table 7.1: Comparison of transistor characteristics of CuPc OFETs with nominally 8 nm TTC and PMMA as passivation layer. Charge carrier mobilities and contact resistances are determined by TLM at $|V_{eff}| = 20\,V$.

Another effect contributing to the improved mobilities on TTC can be the lower dielectric constant of TTC compared to PMMA. In our case, we determined $\varepsilon_{\mathrm{TTC}} = 2.5$ and $\varepsilon_{\mathrm{PMMA}} = 3.6$ from capacitance measurements. As discussed in chapter 5.2, the charge carrier mobility in organic single-crystal FETs depends strongly on the dielectric constant of the insulator due to the formation of Fröhlich polarons, i.e. polarization clouds in the insulator [106]. A high polarizability of the insulator hinders a fast movement of these polarons along the channel. Similar results have been obtained for charge carrier transport in P3HT on various gate dielectrics [37].

7.2.2 Influence of the TTC thickness on the device performance

Measurements

As already known from the AFM measurements discussed in sec. 7.1.2, the morphology of the TTC layer depends strongly on the deposited thickness and can be divided into three growth regimes. Consequently, it is crucial to investigate the influence of these morphological changes on the device performance. Fig. 7.8 depicts transfer characteristics in the linear regime of a series of transistors with CuPc as active layer and Au top contacts. All devices are identical except for the thickness of the TTC passivation layer. The investigated thickness series ranges from $d_{\mathrm{TTC}} = 0\,\mathrm{nm}$ (i.e. bare SiO_2) to $d_{\mathrm{TTC}} = 22\,\mathrm{nm}$ in steps of 2 nm. For clarity, only a selection of relevant thicknesses are shown in the graph. TLM analysis is performed to determine charge carrier mobilities and contact resistances. Electron and hole mobilities are plotted as a function of nominal TTC thickness in fig. 7.9 [139]. The lines are guides for the eye and demonstrate the general trend. Three distinct transport regimes can be distinguished for both charge carrier types, denoted as I, II and III in the graph. The error bars represent typical variations between nominally identical samples.

Initially, there is the sub-monolayer regime I for TTC thicknesses below 5 nm. Here, the hole mobility increases with increasing TTC thickness from typically $\mu_{\mathrm{h}} \approx 2 \times 10^{-3}\,\mathrm{cm^2/Vs}$ on bare SiO_2 to $\mu_{\mathrm{h}} \approx 5.5 \times 10^{-3}\,\mathrm{cm^2/Vs}$ for $d_{\mathrm{TTC}} = 4\,\mathrm{nm}$. For this thickness, electron transport begins with a low mobility that is approximately two orders of magnitude lower than the hole mobility: $\mu_{\mathrm{e}} = 3 \times 10^{-5}\,\mathrm{cm^2/Vs}$.

In regime II, i.e. for TTC thicknesses from about one monolayer to less than three monolayers, stable ambipolar transport is observed with a plateau region for both charge carrier mobilities with $\mu_{\mathrm{h}} \approx 1 - 2 \times 10^{-2}\,\mathrm{cm^2/Vs}$ for hole transport

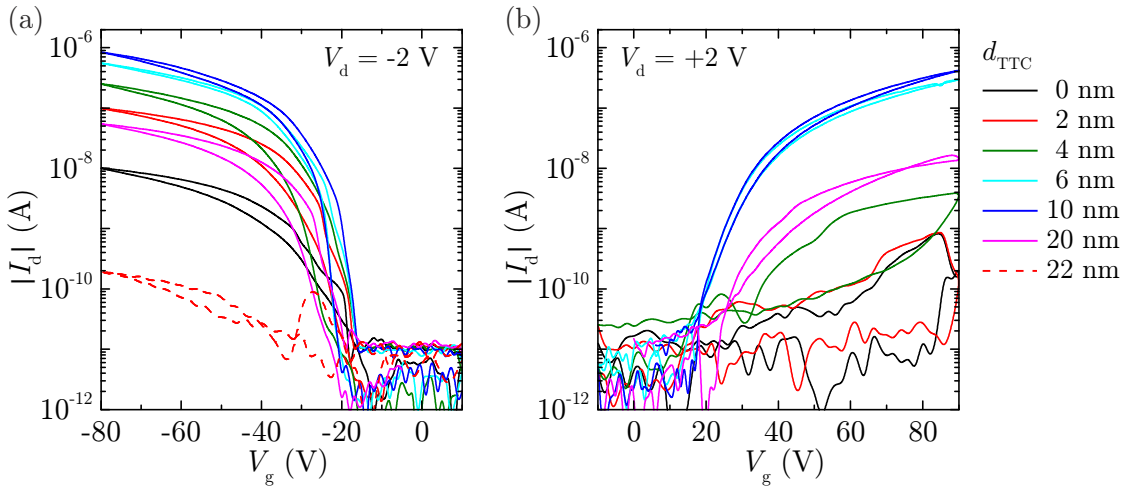


Figure 7.8: Transfer characteristics of a series of OFETs with a varying thickness of the TTC passivation layer, CuPc as active layer and Au top contacts. All devices are identical except for the nominal thickness of the TTC layer. The hole transport regime is displayed in (a), the electron transport regime in (b).

and $\mu_e \approx 0.5 - 1 \times 10^{-2}\,\mathrm{cm^2/Vs}$ for electron transport. A maximum is reached at $d_{TTC} = 10\,\mathrm{nm}$ with a hole mobility of $\mu_h = 3 \times 10^{-2}\,\mathrm{cm^2/Vs}$ and an electron

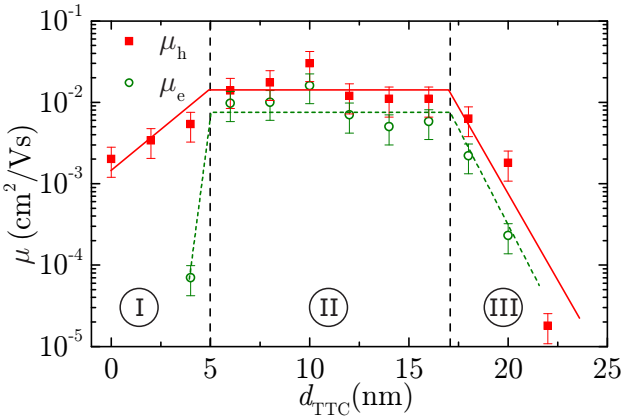


Figure 7.9: Charge carrier mobility of holes (red squares) and electrons (green circles) determined by TLM as a function of nominal TTC thickness. Three distinct transport regimes I, II and III can be distinguished which can be correlated to the growth regimes discussed in sec. 7.1.2. The lines are guides for the eye, the numbers in circles represent the mobility regimes I, II and III [139].

mobility of $\mu_e = 1.6 \times 10^{-2}\,\mathrm{cm^2/Vs}$.

Finally, for TTC thicknesses larger than 16 nm, both charge carrier mobilities decrease rapidly with increasing TTC thickness, until no electron transport is observed for $d_{TTC} = 22\,\mathrm{nm}$ any more. Hole transport performance is drastically reduced with $\mu_h \approx 2 \times 10^{-5}\,\mathrm{cm^2/Vs}$. For even larger TTC thicknesses, no charge carrier transport is observable.

Discussion

In the preceding section, the growth of TTC on SiO_2 was investigated. It can be distinguished in three distinct growth regimes. These three regimes can be directly correlated to the three mobility regimes observed in the $\mu(d_{TTC})$ dependence depicted in fig. 7.9. In regime I, which is schematically drawn in fig. 7.10(a), the TTC layer is not completely closed, which implies electron traps at the interface between bare SiO_2 and CuPc. This leads to the suppression of electron transport in analogy

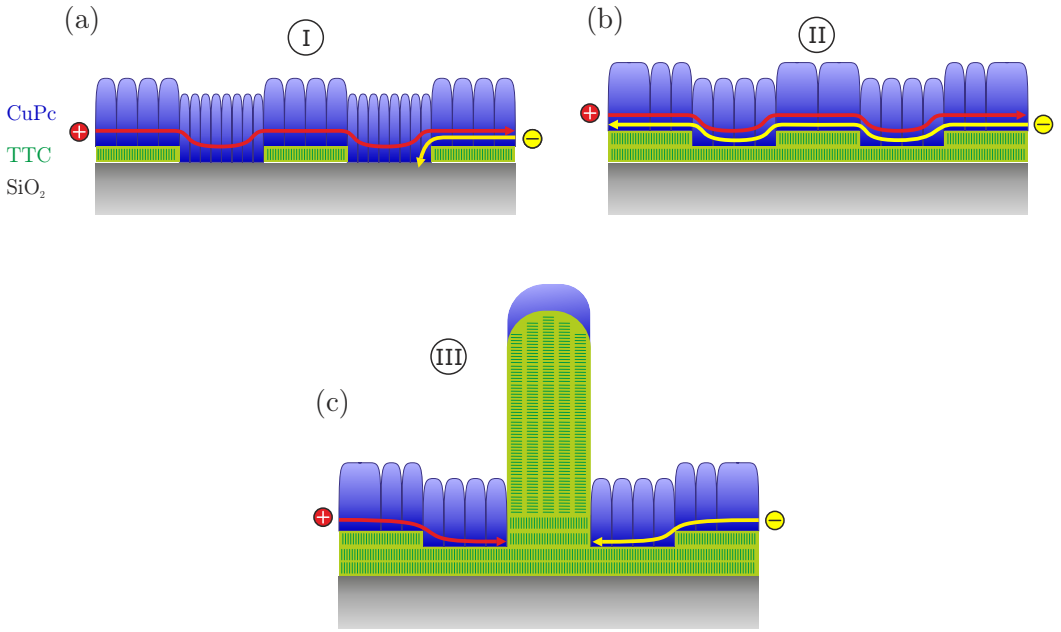


Figure 7.10: Schematic sketch of the three charge carrier transport regimes correlated to different growth behaviors for CuPc (blue) deposited on TTC (green). The charge carrier transport is indicated by red and yellow lines for holes and electrons, respectively. (a) Sub-monolayer regime I with electron traps, (b) ambipolar regime II and (c) domination of high TTC columns consisting of flat-lying TTC molecules that suppress charge carrier transport in regime III.

to the results on unipolar FETs discussed in chapter 5. The transport of holes and electrons is indicated by red and yellow lines, respectively. For $d_{\mathrm{TTC}} = 4\,\mathrm{nm}$, there is already a percolation path for electrons across the channel, which leads to the onset of electron transport, but the uncovered parts of the substrate hinder high mobilities. The behavior of the hole transport can be explained by the larger grains of CuPc on TTC than on SiO_2. The higher the nominal TTC thickness, the larger is the average size of the CuPc crystallites. Thus, the number of grain boundaries in the CuPc film is reduced with increasing TTC coverage and the hole mobility increases.

Regime II is characterized by stable ambipolar charge carrier transport, as illustrated in fig. 7.10(b). The SiO_2 substrate is completely covered by TTC, and electrons and holes can be transported. The charge carrier mobilities on TTC are significantly higher than on PMMA because the size of the CuPc crystallites is larger and the polaronic interaction is lower due to a smaller dielectric constant. The AFM images demonstrate that this regime is already characterized by the formation of individual TTC columns. It seems surprising that they do not affect the charge carrier transport for thicknesses around $10 - 14\,\mathrm{nm}$ as seen in fig. 7.1. As will be shown in chapter 8, this can be explained by two processes competing against each other in this regime. On the one hand, the ratio of the substrate occupied by the high insulating columns increases with increasing TTC thickness, but on the other hand, the CuPc grains become larger, as already seen in fig. 7.4(d). Thus, these two processes balance each other until the TTC columns become too numerous and regime III is reached.

In regime III, depicted in fig. 7.10(c), the transport of charge carriers is seriously affected by the insulating TTC columns that are obstacles for electrons and holes. Consequently, the respective charge carrier mobilities decrease due to the increasing roughness of the interlayer until there are no percolation paths between the columns any more and the charge carrier transport is completely suppressed. The issue of surface roughness of the dielectric is a well-known problem for efficient charge carrier transport in OFETs [128].

7.3 Reduction of contact resistance

7.3.1 Measurements

As already discussed in sec. 6.2.3, it is desirable to adjust the type of injected charge carriers by the choice of the appropriate contact material. This is important for the realization of complementary inverters which require one n-type and one p-type

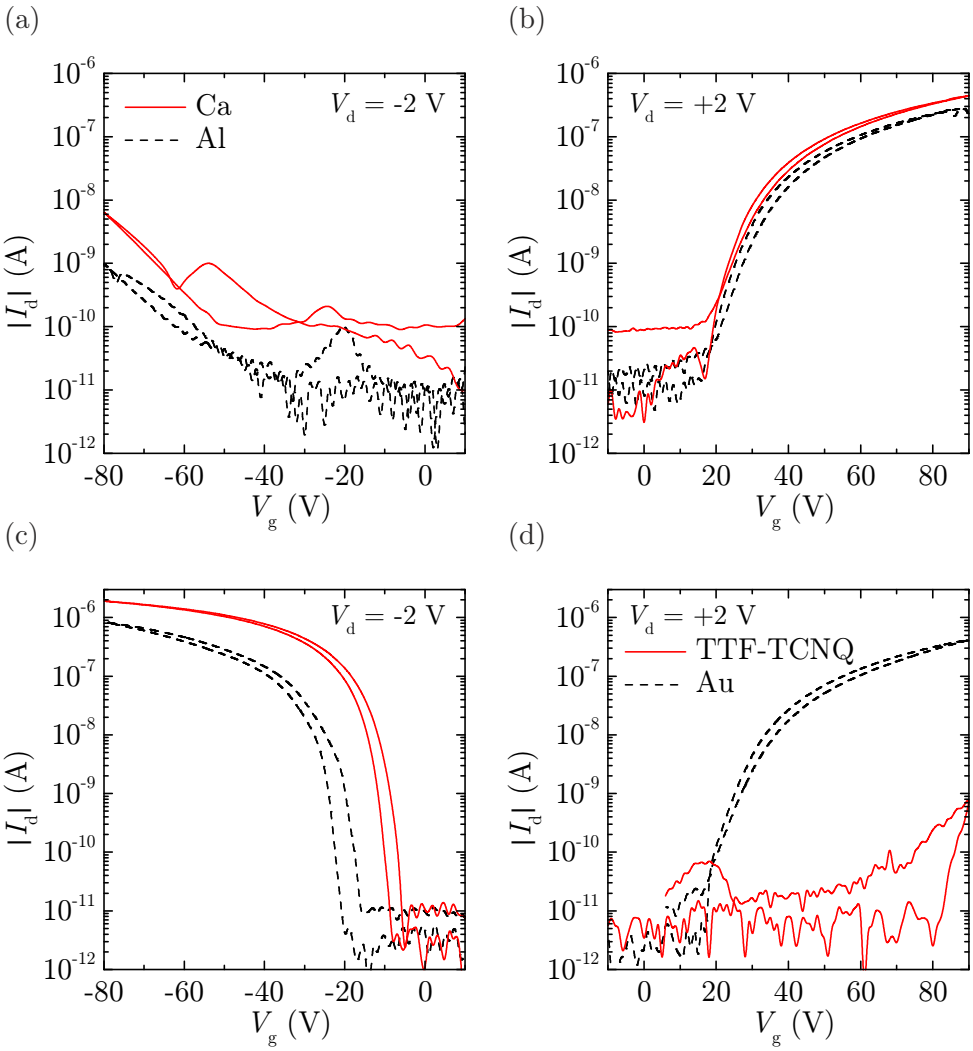


Figure 7.11: (a) and (b): Transfer characteristics of transistors with Ca and Al top contacts. Parameters of both devices are: $d_{\mathrm{TTC}} = 11\,\mathrm{nm}$, $d_{\mathrm{CuPc}} = 25\,\mathrm{nm}$, $L = 50\,\mu\mathrm{m}$, $W = 3.0\,\mathrm{mm}$. Electron mobilities determined by TLM are $\mu_e = 1.1 \times 10^{-2}\,\mathrm{cm^2/Vs}$ for both devices, contact resistances are $R_{\mathrm{c,Ca}} = 1.1\,\mathrm{M\Omega}$ for Ca electrodes and $R_{\mathrm{c,Al}} = 4.2\,\mathrm{M\Omega}$ for Al electrodes determined at $V_{\mathrm{eff}} = 20\,\mathrm{V}$. (c) and (d): Comparison of transfer characteristics of transistors with TTF-TCNQ and Au top contacts. Parameters of both devices are: $d_{\mathrm{TTC}} = 11\,\mathrm{nm}$, $d_{\mathrm{CuPc}} = 25\,\mathrm{nm}$, $L = 50\,\mu\mathrm{m}$, $W = 3.0\,\mathrm{mm}$.

transistor on the same substrate. Ca and Al exhibit good *n*-type characteristics, whereas hybrid electrodes of F_4TCNQ and Au inject only holes in the case of PMMA-passivated CuPc transistors. Ca and Al are also suitable for *n*-type devices on TTC-passivated substrates, as it is shown in fig. 7.11(a) and (b). Here, transfer characteristics of two CuPc OFETs with a TTC passivation layer of nominally

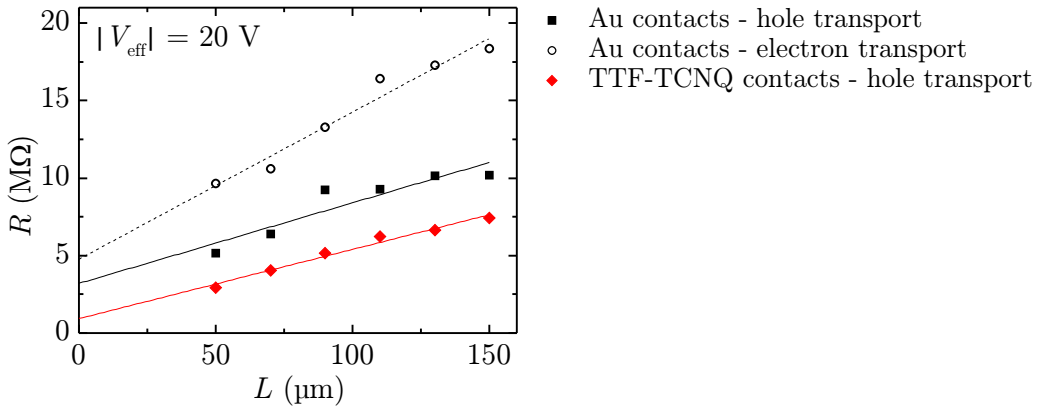


Figure 7.12: TLM analysis of the devices shown in fig. 7.11(c) and (d). The lines are linear fits of the data to determine charge carrier mobilities and contact resistances.

11 nm are depicted. Both samples exhibit good electron transport with identical mobilities of $\mu_e = 1.1 \times 10^{-2}\,\mathrm{cm^2/Vs}$. The current increase observed in the hole transport regime is very low and only slightly above leakage current. Thus, hole injection barriers are extremely high and the devices can be considered as unipolar *n*-type. In analogy to the differences of the respective work functions, the contact resistance of the sample with Ca contacts is only $R_{c,Ca} = 1.1\,\mathrm{M\Omega}$, whereas it is $R_{c,Al} = 4.2\,\mathrm{M\Omega}$ for Al electrodes, which is in good agreement with the lower electron injection barrier of Ca than Al (see also sec. 6.2.3).

F_4TCNQ/Au electrodes are unfavorable because the fabrication is critical. The thickness of the thin F_4TCNQ interlayer is hard to control. In several cases, a suppression of electron injection on TTC-passivated substrates could not be achieved with F_4TCNQ/Au electrodes [131]. Additionally, the material is highly sensitive to air and the usage of F_4TCNQ in the evaporation chamber has to be done with care because of its low sublimation temperature. Hence, an alternative contact material is required that provides unipolar hole injection but is more reliable and easier to handle. Organic metals are promising candidates due to their relatively high work function, stability in ambient air and convenient evaporation temperatures [90,92]. Thus, the organic metal TTF-TCNQ is used to fabricate top contacts with a thickness of 150 nm.

Fig. 7.11(c) and (d) depict transfer characteristics of two CuPc transistors on nominally 10 nm TTC. One device has Au contacts whereas the other one has TTF-TCNQ contacts. The transistor with Au contacts is ambipolar, as usual, but the device with TTF-TCNQ contacts shows unipolar *p*-type behavior. The threshold voltage for the hole transport regime is reduced from $V_{t,h} = -36\,\mathrm{V}$ for Au con-

tacts to $V_{t,h} = -17\,V$ for TTF-TCNQ contacts. A TLM analysis of both devices is given in fig. 7.12 for electron transport with Au contacts and hole transport for both contact materials. The characteristic device properties can be seen in table 7.2. Hole mobilities are almost identical for Au and TTF-TCNQ contacts but the contact resistance of the sample with TTF-TCNQ contacts is by a factor of 3 lower than for Au contacts. These results confirm that the injection barrier is considerably lowered and hole injection is enhanced. Apart from TTF-TCNQ, CuPc transistors were also fabricated with TSF-F_2TCNQ top contacts. The results are comparable. Electron injection is suppressed, whereas hole injection is enhanced with reduced threshold voltage and contact resistance for TSF-F_2TCNQ contacts and a hole mobility comparable to Au contacts. The reduction of the contact resistance was even stronger than with TTF-TCNQ: $R_{c,Au} = 55\,M\Omega$ and $R_{c,TSF-F_2TCNQ} < 10\,M\Omega$. However, the results are hard to compare because the TTC thickness was not optimized in the case of the comparison between Au and TSF-F_2TCNQ as contact materials which resulted in a relatively low hole mobility of $\mu_h \approx 7.4 \times 10^{-3}\,cm^2/Vs$ [75].

Comparing the sub-threshold swing in the hole transport regime, one determines values of $S_{TTF-TCNQ} = 1.2\,V/dec$ and $S_{Au} = 1.5\,V/dec$. These values are almost comparable to amorphous silicon TFTs, which exhibit values between 0.3 and 1.5 V/dec [146].

contact material	$V_{t,h}$ (V)	$V_{t,e}$ (V)	μ_h (cm^2/Vs)	μ_e (cm^2/Vs)	$R_{c,h}$ (MΩ)	$R_{c,e}$ (MΩ)
Au	−36	+49	3.0×10^{-2}	1.7×10^{-2}	3.2	4.8
TTF-TCNQ	−17	—	3.5×10^{-2}	—	0.9	—

Table 7.2: Transistor data determined by TLM of the devices shown in figs. 7.11(c) and (d) and 7.12.

7.3.2 Discussion

TTF-TCNQ has been reported to exhibit a work function of approximately 4.8 eV, which is comparable to Ag, whereas the work function of TSF-F_2TCNQ is supposed to be slightly higher, approximately 5.0 eV, therefore comparable to Au [90, 92]. As already discussed in sec. 6.2.3, the effective work function of Au and Ag top electrodes is considerably lower so that electron injection is enabled. Damages in the uppermost CuPc layer due to the exposure to high temperatures during metal evaporation can be responsible for this reduction [118, 147]. Furthermore, a

decrease of the effective work function is supposed to be induced by metal clusters inside the organic layer [116, 117, 148].

Another effect lowering the work function of metal electrodes on organic surfaces is the so-called *push-back effect* [149]. Before metal and organic semiconductor are brought into contact, the metal work function can be written as the sum of the chemical potential of the bulk metal μ_{bulk} and a surface dipole SD caused by electrons spilling out of the metal surface into vacuum:

$$\phi = \mu_{\text{bulk}} + \text{SD}. \tag{7.1}$$

This effect is illustrated schematically in fig. 7.13(a). The corresponding profile of the electron density ρ is shown in (b). When the metal and the organic semiconductor are brought into contact the push-back effect occurs: the electrons spilling out in vacuum are pushed back into the metal by the adsorbed organic molecules,

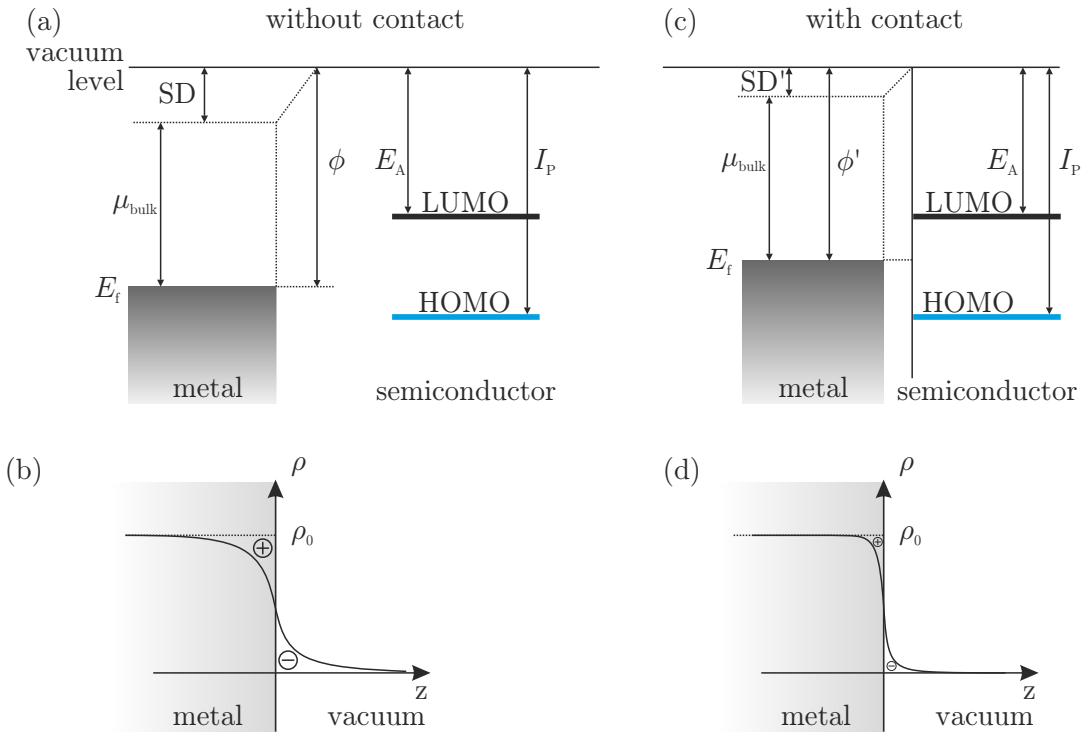


Figure 7.13: Schematic illustration of energy level alignment at metal/organic interfaces [149, 150]. (a) Without contact, the metal work function is the sum of the bulk chemical potential and the surface dipole caused by electrons spilling out of the metal surface. (b) Electron density profile in the case of (a). (c) Reduction of the surface dipole and thus of the effective work function due to the push-back effect when the metal is brought into contact with an organic semiconductor. (d) Electron density profile in the case of (c).

and the surface dipole is reduced to SD′ as depicted in fig. 7.13(c) and (d). Consequently, the "new" effective work function of the contact is given by

$$\phi' = \mu_{\mathrm{bulk}} + \mathrm{SD}' < \phi. \tag{7.2}$$

This shift of the metal work function can explain the decrease of the electron injection barrier and the increase of the hole injection barrier in top contacts of Au and Ag, as it is observed in our case.

Organic/organic interfaces are known to behave differently. Due to the lower charge carrier densities in organic materials, no push-back effect is supposed to occur here. Hence, the Fermi levels of TTF-TCNQ and TSF-F_2TCNQ are assumed to be aligned closely to the HOMO of CuPc. This assumption agrees well with the observed unipolar *p*-type characteristics and the low contact resistances of OFETs with top electrodes of these materials and can also explain the reduction of the threshold voltage for hole transport when TTF-TCNQ is used instead of Au.

7.4 Summary

TTC has been introduced as an alternative passivation layer in this chapter. The growth mechanism of TTC on SiO_2 can be classified as Stranski-Krastanov-like with three different growth regimes depending on the nominal TTC thickness: (i) growth of isolated flat TTC islands consisting of one monolayer, (ii) formation of a closed TTC film with flat, smooth terraces and some individual columns and (iii) domination of TTC columns with several hundreds of nanometers in height. XRD measurements confirmed the high crystallinity of the TTC layer with a low mosaicity. CuPc forms a polycrystalline layer consisting of α-phase CuPc when deposited on TTC. The grain size is considerably larger than on SiO_2 or PMMA and can be compared to that on OTS-treated SiO_2. XRD measurements indicate that an additional crystal phase is formed with increasing TTC thickness. However, this effect cannot be investigated in more detail at this point due to the high TTC columns. Transistor characteristics of CuPc OFETs with TTC passivation layer and Au top electrodes depend strongly on the TTC thickness and are also distinguished in three regimes which can be correlated to the growth regimes: (I) unipolar hole transport due to the presence of electron traps on bare SiO_2 ($d_{\mathrm{TTC}} < 5$ nm), (II) stable ambipolar charge carrier transport with mobilities of $\mu_{\mathrm{h}} \approx 1 - 2 \times 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$ and $\mu_{\mathrm{e}} \approx 0.5 - 1 \times 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$ ($d_{\mathrm{TTC}} = 5 - 14$ nm) and (III) a strong decrease of both charge carrier mobilities due to a reduction of transport paths by the increasing number of TTC columns ($d_{\mathrm{TTC}} > 14$ nm).

Unipolar *n*-type characteristics with high electron mobilities can be achieved with

Ca or Al top-contacts which additionally provide significantly lower contact resistances than Au electrodes due to the lowered electron injection barriers. Organic metal top contacts of TTF-TCNQ and TSF-F_2TCNQ exhibit unipolar *p*-type characteristics and low contact resistances. Differences in energy level alignment between organic/organic and metal/organic interfaces as well as influences of high temperature during metal deposition are supposed to lower the effective work function of inorganic metal top contacts like Ag or Au. This effect enables electron injection but increases the hole injection barrier.

A remaining problem for ambipolar and complementary logic devices is the asymmetry between hole and electron mobilities. It limits the performance of organic inverters, as will be shown in chapter 11. AFM images indicate that the CuPc grain size increases with higher nominal TTC thickness, which should have positive influence on the charge carrier mobilities. However, the growth of the high TTC columns is supposed to counterbalance this effect. Consequently it is crucial to find a way to improve the layer-by-layer growth of the TTC film to be able to investigate the intrinsic effects of the increased CuPc crystallinity. This will be the topic of the following chapter.

Chapter 8

Balanced charge carrier mobilities with annealed TTC layers

8.1 Morphology

8.1.1 Morphology of annealed TTC passivation layers

AFM measurements

TTC used for our experiments has a bulk melting temperature around $T_m = 86$℃ as determined by differential scanning calorimetry (DSC) measurements [142]. To reorganize the surface morphology and to achieve a better ordering, substrates with TTC layers of various thicknesses were annealed at different temperatures in the range between 45℃ and 80℃ directly after deposition in dry nitrogen atmosphere for 120 min. Fig. 8.1 depicts AFM images of TTC layers with nominal thicknesses between 2 nm and 24 nm, which have been annealed at 60℃. The height profiles along the red lines are displayed in fig. 8.2(a) and (b). A drastic change of the surface topography is observed comparing these images to the non-annealed TTC layers shown in fig. 7.1. In the sub-monolayer regime I there are TTC islands with a height of one monolayer, like in the previous case. However, the area of the islands is larger and no second layer is present.

Serious deviations from the non-annealed samples occur at thicknesses higher than one monolayer (regime II). The height distribution becomes more homogeneous

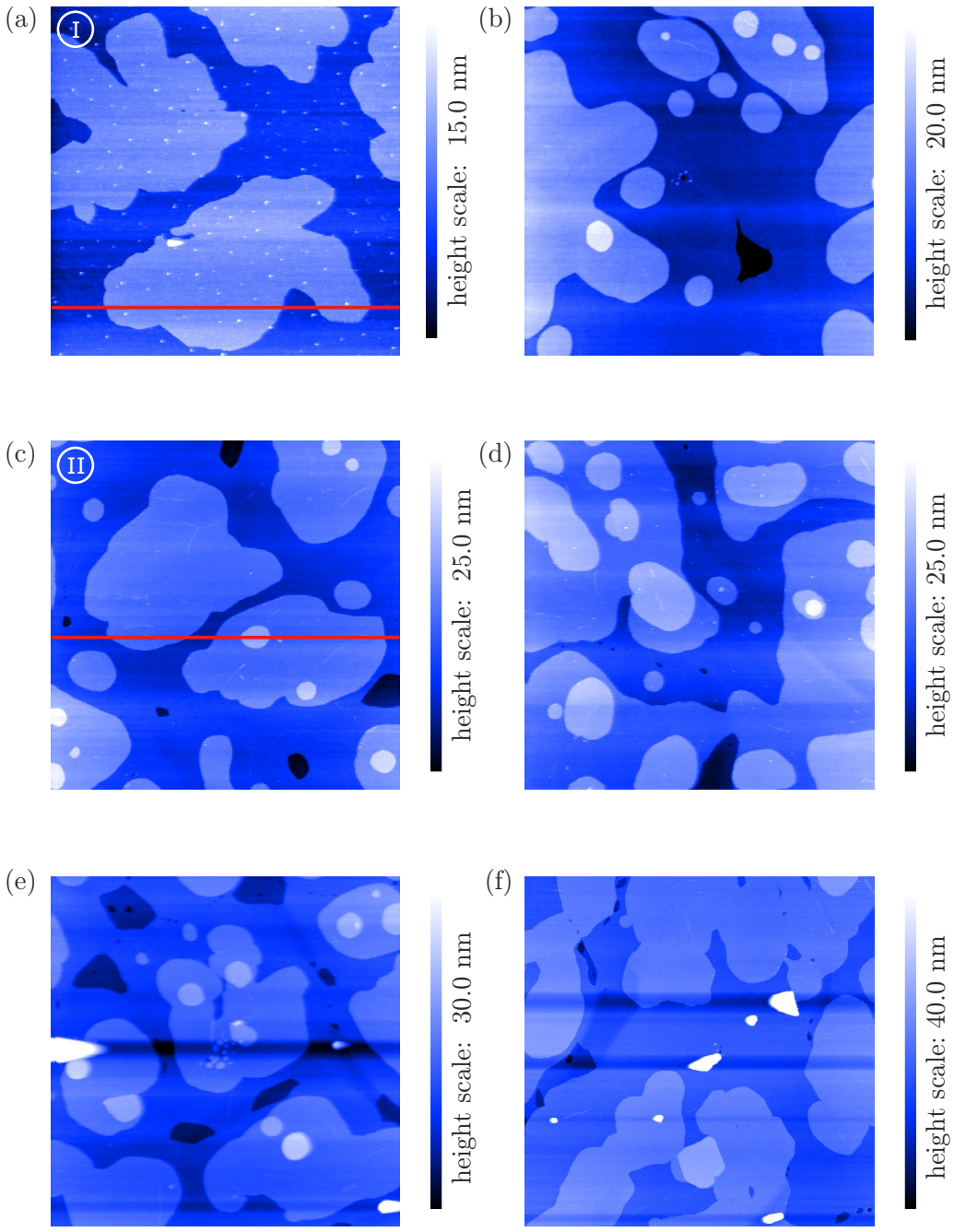


Figure 8.1: AFM images of nominally (a) 2 nm, (b) 6 nm, (c) 10 nm, (d) 12 nm, (e) 14 nm and (f) 24 nm TTC on SiO_2 annealed at 60°C for 120 min. Regime I corresponds to the sub-monolayer regime, regime II to a closed surface with flat terraces. Regime III with high TTC columns has vanished. All images are $5 \times 5\,\mu m^2$ [139].

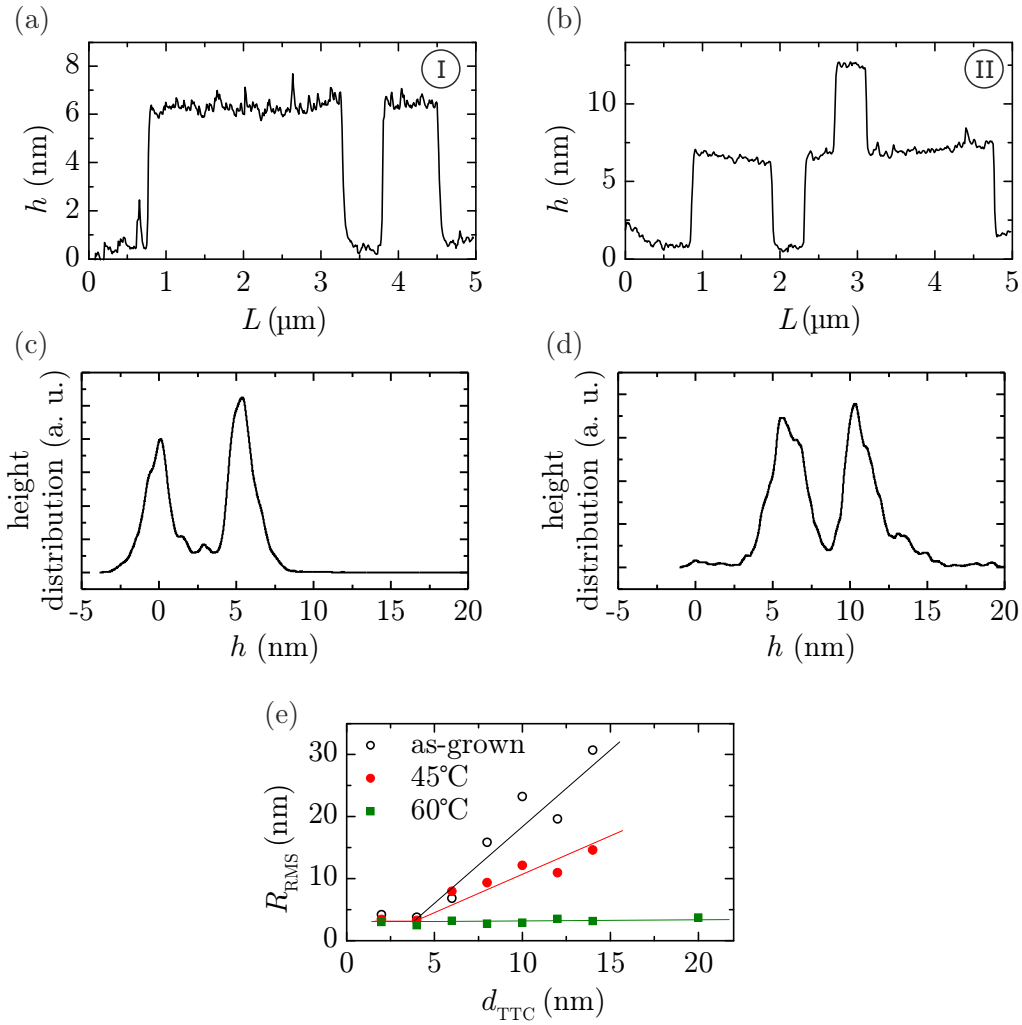


Figure 8.2: Height profiles along the red lines in fig 8.1 of passivation layers of 2 nm (a) and 10 nm (b) TTC annealed at 60°C for 120 min. (c) and (d) Height distributions of (a) and (b). (e) RMS roughness as a function of the TTC layer thickness for different annealing temperatures [142]. The lines are guides to the eye.

and the individual terraces are enlarged. Figs. 8.2(c) and (d) depict the height distribution of both samples. There are two distinct peaks with a distance of 5.5 nm representing the silicon oxide and the first TTC layer for the 2 nm sample and the first and second TTC layers for the 10 nm sample, respectively. In contrast to the as-grown TTC films, no regime III appears, where high TTC columns are dominating. Instead, flat terraces of constant height can still be determined for nominal TTC thicknesses of 24 nm and more. The extremely high TTC columns have disappeared and the material is redistributed to smooth terraces [139].

Fig. 8.2(e) shows the RMS roughness of the TTC films as a function of nominal TTC thickness for as-grown samples and samples annealed at 45℃ and 60℃ for 120 min. The RMS roughness increases with increasing TTC thickness for an annealing temperature of 45℃ but the slope is less steep than for the non-annealed samples. For 60℃, the roughness remains constant at $R_{\mathrm{RMS}} \approx 3.0\,\mathrm{nm}$. Higher annealing temperatures lead to a de-wetting of the SiO_2 surface even for temperatures below the melting point of TTC, possibly due to a reduced melting temperature of the TTC thin-film phase. Thus, 60℃ can be considered as the ideal annealing temperature for TTC passivation layers.

XRD measurements

Θ-2Θ-spectra of annealed TTC layers with nominally 5.5 nm and 20 nm TTC are displayed in fig. 8.3(a). The data has been measured by Alexander Hinderhofer

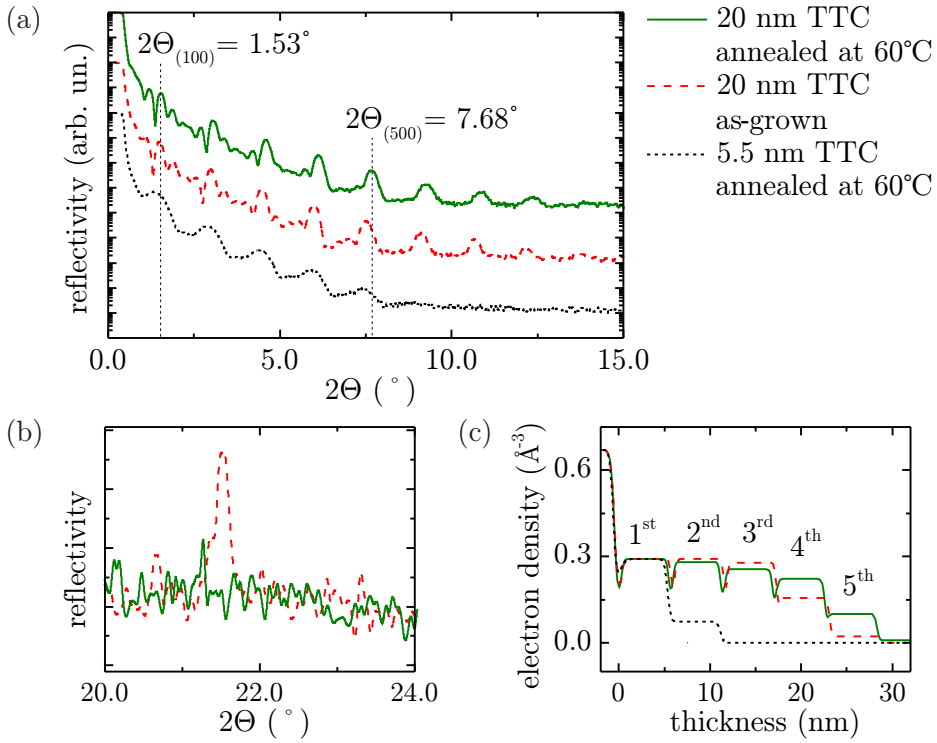


Figure 8.3: (a) Θ-2Θ-scans of TTC deposited on cleaned SiO_2 for various TTC thicknesses, with and without annealing. The lattice spacing of the annealed sample is reduced to $d' = 5.75\,\mathrm{nm}$ after annealing. (b) Θ-2Θ-scan of the reflex of flat-lying TTC. This phase vanishes upon annealing. (c) Electron density profiles of the first to fifth monolayer of the different samples determined by a fit of the reflectivity with the Parrat model.

from the group of Prof. Frank Schreiber at the University of Tübingen. For comparison, the data of an as-grown TTC layer of 20 nm is included in the diagram. Both annealed TTC layers are crystalline, whereas the reflexes are much more intense for the 20 nm layer due to a higher number of scattering molecules. A lattice spacing of $d' = 5.75\,\text{nm}$ was calculated from the (500) reflex at $2\Theta_{(500)} = 7.68°$. This is slightly lower than in the non-annealed case, where the lattice spacing can be calculated as $d = 5.86\,\text{nm}$ and shows that the molecules are tilted by approximately 10° and the molecular packing is increased after annealing.

Fig. 8.3(b) displays the Θ-2Θ-scan of flat-lying TTC molecules for the non-annealed TTC films shown in the inset of fig. 7.3(a). This TTC phase disappears upon annealing, as is demonstrated by the vanishing reflex at $2\Theta = 21.51°$. Hence, the assumption that the high columns consist of lying TTC molecules is confirmed. The occupancy of the individual monolayers, shown in fig. 8.3(c), can be derived from the fits of the reflectivity data with the Parrat model. Only the first and a small part of the second monolayer is filled in case of the 5.5 nm film. This agrees well with the length of the TTC molecule of approximately 6 nm. A comparison between the annealed and the as-grown sample with identical nominal TTC thickness reveals that the electron density of the annealed layer in the fourth and fifth monolayer is considerably higher than for the as-grown case. This is in good agreement with the AFM data and shows that the lying TTC molecules from the high columns are redistributed to the upright-standing phase in the smooth terraces.

As a conclusion, it can be stated that annealing of the TTC-covered substrates at 60℃ for 120 min in nitrogen atmosphere significantly improves the morphology and reduces the roughness, especially for large TTC thicknesses in the growth regimes II and III.

8.1.2 Growth of CuPc on annealed TTC

AFM measurements

In the next step, the growth of CuPc on annealed TTC layers is investigated and compared to the non-annealed case. CuPc is deposited on annealed TTC layers of various thicknesses ranging from 2 nm to 24 nm. The corresponding AFM images are given in fig. 8.4. TTC terraces covered by polycrystalline CuPc can clearly be seen. For all TTC thicknesses, proper AFM images can be achieved due to the vanishing of the high TTC columns upon annealing. The images confirm another effect that has already been indicated by the AFM measurements of CuPc on as-grown TTC: the length of the CuPc crystallites increases considerably with increasing TTC thickness. Fig. 8.5 demonstrates this growth with the help of

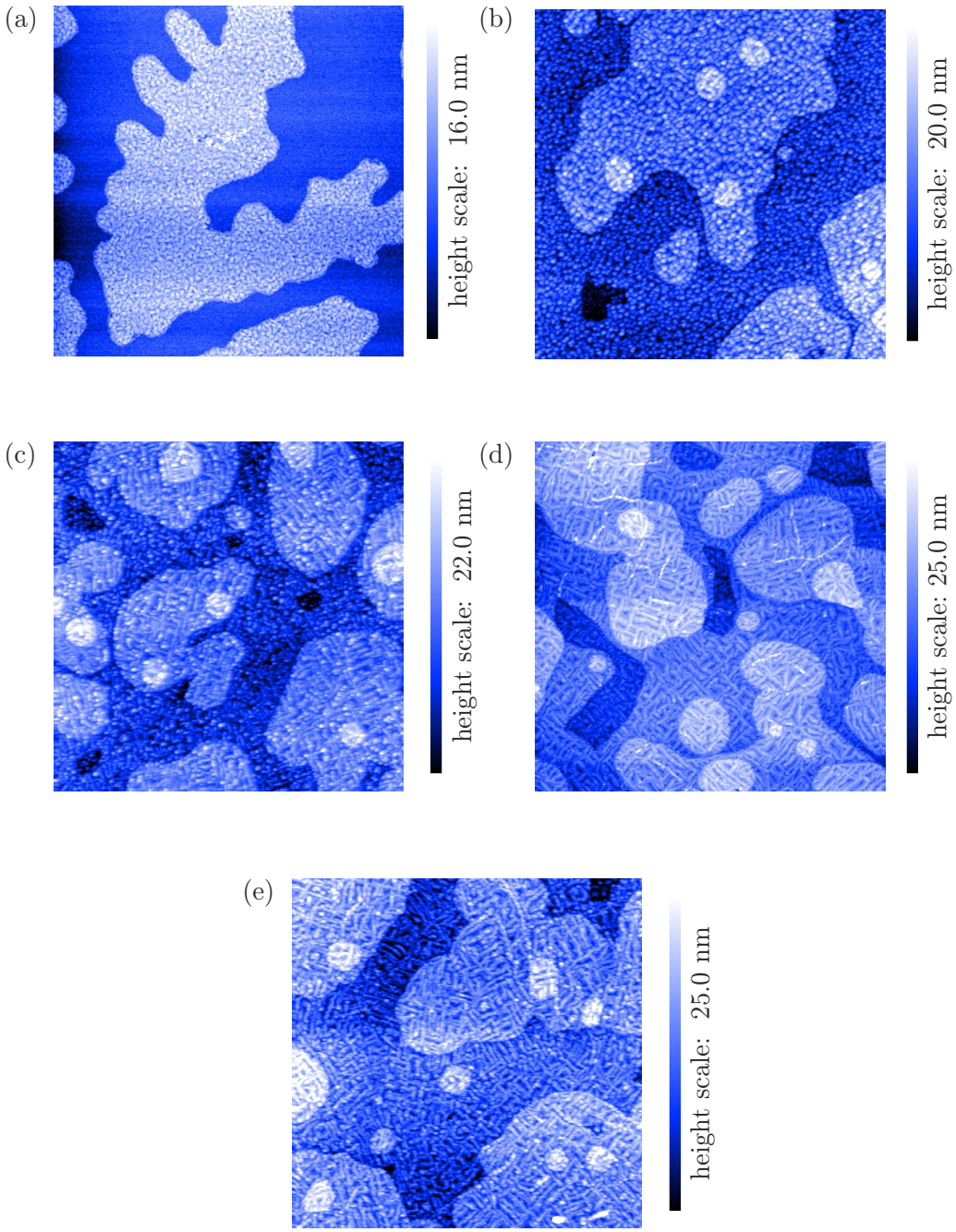


Figure 8.4: AFM images of CuPc on nominally (a) 2 nm, (b) 6 nm, (c) 10 nm, (d) 14 nm and (e) 20 nm TTC annealed at 60°C for 120 min on SiO_2. All images are $5 \times 5\,\mu m^2$ [139].

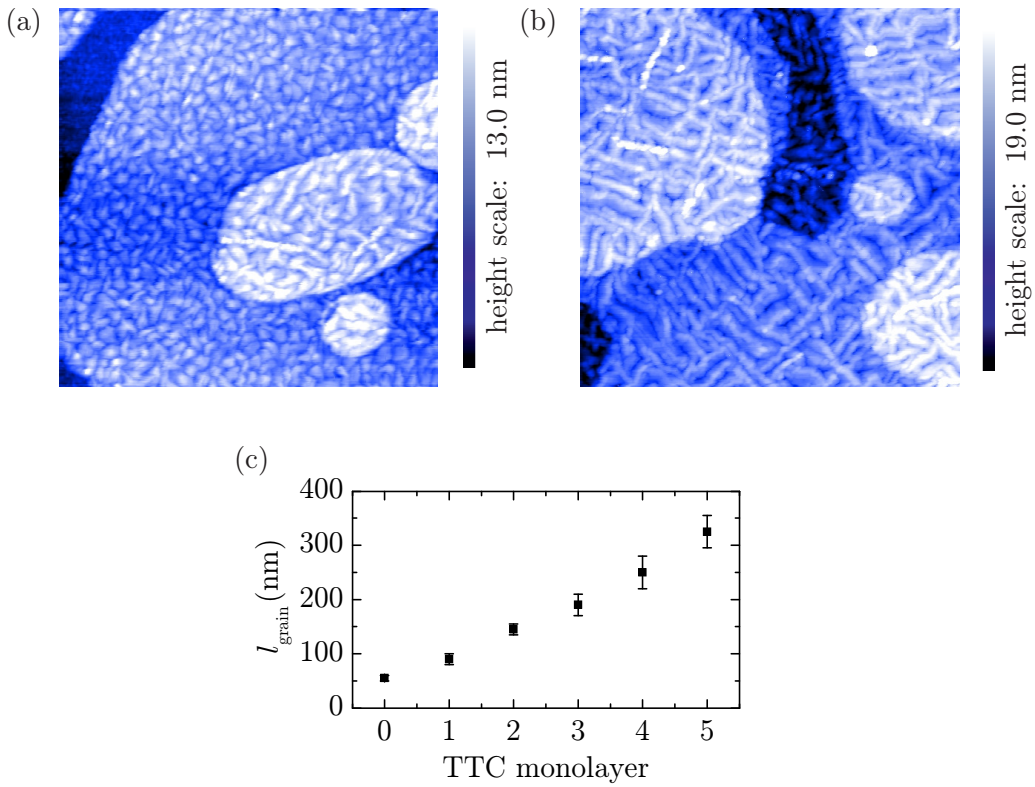


Figure 8.5: Enlarged AFM images ($2 \times 2\,\mu m^2$) of 5 nm CuPc on nominally (a) 5.5 nm and (b) 14 nm TTC annealed at 60°C for 120 min on SiO_2. An increase of the grain size with increasing number of monolayers can be observed. (c) Average length of CuPc grains as a function of the number of the TTC monolayer. The width of the grains is approximately 50 nm for each TTC thickness.

AFM micrographs of 5 nm CuPc on nominally 5.5 nm (a) and 14 nm (b) annealed TTC. In case of 5.5 nm, CuPc crystallites can be identified on the first and the second TTC monolayer, whereas CuPc grains on the second, third and fourth monolayer are visible on 14 nm annealed TTC. The CuPc grains become more and more elongated, while their width remains constant at approximately 50 nm. The typical length of the CuPc grains l_{grain} in dependence of the number of the TTC monolayer is given in fig. 8.5(c). The error bars are determined by variations between several representative grains. The length of the grains is increasing linearly with the number of TTC monolayers.

Additionally, the crystallites seem to grow preferentially along certain directions on thicker TTC layers. This effect can be seen in fig. 8.4(e), which depicts CuPc on nominally 20 nm TTC. Numerous long crystallites grow approximately perpendicular to each other [139].

XRD measurements

Θ-2Θ-scans of 25 nm CuPc on annealed and as-grown layers of nominally 20 nm TTC are depicted in fig. 8.6. At a first glance, both graphs look similar, but a remarkable difference is the increasing intensity of the unknown CuPc peak at $2\Theta = 8.55°$ on the annealed substrate. Even the second order of this peak at $2\Theta = 17.1°$ can be observed. This crystal phase can very likely be attributed to the long CuPc crystallites which grow on higher TTC monolayers. The redistribution of TTC molecules from the high columns to the flat terraces caused by the annealing process leads to a better filling of the fourth and fifth monolayer, as shown in fig. 8.3(c). It is known from AFM data that the size of the CuPc crystallites increases when they grow on thicker TTC layers. Hence, the proportion of large CuPc grains increases when deposited on annealed substrates, which leads to an increase of the XRD reflexes of this phase.

In summary, it can be stated that annealed TTC layers provide favorable growth conditions for CuPc. The grain size of the CuPc film increases linearly with underlying TTC monolayer in the analyzed range. These crystallites are oriented along preferential directions perpendicular to each other. This effect is accompanied by the formation of a new crystal phase that is only observed on thicker TTC layers. Hence, the growth of CuPc on higher TTC monolayers seems to be some kind of "pseudo-epitaxial" growth. It is imaginable that TTC grows in a slightly distorted way on SiO_2 and needs some five monolayers to relax to its original crystal structure, which then promotes optimum CuPc growth. But XRD measurements of TTC on SiO_2 do not exhibit any differences between thin and thick layers. An-

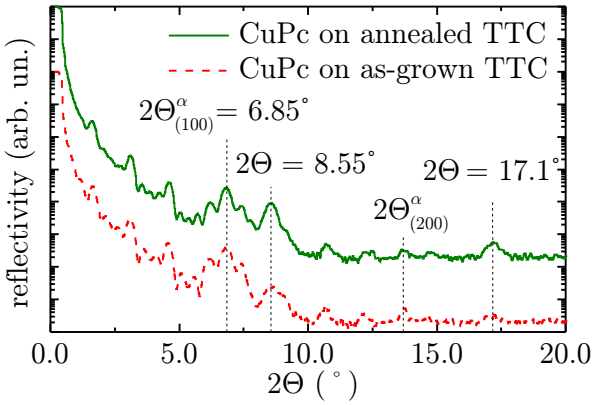


Figure 8.6: Θ-2Θ-scans of 25 nm CuPc on annealed and as-grown TTC passivation layers. The intensity of the reflex of the unknown CuPc phase ($2\Theta = 8.55°$) increases on annealed substrates with large TTC thickness.

other possible explanation might be the decreasing interaction between the CuPc molecules and the SiO_2 substrate in the case of increasing TTC thickness. However, the reason for this effect is not yet understood. For a further analysis, in-plane X-ray spectroscopy would be necessary. Unfortunately, this technique has not been available in the course of this thesis.

8.2 Transistor characteristics

8.2.1 Measurements

A series of transistors with annealed TTC passivation layer, CuPc as active material and Au top contacts have been fabricated. Except for the nominal TTC layer thickness, which is varied between 2 nm and 28 nm, all devices are identical. The transfer curves of a selection of this series are shown in fig. 8.7(a) and (b) for hole and electron transport, respectively. In contrast to the non-annealed case, no reduction of the transistor performance for large TTC thicknesses is observed. Charge carrier mobilities determined by TLM are plotted as a function of d_{TTC} in fig. 8.8. The lines are guides for the eye and demonstrate the general trend.

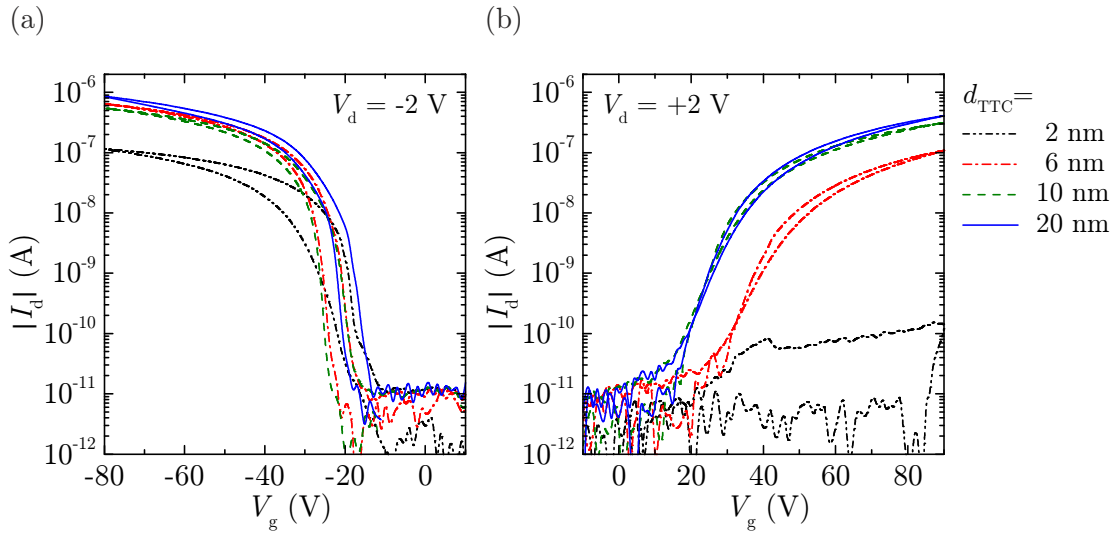


Figure 8.7: Transfer characteristics of a series of OFETs with annealed TTC passivation layer, CuPc as active layer and Au top contacts. All devices are identical with $L = 50\,\mu\mathrm{m}$ and $W = 3.0\,\mathrm{mm}$ except for the nominal thickness of the TTC layer. The hole transport regime is displayed in (a), the electron transport regime in (b).

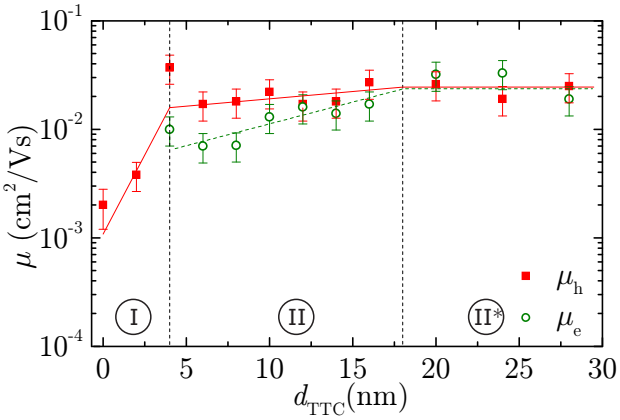


Figure 8.8: Charge carrier mobility of holes (closed squares) and electrons (open circles) determined by TLM as a function of nominal TTC thickness for transistors on annealed TTC layers. The lines are guides for the eye, the numbers in circles represent the mobility regimes I, II and II* [139].

The thickness dependence of the mobility can be distinguished into three regimes. Below a nominal TTC thickness of 4 nm, the transistors exhibit unipolar *p*-type characteristics (regime I) similar to the non-annealed case. The onset of electron transport occurs at $d_{\mathrm{TTC}} = 4\,\mathrm{nm}$ with $\mu_{\mathrm{e}} < \mu_{\mathrm{h}}$. Both charge carrier mobilities increase steadily between $d_{\mathrm{TTC}} = 4\,\mathrm{nm}$ and 18 nm (regime II). μ_{h} increases slowly until it reaches its maximum value $\mu_{\mathrm{h,max}} \approx 2 \times 10^{-2}\,\mathrm{cm^2/Vs}$, whereas the increase of μ_{e} is more pronounced. In contrast to the non-annealed case there is no regime III with diminishing charge carrier transport for large TTC thicknesses. Instead, for a thickness larger than 16 nm TTC (regime II*) electron and hole mobilities are equal with $\mu \approx 2 - 3 \times 10^{-2}\,\mathrm{cm^2/Vs}$ and remain constant with increasing TTC thickness [139].

8.2.2 Discussion

Figs. 8.7 and 8.8 have to be compared to the corresponding graphs of the non-annealed devices in figs. 7.8 and 7.9. The sub-monolayer regimes I are similar, as drawn schematically in fig. 8.9(a). The TTC layer is not fully closed, there are regions where CuPc grows on bare SiO_2, which results in a lower grain size and electron traps at the SiO_2 surface. Upon increasing d_{TTC}, more and more of the substrate is covered by TTC and the hole mobility increases. Annealing leads to a redistribution of the TTC molecules from upper layers to lower ones and thus shifts the complete filling of the first monolayer to smaller values of d_{TTC}. Thus, the onset of electron transport on annealed TTC occurs at a lower nominal TTC

thickness than on as-grown TTC and the transition from regime I to regime II occurs earlier.

Regime II, depicted in fig. 8.9(b), is characterized by increasing mobilities for both charge carrier types. The increase of the mobilities is not observed in the non-annealed case. The most important difference between annealed and as-grown TTC passivation layers is the vanishing of the high columns and the resulting equal RMS roughness for all TTC thicknesses. Here, two processes have to be considered.

On the one hand, the effect of the increasing size of the CuPc grains in the case of annealed TTC layers is important. As explained in sec. 2.1, the mobility in polycrystalline films increases with grain size because the charge carrier transport is limited by the hopping processes between grains for small grain sizes [25, 29]. The fact that the increase of μ_h is less pronounced than for μ_e demonstrates that the influence of grain boundaries is different for electrons and holes. An important parameter that determines the efficiency of this hopping process is the *grain boundary trap density* [30, 31]. Impurities or isolated CuPc molecules can be possible reasons for these traps. Since the trap density can be different for electrons and holes and since

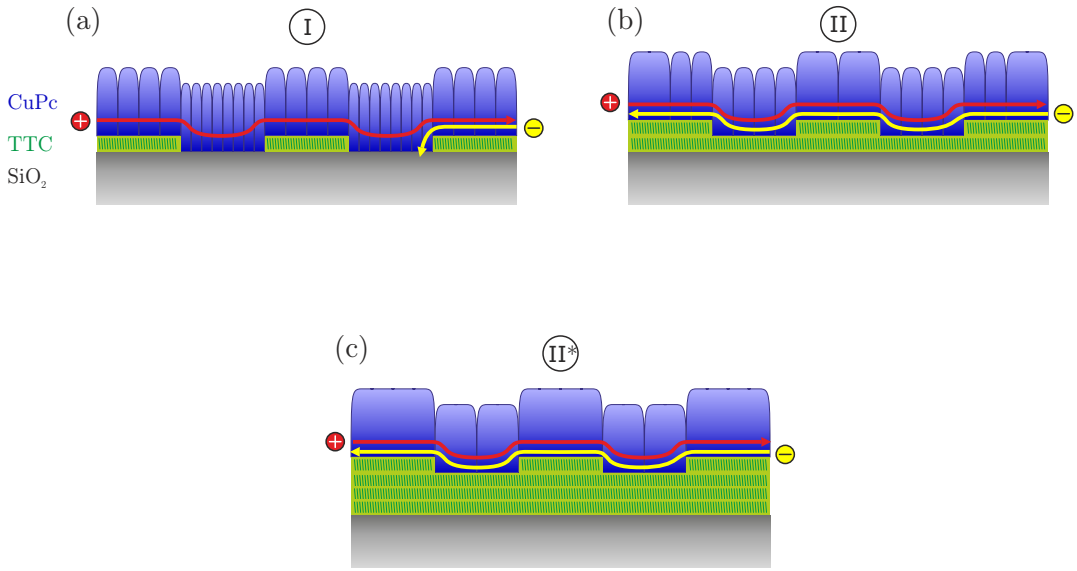


Figure 8.9: Schematic sketch of the three charge carrier transport regimes correlated to different growth behaviors for CuPc (blue) deposited on annealed TTC (green). The charge carrier transport is indicated by red and yellow lines for holes and electrons, respectively. (a) Sub-monolayer regime (I) with electron traps, (b) ambipolar regime (II) with higher hole mobilities and (c) balanced ambipolar regime (II*) with large CuPc grains.

the total number of grain boundary traps depends strongly on the average grain size, an asymmetric dependence of the charge carrier mobility on the morphology for electrons and holes is very likely. In chapter 10, a model will be discussed that allows for the estimation of the grain boundary trap densities of the respective charge carrier type. In our case, we determine higher grain boundary trap densities for electrons than for holes. This result indicates that the grain boundaries in CuPc thin films have a stronger influence on electron transport than on hole transport. The saturation value of μ_h in regime II is in good agreement with the data obtained for *p*-type devices on OTS-treated SiO_2 discussed in chapter 5. In that case, the CuPc morphology changes from round grains with diameters of approximately 90 nm on substrates kept at room temperature to worm-like crystallites with a typical length of 150 nm on heated substrates. However, the mobility turns out to be identical for both cases. These results show that a morphological optimum for hole transport in polycrystalline CuPc thin films is reached at $\mu_\mathrm{h} \approx 2 - 3 \times 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$. This assumption is confirmed by the fact that these values are comparable to the highest reported values in literature for hole transport in thin-film transistors with heated CuPc layer and silanization [80, 111]. Higher hole mobilities in CuPc are only reported in single-crystal FETs with $\mu_\mathrm{h} \approx 10^{-1}\,\mathrm{cm}^2/\mathrm{Vs}$ [107–109]. Electron mobilities of $\mu_\mathrm{e} \approx 2.0 - 3.0 \times 10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$ obtained here are record values for electron transport in CuPc indicating that TTC provides favorable growth conditions for CuPc thin films.

On the other hand the electrostatic interaction between the charge carriers and the SiO_2 surface has to be regarded. It depends on the distance between the channel and the substrate, i.e. the TTC thickness. As discussed in the preceding chapter, the charge carriers are supposed to form polarization clouds ("Fröhlich polarons") that move along the channel. These polarons can extend into the silicon dioxide for thin TTC layers, whereas they are completely uncoupled from the substrate for larger thicknesses. Interactions are also possible between the charge carriers and interface traps at the oxide surface. These traps can be charged and thus affect electrons and holes differently. Additionally, the effective mass of the polaron can be different for negative and positive charges. Both effects will decrease with increasing distance between SiO_2 and CuPc.

The existence of regime II* with constant mobilities for large TTC thicknesses instead of regime III with suppression of charge carrier transport can be explained by the vanishing of high TTC columns upon annealing. This effect is depicted schematically in fig. 8.9(c). The transition from regime II to II* with saturation of the charge carrier mobilities occurs at nominal TTC thicknesses around 17 nm, i.e. approximately after the third monolayer. However, as shown in fig. 8.5(c), the CuPc grain size increases further for larger TTC thicknesses. Hence, the charge

carrier transport is not limited by the grain size any more. Additionally, polaronic effects are assumed to be independent of the TTC thickness in this regime due to the large distance between SiO_2 and the transport channel. Thus, a saturation of the charge carrier mobilities occurs and the intrinsic limit of charge carrier transport of CuPc on TTC might be reached. It also has to be mentioned that the individual CuPc grains do not have to be defect-free. Zhang *et al.* showed with the help of transverse shear microscopy that even small islands of pentacene, which seemed to be structureless in AFM images, can consist of several randomly oriented crystallites [151]. Hence, there are additional intra-island grain boundaries which cannot be observed by AFM but which can be limiting factors for the charge carrier transport.

A further effect that has to be discussed is the influence of the steps between the individual TTC terraces on the charge carrier transport. These steps of approximately 6 nm in height are obstacles for the charge carriers and lead to a reduction of the charge carrier mobility, as discussed in sec. 7.2.2. The limiting effect of the steps might also be an explanation for the fact that the charge carrier mobilities saturate between regimes II and II* although the size of the CuPc grains increases at least up to the fifth TTC monolayer, which corresponds to a TTC thickness of approximately 30 nm, as shown in fig. 8.5(c). Since the grains do not seem to grow across the steps, another effect of these steps is that the CuPc molecules are vertically displaced by approximately 6 nm at each step, which corresponds to the half of the length of a CuPc molecule. This causes a different molecular overlap between two CuPc molecules. It would be useful to investigate this different molecular arrangement with the help of DFT calculations.

8.3 Summary

Charge carrier transport on annealed TTC layers has been investigated in this chapter. Annealing of the TTC-covered SiO_2 substrates in nitrogen atmosphere at 60°C for 120 min considerably improves the morphology of the passivation layer. The growth follows a well defined layer-by-layer growth. The high TTC columns vanish upon annealing and the RMS roughness is found to be independent of the TTC thickness. XRD measurements show that TTC layers are highly crystalline with a slightly reduced lattice spacing compared to the as-grown layers. The Bragg reflex of flat-lying TTC disappears after annealing, which confirms that the high columns of lying molecules, are redistributed to the smooth TTC terraces.

CuPc forms two distinct phases on annealed TTC: the usual α-phase and a yet unknown phase with a reduced lattice spacing. The intensity of the reflex of the new

phase increases with increasing TTC thickness. AFM measurements demonstrate that the CuPc morphology changes from round grains with a diameter of 50 nm on the first TTC monolayer to elongated grains with lengths up to 300 nm on the fifth monolayer. These long crystallites are supposed to be responsible for the new CuPc phase.

The behavior of the charge carrier mobilities as a function of nominal TTC thickness can be distinguished in three regimes. They differ from the regimes observed in the case of non-annealed samples. In the sub-monolayer regime, unipolar hole transport is observed. The hole mobility increases with TTC thickness due to the formation of larger CuPc grains on TTC compared to SiO_2. Regime II is characterized by a slowly increasing hole mobility and a stronger increase of electron mobility up to comparable values. This effect can be attributed to a growing CuPc grain size with increasing TTC thickness. Differences in the electrostatic interaction between the charge carriers and the SiO_2 gate dielectric as well as differing grain boundary trap densities are supposed to be responsible for the asymmetric dependence of electron and hole mobility on CuPc grain size. This effect will be investigated in more detail in chapter 10. Regime II* accounts for TTC thicknesses larger than 18 nm and is characterized by balanced electron and hole transport. Here, hole mobilities are in the same range as the highest reported values for thin-film transistors with CuPc and electron mobilities are the highest values ever reported for CuPc.

Chapter 9

Ambipolar MIS diodes

XRD and AFM measurements revealed that CuPc layers deposited on SiO_2, PMMA or TTC are polycrystalline with molecules standing almost upright on the substrate. Thus, the molecular stacking in these layers is highly anisotropic with considerably differing layer spacings parallel and perpendicular to the dielectric-semiconductor interface. Consequently, the molecular overlap between orbitals of neighboring molecules, which is a key parameter for the electrical properties of a thin film, is completely different for these two directions. FETs, which have been analyzed in the preceding chapters, are suitable for the investigation of charge carrier transport along the channel, i.e. parallel to the substrate. MIS diodes, which will be discussed in the following, are the right tool to measure charge carrier transport perpendicular to that interface. This will be done by impedance spectroscopy as explained in sec. 3.2.

9.1 MIS diodes with PMMA passivation layer

9.1.1 $C(V)$ measurements

In analogy to chapter 6, where the type of injected charge carriers is controlled by the choice of the top contact material, MIS diodes are fabricated on PMMA-passivated SiO_2 with Au, F_4TCNQ/Au and Ca contacts. TTF-TCNQ is not suitable as top contact material in MIS diodes because the conductivity of the organic metal is significantly lower than that of inorganic metals. Due to this effect, the

resistivity of TTF-TCNQ becomes the limiting factor at higher frequencies of the external AC field. The sample with Au contacts is structured with tape, whereas the two other diodes are structured with photoresist as described in sec. 4.2.2. In the following discussion of the impedance measurements, the specific capacitances C' will be used to provide a better comparability. As shown in sec. 3.2, a saturation of C' at high positive gate voltages corresponds to the accumulation of charge carriers at the semiconductor-dielectric interface, whereas the minimum in the $C'(V)$ graph is equivalent to the depletion of the semiconductor. The $C'(V)$ curves of the unipolar diodes with F_4TCNQ/Au and Ca contacts are depicted in fig. 9.1(a) and (b), respectively. The MIS diode with F_4TCNQ/Au top contacts shows unipolar hole injection since the accumulation capacitance is only detected for negative gate voltages, whereas the device with Ca contacts exhibits unipolar electron accumulation with a maximum of the capacitance at positive gate voltages. The diode with Au top contacts (fig. 9.1(c)) exhibits ambipolar characteristics with hole injection for negative gate voltages and electron injection with a comparable capacitance for

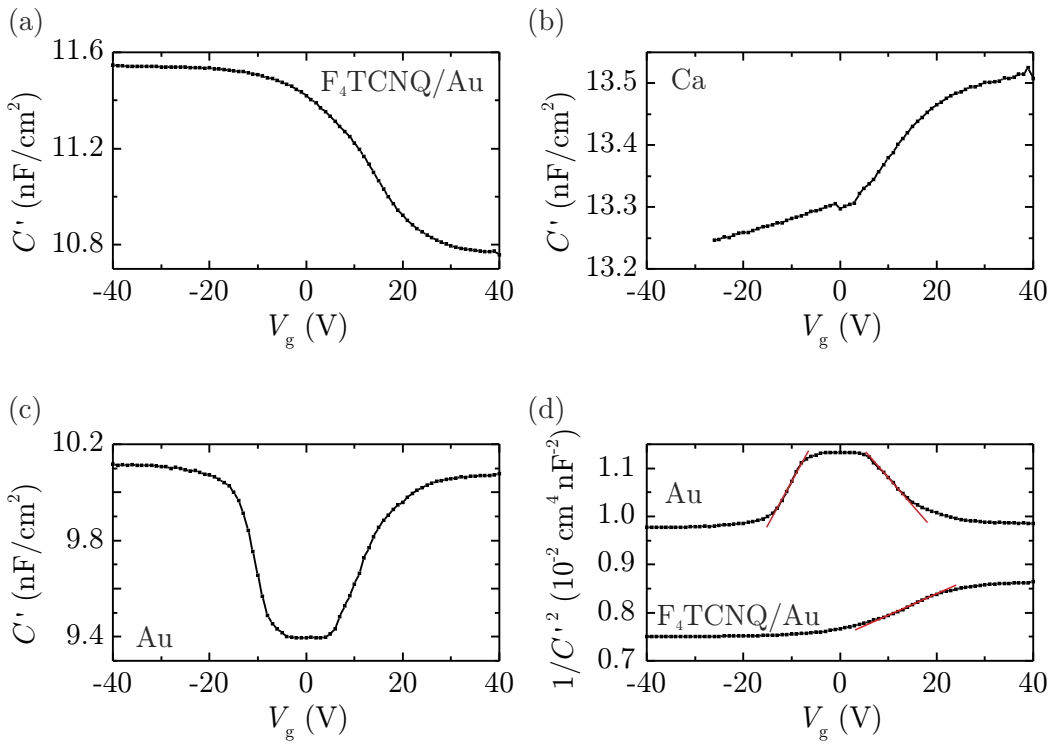


Figure 9.1: $C'(V)$ curves of PMMA-passivated SiO_2 measured at a frequency of $f = 1\,\mathrm{Hz}$. Top contacts are F_4TCNQ/Au (a), Ca (b) and Au (c). For a better comparability, the specific capacitances C' are plotted. The Mott-Schottky analysis of the devices with Au and F_4TCNQ/Au contacts is displayed in (d).

positive gate voltages. It is depleted around $V_g = 0\,V$. The switch-on voltages are approximately $V_{so,h} = -7\,V$ for holes and $V_{so,e} = +5\,V$ for electrons. These results are in agreement with the transistor measurements.

The thicknesses of the CuPc layers are 25 nm in the case of Au and Ca contacts and 50 nm in the case of F_4TCNQ/Au contacts. The capacitances for accumulation and depletion calculated from the geometrical parameters of the samples are listed in table 9.1. The measured values of the insulator capacitance C'_i and the total capacitance C'_{tot} of the device with Au contacts agree well with the calculated values which demonstrates that the device is fully depleted. As discussed in sec. 3.2.2, this causes problems with the Mott-Schottky analysis and only an upper limit of the doping concentration can be given. In the case of the sample with F_4TCNQ/Au contacts, where the thickness of the CuPc layer is 50 nm, the calculated total capacitance is lower than the measured value. This might be an indication that the device is not fully depleted and that the Mott-Schottky analysis can be applied. The minimum measured capacitance for this sample is equivalent to a CuPc thickness of 40 nm. Hence, the depletion length can be estimated to be of this order of magnitude: $l_{dep} \approx 40\,nm$. In the case of Ca, the capacitance does not saturate neither in the accumulation nor in the depletion regimes. This might be attributed to the structuring with photoresist, which could lead to a parasitic parallel capacitance that is superimposed to the $C'(V)$ data or to inaccuracies of the CuPc thickness. These effects prevent a proper Mott-Schottky analysis.

Fig. 9.1(d) depicts $1/C'^2$ vs. V_g used for the Mott-Schottky analysis. The red lines are linear fits of the $1/C'^2$ graph in the quadratic regime of the $C'(V)$ curve. The dopant concentrations for acceptors N_A and for donors N_D can be calculated from the slope of the fits with the help of eqs. 3.24 - 3.26. The results are given

contact material	calculated		measured			
	C'_i (nF/cm^2)	C'_{tot} (nF/cm^2)	C'_i (nF/cm^2)	C'_{tot} (nF/cm^2)	N_A (cm^{-3})	N_D (cm^{-3})
F_4TCNQ/ Au	12.2	10.4	11.56	10.78	7×10^{17}	—
Ca	13.5	12.4	13.52	13.25	—	—
Au	10.0	9.41	10.11	9.39	2×10^{17}	3×10^{17}

Table 9.1: Device parameters of MIS diodes with PMMA passivation layer and CuPc as active material. The calculated capacitances are determined by the geometric dimensions of the devices, the measured capacitances are extracted from the graphs in fig. 9.1. The dopant concentrations are determined by a Mott-Schottky analysis.

in table 9.1. Dopant concentrations are in the range of $10^{17}\,\mathrm{cm}^{-3}$ for both charge carrier types and both devices. Comparable values have already been measured by our group for hole-only diodes of CuPc [123] and have also been reported in polymeric MIS diodes by Scheinert *et al.* [61]. Impurities in the CuPc layer are supposed to be the origin of doping. These can be chemical impurities that have not been removed during purification or that have been incorporated into the layer during evaporation and act as interface states also causing the shift of the threshold voltage. Since F_4TCNQ is a strong organic acceptor, it can be responsible for the higher doping concentration of this device.

However, the Mott-Schottky analysis is related to some problems in the case of organic MIS diodes. Firstly, the existence of a single defined shallow acceptor or donor level is assumed [69]. This is usually not the case in organic semiconductors, which are not intentionally doped and exhibit an energetic distribution of localized states. Secondly, the thickness of the semiconductor has to be larger then the depletion length. In our case, this parameter can only be estimated, as done above. If the active layer is thinner or if the depletion length varies, only rough estimation of the doping can be given.

9.1.2 $C(f)$ measurements

Measurements

Following the approach by Stallinga *et al.* the charge carrier transport perpendicular to the substrate-semiconductor interface is supposed to be determined by diffusion [68]. The charge carrier mobility along this direction can be calculated by eq. 3.37:

$$\mu_\perp = \frac{2\pi e\, f_\mathrm{r}\, d_\mathrm{s}^2}{kT} \tag{9.1}$$

where f_r is the relaxation frequency of the respective charge carrier type in a $C'(f)$ measurement and d_s denotes the thickness of the semiconductor.

$C'(f)$ curves of the ambipolar MIS diode with Au contacts—corresponding to the $C'(V)$ measurements in fig. 9.1(c)—are depicted in fig. 9.2(a) for all three relevant regimes: hole accumulation ($V_\mathrm{g} = -40\,\mathrm{V}$), electron accumulation ($V_\mathrm{g} = +40\,\mathrm{V}$) and depletion ($V_\mathrm{g} = 0\,\mathrm{V}$). In the depletion regime, the measured capacitance corresponds to the depletion capacitance over the whole frequency range, whereas in both accumulation regimes, the accumulation capacitance is only detected at low frequencies where the charge carriers in the organic semiconductor can follow the external electric field. Upon increasing the AC frequency, the capacitance drops to the depletion value at $f = f_\mathrm{r}$. The relaxation frequency f_r is the frequency

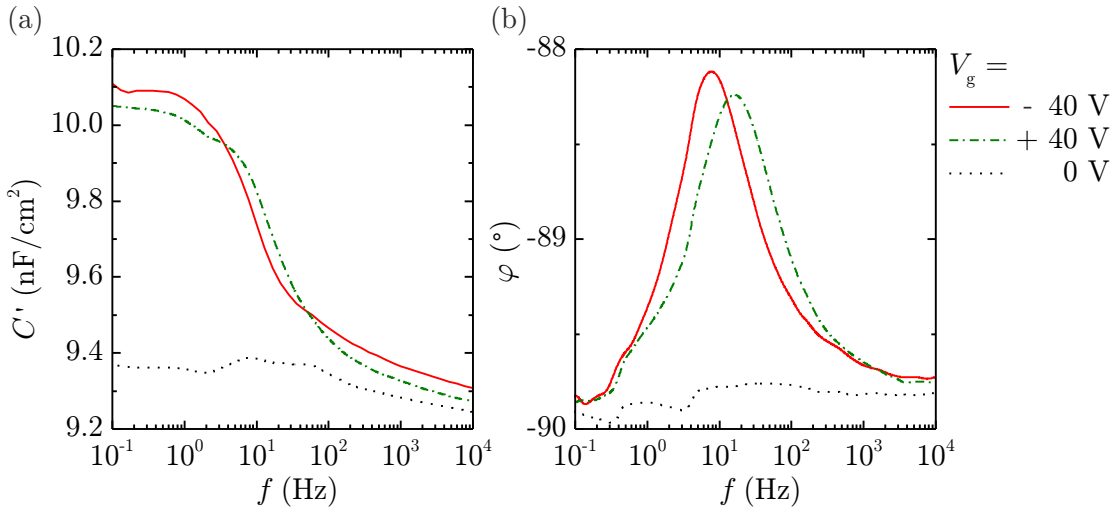


Figure 9.2: (a) $C'(f)$ curves of an MIS diode with 25 nm CuPc on PMMA-passivated SiO_2 and Au top contacts for hole accumulation (solid line), electron accumulation (dash-dotted line) and depletion (dotted line). (b) Corresponding phase shift to determine the relaxation frequencies.

where the charge carriers in the organic semiconductor cannot follow the external field any more. In regions where the capacitance is constant, the device acts as capacitor and the phase shift between real and imaginary part of the impedance is $\varphi = -90°$. As explained in sec. 3.2.3, a peak of φ can be attributed to the relaxation frequency. Thus, f_r can be identified with the maximum of φ as can be seen in fig. 9.2(b), where φ is plotted as a function of f for the three regimes. $C'(f)$ measurements are also performed on the diode with F_4TCNQ/Au contacts and displayed in fig. 9.3. The corresponding relaxation frequencies for holes $f_{r,h}$ and electrons $f_{r,e}$ using the diffusion and the doping approach (see sec. 3.2.3) are listed in table 9.2.

top contact			diffusion approach		doping approach	
	$f_{r,h}$ (Hz)	$f_{r,e}$ (Hz)	$\mu_{\perp,h}$ (cm^2/Vs)	$\mu_{\perp,e}$ (cm^2/Vs)	$\mu_{\perp,h}$ (cm^2/Vs)	$\mu_{\perp,e}$ (cm^2/Vs)
Au	8	17	1.2×10^{-8}	2.6×10^{-8}	6.1×10^{-10}	8.5×10^{-10}
F_4TCNQ/ Au	6	—	3.7×10^{-8}	—	1.3×10^{-10}	—

Table 9.2: Relaxation frequencies and charge carrier mobilities perpendicular to the substrate-semiconductor interface.

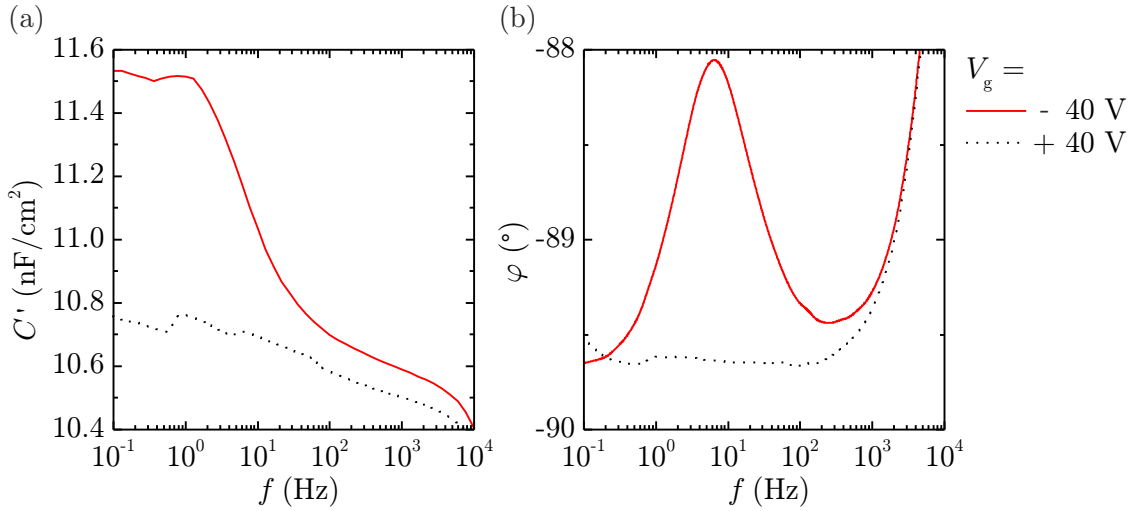


Figure 9.3: (a) $C'(f)$ curves of an MIS diode with 50 nm CuPc on PMMA-passivated SiO_2 and F_4TCNQ/Au top contacts for hole accumulation (solid line) and depletion (dotted line). (b) Corresponding phase shift to determine the relaxation frequency.

Discussion

Charge carrier mobilities perpendicular to the dielectric-semiconductor interface determined by the diffusion approach are in the range of $10^{-8}\,cm^2/Vs$ for both charge carrier types and contact materials. This is approximately four orders of magnitude below the field-effect mobility of electron transport in CuPc on PMMA-passivated SiO_2 and even five orders of magnitude below the hole mobility. This huge anisotropy between in- and out-of-plane mobility is in accordance with the DFT calculations. These calculations, discussed in sec. 2.3, predict a difference by a factor of at least 1000 between planar and perpendicular conduction. The overlap of the π-orbitals of neighboring CuPc molecules, which is crucial for efficient charge carrier transport, is significantly lower in the MIS-related case. Fig. 9.4 depicts a schematic sketch of both transport directions to illustrate the effects of different molecular arrangements parallel and perpendicular to the interface. A similar anisotropy has been observed for CuPc in unipolar *p*-type MIS diodes [123].

In literature, the dependence of the charge carrier mobility on the charge carrier density has been shown to be a further contribution to this anisotropy. Since the density of holes or electrons in field-effect devices decreases exponentially with the distance from the dielectric-semiconductor interface, the average charge carrier density is considerably lower in MIS diodes than in FETs [152]. In MIS diodes charge carrier transport takes place in the whole layer whereas in FETs, it is restricted to

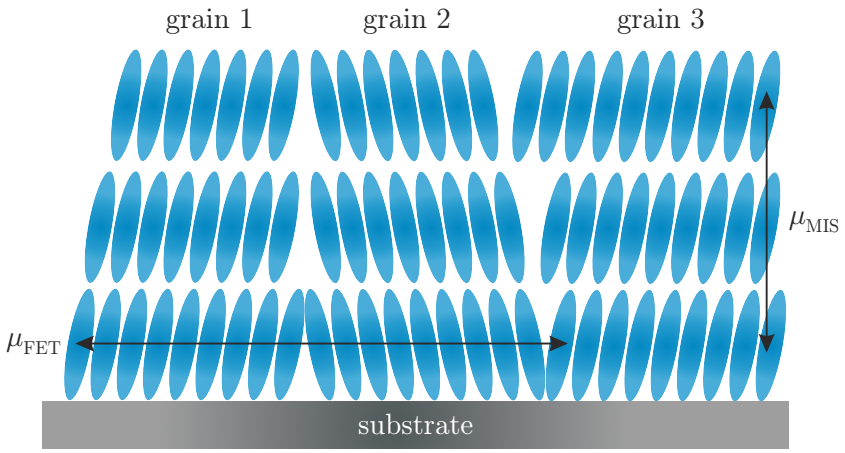


Figure 9.4: Illustration of charge carrier transport in FETs and MIS diodes. The anisotropy is caused by differing molecular overlaps in both directions as well as differing influences of grain boundaries.

the first nanometers next to the dielectric-semiconductor interface. The anisotropy between diodes and transistors with polymer active layers could be explained by this effect [57]. In that case, it has been attributed to the high energetic disorder related to a broad Gaussian-like DOS in amorphous polymers. However, in our case, the energetic distribution is supposed to be significantly lower due to the polycrystallinity of the organic semiconductor. Thus, the dependence of charge carrier mobility on the charge carrier density is assumed to be less pronounced, which is supported by the transistor measurements shown in chapter 6.

In contrast to OFETs, electron mobility in MIS diodes with CuPc on PMMA is approximately by a factor of two larger than hole mobility. Comparisons between individual samples demonstrate that this factor can be due to statistical variations and thus, electron and hole mobility can be considered as equal with $\mu_{\mathrm{MIS}} \approx 1 - 2 \times 10^{-8}\,\mathrm{cm}^2/\mathrm{Vs}$. As shown in chapter 6, hole mobility in comparably-fabricated FETs is systematically one order of magnitude larger than electron mobility with $\mu_{\mathrm{FET,h}} \approx 2 \times 10^{-3}\,\mathrm{cm}^2/\mathrm{Vs}$. A possible explanation for the reduced asymmetry in MIS diodes might be obtained by considering the number of grain boundaries and the related traps that have to be overcome by the charge carriers along their transport paths. In chapter 8, it has been demonstrated by variation of the grain size that the asymmetry between electron and hole transport decreases and eventually vanishes when the grain size is increased and the number of grain boundaries is reduced. Polycrystalline CuPc layers on PMMA consist of circular crystallites with diameters of ca. 50 nm. Since the layer thickness is only 25 nm for the sample with Au contacts and 50 nm for the device with F_4TCNQ/Au contacts,

one can assume that charge carriers do not have to cross a grain boundary when moving perpendicular to the dielectric-semiconductor interface like in MIS diodes. In OFETs, where the typical channel length is 50 µm, there are by a factor of 1000 more grain boundaries to cross. This effect is also illustrated in fig. 9.4. Thus, the effect of traps at grain boundaries will be much more pronounced in FETs than in MIS diodes with the given morphology.

The perpendicular charge carrier mobilities determined by the doping approach are approximately two orders of magnitude lower than those determined by the diffusion approach. These variations might be caused by the differing charge carrier transport processes, on which the respective models are based. The fact that in the diffusion model the hole mobility of the sample with F_4TCNQ/Au contact is the highest, whereas in the doping model it is lower than the mobility of the device with Au contacts can be attributed to the higher doping concentration of the diode with F_4TCNQ/Au contact. However, since the determination of the doping concentration is related to problems as discussed at the end of sec. 9.1.1, the mobilities calculated with the diffusion approach seem to be more reliable. Consequently, only the diffusion model will be discussed in the following case.

9.2 MIS diodes with TTC passivation layer

TTC has turned out to be the preferable passivation layer for ambipolar OFETs with CuPc as active material. For comparison to the experiments discussed above, MIS diodes were also fabricated on TTC. Fig 9.5(a) depicts a $C'(V)$ curve of an MIS diode with 25 nm CuPc on 15 nm as-grown TTC on SiO_2 and Au top contact. A clear ambipolar behavior is observed with distinct depletion and saturated accumulation regimes. The respective capacitances calculated geometrically are $C_{\mathrm{tot}} = 20\,\mathrm{nF/cm^2}$ and $C_{\mathrm{i}} = 24\,\mathrm{nF/cm^2}$. They are comparable to the measured values. This demonstrates that the device is fully depleted at $V_{\mathrm{g}} = 0\,\mathrm{V}$. The Mott-Schottky analysis can be seen in fig. 9.5(b), the corresponding doping concentrations are given in table 9.3. They are almost identical to the values of the PMMA-passivated device discussed above which shows that the doping is independent of the morphology and can be considered as a bulk value. However, as in sec. 9.1.1, they can only be considered as upper limits due to the fully depleted semiconductor. $C'(f)$ measurements and the corresponding phase shift φ of this device are shown in fig 9.6(a) and (b), respectively. The calculated charge carrier mobilities perpendicular to the dielectric-semiconductor interface are listed in table 9.3. An important difference to the $C'(f)$ data on PMMA given in table 9.2 is observed: while the electron mobility is comparable to the device with PMMA

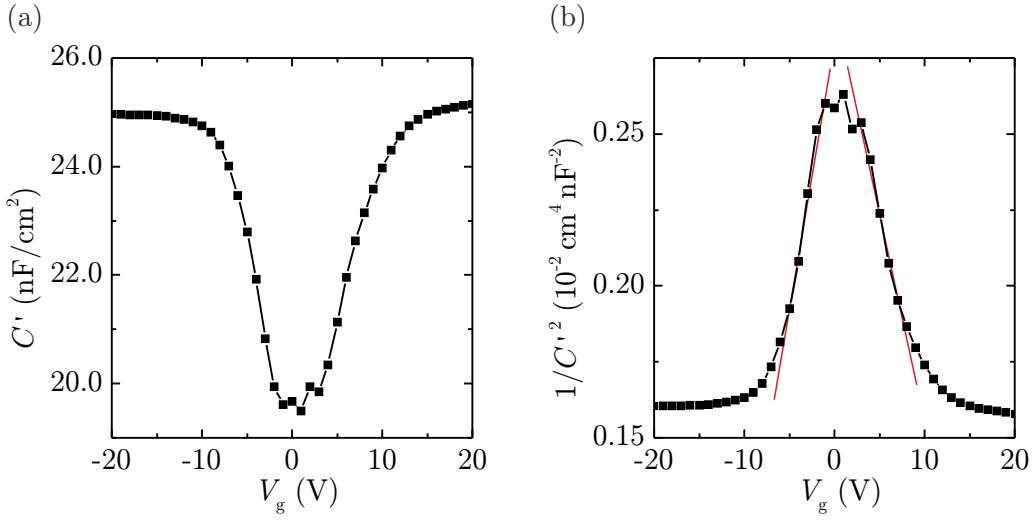


Figure 9.5: $C'(V)$ curve (a) and Mott-Schottky analysis (b) of an MIS diode with 25 nm CuPc on 15 nm as-grown TTC with Au top contacts measured at a frequency of $f = 0.5$ Hz. The straight lines are linear fits to determine the doping concentration of the semiconductor.

passivation layer, the hole mobility is approximately one order of magnitude higher. This is a contradiction to the fact that the asymmetry between electron and hole

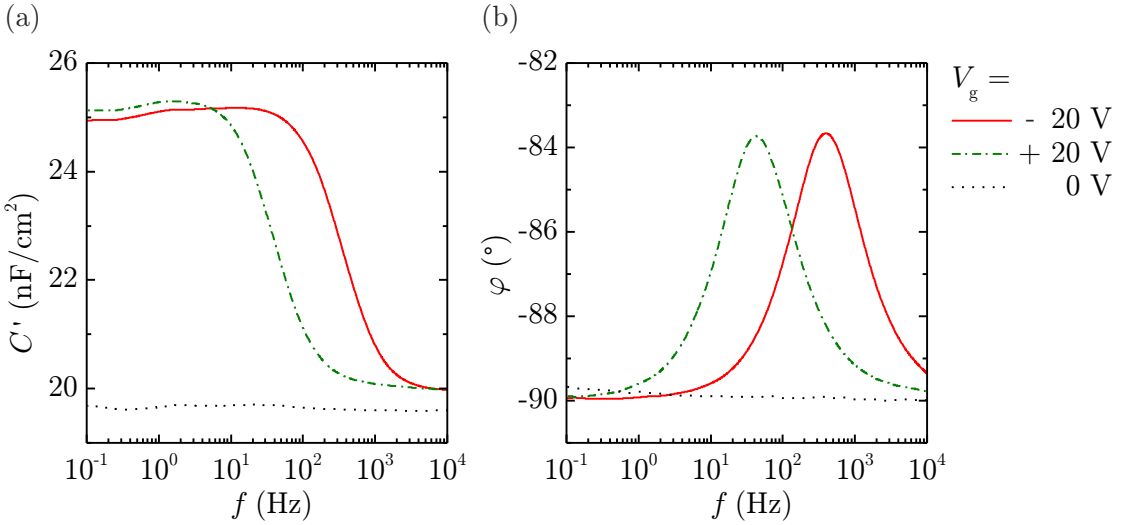


Figure 9.6: (a) $C'(f)$ curves of an MIS diode with 25 nm CuPc on 15 nm as-grown TTC with Au top contacts for hole accumulation (solid line), electron accumulation (dash-dotted line) and depletion (dotted line). (b) Corresponding phase shift to determine the relaxation frequencies.

transport vanishes upon reducing the number of grain boundaries.

An important factor that has to be taken into account is the new crystal phase that is formed on thicker TTC layers. XRD measurements show that the molecular packing of CuPc in this phase is more dense than in the α-phase of CuPc. This effect changes the molecular overlap of π-orbitals between neighboring molecules perpendicular to the substrate and might explain the increased hole mobility in this direction compared to PMMA. However, further experiments like the analysis of a series of different TTC thicknesses would be necessary to clarify this issue.

charge carrier type	doping (cm^{-3})	f_r (Hz)	$\mu_\perp$ (diffusion approach) (cm^2/Vs)
holes	1.8×10^{17}	380	5.8×10^{-7}
electrons	2.5×10^{17}	45	6.9×10^{-8}

Table 9.3: Characteristic parameters of the MIS diode from figs. 9.5 and 9.6.

9.3 Summary

MIS diodes with CuPc as active layer have been discussed in this chapter. These devices are suitable to measure charge carrier transport properties perpendicular to the dielectric-semiconductor interface and are an important supplement to FETs. In analogy to the results shown in chapter 6, the type of injected charge carriers can be controlled by the work function of the top electrode. MIS diodes with a Au electrode exhibit ambipolar charge carrier injection, whereas diodes with Ca or F_4TCNQ/Au contacts show unipolar n- or p-type behavior, respectively. Charge carrier mobilities in MIS diodes are in the range of $10^{-8}\,cm^2/Vs$ and thus four to five orders of magnitude below transistor mobilities. This high anisotropy is predicted by DFT calculations and is caused by a larger layer spacing of the CuPc molecules perpendicular to the substrate plane than parallel to it, leading to a reduced electronic overlap. The asymmetry between electron and hole mobility vanishes in MIS diodes with PMMA passivation layer which can be attributed to the fact that the average CuPc grain size is larger than the thickness of the semiconductor layer. Consequently, the number of grain boundary traps, which predominantly affect electron transport, is by a factor of 1000 lower than along the channel in a transistor. Surprisingly, hole mobility in MIS diodes with TTC passivation layer is one order of magnitude higher although the grain size in the perpendicular direction is not supposed to change. A possible explanation for this effect could be the new CuPc phase which features a closer packing and thus an enhanced molecular overlap in the vertical direction.

Chapter 10

Modeling of charge carrier transport

At the beginning of this chapter two models for charge carrier transport in polycrystalline field-effect devices will be discussed. Both models account for polycrystalline semiconductor layers and include various parameters that affect the electronic properties of the devices like threshold voltage, grain boundaries, trap densities etc.. Thereafter, a technique will be presented that allows for the determination of the energetic distribution of the density of trap states. Subsequently, it will be shown with the help of simulations that the parameters mentioned above can account for the deviations from ideal characteristics observed in our experiments. The analytical model discussed in sec. 2.2.2 will be used to simulate OFET characteristics. Finally, fits of our OFET and MIS data are performed to determine quantitative numbers for these parameters to find possible reasons for the asymmetries between electron and hole transport.

10.1 Models for charge carrier transport in polycrystalline organic films

10.1.1 Grain boundary trap density model by Levinson

The first model that is presented here has been developed in 1982 by Levinson *et al.* for polycrystalline inorganic semiconductors [153]. This model allows for an estimation of the grain boundary trap density and has already been applied successfully to organic semiconductors [30].

Polycrystalline models are based on the assumption that the charge carrier transport process can be separated into two contributions as already discussed in fig. 2.3: a high-mobility transport within defect-free grains (which can even be band-like in some cases) and a thermally activated, low-mobility transport across the grain boundaries. Furthermore, all defects are supposed to be located at the grain boundaries [25]. Levinson *et al.* describe the polycrystalline film as a series of crystallites with grain size l_G and a trap concentration N_t per unit area at the grain boundaries. Since the *intra*-grain mobility is drastically higher than the *inter*-grain mobility, the total charge carrier transport can be considered as determined by the latter. Hence, the total mobility is thermally activated following the law

$$\mu = \mu_0 \cdot \exp\left(-\frac{E_\mathrm{b}}{k_\mathrm{B}T}\right), \tag{10.1}$$

where E_b denotes the energy barrier at the grain boundaries and μ_0 a mobility prefactor. According to several models describing charge carrier transport in polycrystalline inorganic semiconductors, thermionic emission is the dominant transport mechanism over the barriers [154, 155]. An expression for E_b is derived with the help of these assumptions:

$$E_\mathrm{b} = \frac{e^2 N_\mathrm{t}^2}{8\varepsilon_\mathrm{s}\varepsilon_0(N'_\mathrm{d} + N_\mathrm{g}/t)}, \tag{10.2}$$

with ε_s being the dielectric constant of the semiconductor, N'_d the doping concentration per unit volume, N_g the gate-bias accumulated charge carrier density per unit area and t the thickness of the channel. The thickness is assumed to be two molecular layers [156], leading to $t = 2.4\,\mathrm{nm}$ in the case of α-phase CuPc. N_g can be calculated by

$$N_\mathrm{g} = \frac{C'\,(V_\mathrm{g} - V_\mathrm{so})}{e}, \tag{10.3}$$

with the specific insulator capacitance C', the gate voltage V_g and the switch-on voltage V_so. The Levinson analysis is usually done at an effective gate voltage of $|V_\mathrm{g} - V_\mathrm{so}| = 20\,\mathrm{V}$. For a typical value of $C' = 10^{-4}\,\mathrm{F/m^2}$, one can thus calculate an accumulated charge carrier density of $N_\mathrm{g}/t = 5.2 \times 10^{18}\,\mathrm{cm^{-3}}$. This is more than one order of magnitude higher than the doping concentrations N'_d determined in sec. 9.2. Hence, N'_d will be neglected in the following. Using eqs. 10.2 and 10.3, the mobility in eq. 10.1 can be written as

$$\mu = \mu_0 \cdot \exp\left(-\frac{e^3 N_\mathrm{t}^2\, t}{8\varepsilon_\mathrm{s}\varepsilon_0\, C'\, k_\mathrm{B}T\,(V_\mathrm{g} - V_\mathrm{so})}\right). \tag{10.4}$$

The drain current in the linear regime is given by

$$I_\mathrm{d} = \frac{WC'}{L}\,\mu\,V_\mathrm{d}\;(V_\mathrm{g} - V_\mathrm{so})\,, \tag{10.5}$$

which results in

$$I_\mathrm{d} = \frac{WC'}{L}\,\mu_0\,V_\mathrm{d}\,(V_\mathrm{g} - V_\mathrm{so}) \cdot \exp\left(-\frac{e^3 N_\mathrm{t}^2\,t}{8\varepsilon_\mathrm{s}\varepsilon_0\,C'\,k_\mathrm{B}T\,(V_\mathrm{g} - V_\mathrm{so})}\right). \tag{10.6}$$

Finally, one plots the following relation as a function of $1/\,(V_\mathrm{g} - V_\mathrm{so})$:

$$\ln\left(\frac{I_\mathrm{d}}{V_\mathrm{g} - V_\mathrm{so}}\right) = \ln\left(\frac{WC'\,\mu_0\,V_\mathrm{d}}{L}\right) - \frac{e^3 N_\mathrm{t}^2\,t}{8\varepsilon_\mathrm{s}\varepsilon_0\,C'\,k_\mathrm{B}T} \cdot \frac{1}{V_\mathrm{g} - V_\mathrm{so}}. \tag{10.7}$$

By fitting a series of transfer curves measured at different temperatures with eq. 10.7, the trap density N_t can be extracted.

10.1.2 Polycrystalline model by Horowitz

Horowitz *et al.* applied an alternative polycrystalline model to estimate the energy barrier at the grain boundaries E_b with the help of temperature dependent transistor measurements. The model is based on thermionic emission and follows an approach developed by van Heek *et al.* for CdSe thin-film transistors [25, 157]. As in eq. 10.1, the mobility is considered to be thermally activated and an expression for the mobility prefactor μ_0 is derived, which is temperature-dependent in this model:

$$\mu(T) = \mu_0(T) \cdot \exp\left(-\frac{E_\mathrm{b}}{k_\mathrm{B}T}\right), \tag{10.8}$$

$$\text{with} \quad \mu_0(T) = \frac{e\,\langle v\rangle\,l_\mathrm{G}}{8k_\mathrm{B}T}.$$

Here, $\langle v\rangle$ denotes the mean charge carrier drift velocity and l_G the average grain size. For the analysis, transistor curves are measured for various temperatures and the mobilities are plotted as a function of temperature. By fitting the resulting graph with eq. 10.8, parameters for $\langle v\rangle \cdot l_\mathrm{G}$ and E_b can be obtained.

In contrast to the models presented in 10.1.1 and 10.1.3, this model is not restricted to the description of FETs but can also be applied to charge carrier transport perpendicular to the dielectric-semiconductor interface since no transistor-specific equations are used.

10.1.3 Analysis by Lang

Recently, Kalb *et al.* presented a comprehensive study where several analysis techniques were applied to describe the density of trap states in polycrystalline pentacene TFTs [26]. In the following, the technique developed by Lang *et al.* that can

be applied easily to analyze our devices will be discussed briefly. Details about this model can be found in literature [26,158]. The model is based on the calculation of the trap density from the temperature-dependence of the transistor characteristics. Therefore, transfer characteristics in the linear regime are measured for a set of different temperatures. The gate voltage-dependent field-effect conductivity σ is calculated for each temperature:

$$\sigma(V_\mathrm{g}) = \frac{L \cdot I_\mathrm{d}}{W \cdot V_\mathrm{d}}. \tag{10.9}$$

This parameter is considered to be thermally activated following the law

$$\sigma(V_\mathrm{g}, T) = A \cdot \exp\left(-\frac{E_\mathrm{a}}{k_\mathrm{B}T}\right), \tag{10.10}$$

with the conductivity prefactor A and the difference between Fermi energy and band edge E_a. Subsequently, E_a is determined by an Arrhenius plot of eq. 10.10. Finally, the trap density per unit volume and energy $N(E_\mathrm{a} = E)$ is calculated via

$$N(E) = \frac{C'}{e \cdot t}\left(\frac{\mathrm{d}E_\mathrm{a}}{\mathrm{d}V_\mathrm{g}}\right)^{-1}. \tag{10.11}$$

Here, t denotes the thickness of the channel. As before, a value of $t = 2.4\,\mathrm{nm}$ is assumed in our case.

10.2 Simulation of transistor curves

The models discussed above describe charge carrier transport in polycrystalline organic semiconductors. Several parameters that account for deviations from ideal characteristics are included in these models, namely contact resistance, grain boundary traps or thermally activated mobilities. The influence of these parameters on the device characteristics will be shown in the following. Simulations of OFET transfer curves are carried out using the general ambipolar theory described by eqs. 2.25 (a) and (b). The model is extended to include contact resistances and charge carrier mobilities determined by grain boundary traps as defined by the Levinson model in eq. 10.4. Typical transfer characteristics in the linear regime for different values of R_c are displayed in fig. 10.1(a). As already discussed in sec. 3.1.2, the contact resistance is responsible for a downward bending of the transfer curve at high gate voltages. This is due to the reduction of the effective drain voltage $V_\mathrm{d,eff} = V_\mathrm{d} - R_\mathrm{c}I_\mathrm{d}$ (see eq. 3.8) which becomes dominant for high currents.

The grain boundary trap density N_t has a strong influence on the electrical characteristics of the device as can be seen in fig. 10.1(b). Here, OFET characteristics

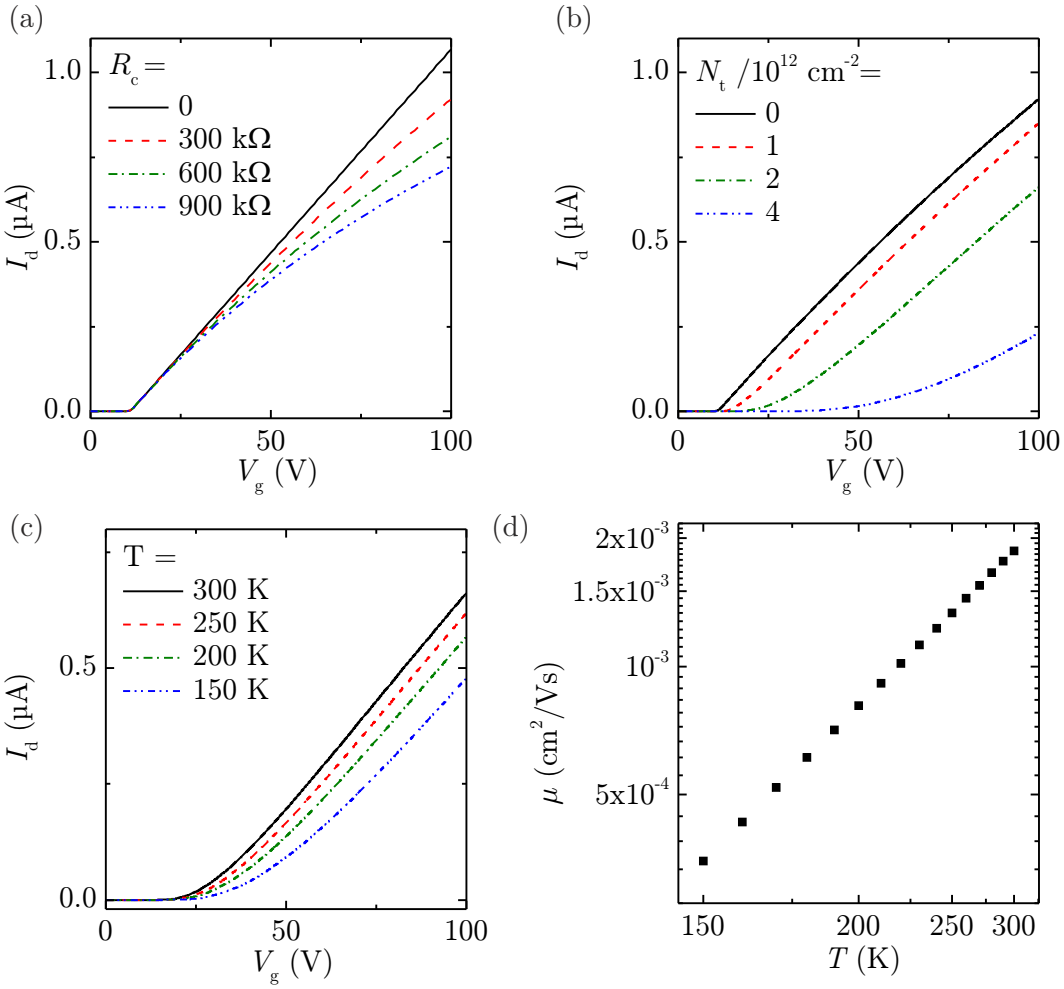


Figure 10.1: Simulations of OFET characteristics with the help of eqs. 2.25 (a) and (b) extended by contact resistance. Charge carrier mobility is considered to be limited by grain boundary traps as defined in eq. 10.4. Device parameters are $L = 50\,\mu\text{m}$, $W = 3.0\,\text{mm}$, $V_d = 2\,\text{V}$, $C_i = 1.0 \times 10^{-4}\,\text{F/m}^2$, $V_t = 10\,\text{V}$ and $\mu_0 = 0.01\,\text{cm}^2/\text{Vs}$. (a) Dependence of the drain current on the contact resistance R_c for a grain boundary trap density $N_t = 0$ and a temperature of $T = 300\,\text{K}$, (b) dependence of I_d on N_t for $R_c = 300\,\text{k}\Omega$ and $T = 300\,\text{K}$, (c) dependence of I_d on T for $R_c = 300\,\text{k}\Omega$ and $N_t = 2 \times 10^{12}\,\text{cm}^{-2}$ and (d) temperature dependence of the charge carrier mobility for the device shown in (c).

are plotted for different values of N_t. The dominant effect of the traps is the appearance of a pronounced curvature at low gate voltages that causes a considerable reduction of the drain current. This curvature leads to problems when determining the threshold voltage. Although the nominal value $V_t = 10\,V$ is used for all simulations, linear fits of the transfer curves lead to significantly differing values. For instance, one obtains $V_t = 30\,V$ by a linear fit of the curve with $N_t = 2 \times 10^{12}\,cm^{-2}$. Hence, the presence of trap states complicates the extraction of parameters from transistor curves.

Since hopping across grain boundaries is a thermally activated process, the charge carrier mobility decreases with decreasing temperature following eq. 10.4 in the Levinson model. Simulated transfer curves for different temperatures are shown in fig. 10.1(c) and the corresponding mobilities in an Arrhenius plot in (d) to demonstrate the thermally activated charge carrier transport.

These simulations are useful tools to understand the experimentally determined transfer characteristics. In the following the models presented in sec. 10.1 will be applied to the experimental data.

10.3 Fits of experimental data

10.3.1 Fits with Levinson model

Fig. 10.2 depicts transfer characteristics of a CuPc OFET with a passivation layer of 14 nm annealed TTC for three different temperatures. The device exhibits a clear thermally activated charge carrier transport with decreasing currents upon decreasing temperature. Comparing the curves to the simulations shown in fig. 10.1, the influence of contact resistance is observable for hole transport by a downward-bending of the transfer curves. The effect of contact resistance for electron transport cannot be seen from the transfer curves because these curves are superimposed by the strong curvature at low currents which are a sign for trap states.

In order to classify the influence of these trap states, the Levinson model is applied to three different devices (passivation layers of PMMA, 14 nm and 28 nm annealed TTC). As described in sec. 10.1.1, $I_d/(V_g - V_{so})$ is plotted logarithmically as a function of $1/(V_g - V_{so})$ and fitted using eq. 10.6. The experimental data are displayed in fig. 10.3 and the results of the fits are given in table 10.1.

Trap densities for electrons are generally higher than those for holes. This result is in agreement with the transfer curves displayed in fig. 10.2, which show a pronounced curvature in the electron transport regime. The fact that both TTC-

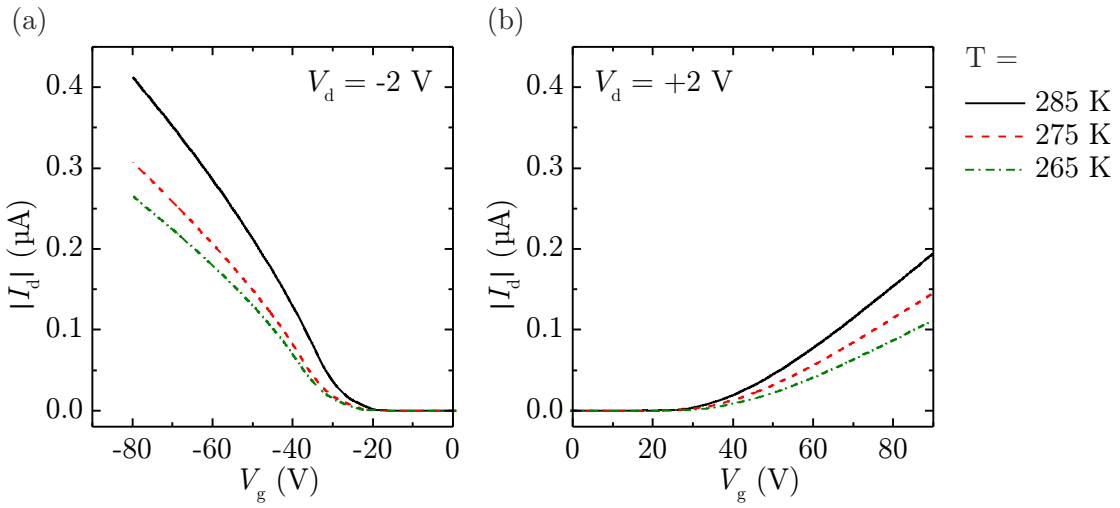


Figure 10.2: Transfer characteristics of a CuPc OFET with a passivation layer of 14 nm annealed TTC, $L = 70\,\mu m$ and $W = 3.0\,mm$ for three different temperatures.

passivated samples can be fitted with a common trap density for electrons and a common trap density for holes and that the corresponding values of the PMMA-passivated devices are only slightly higher leads to the conclusion that the trap density does not depend predominantly on the grain size of the polycrystalline layers but rather on the type of charge carrier. A large asymmetry between electron

T (K)	holes		electrons	
14 nm TTC	μ_0 (cm^2/Vs)	$N_{t,ho}$ (cm^{-2})	μ_0 (cm^2/Vs)	$N_{t,el}$ (cm^{-2})
285	1.1×10^{-2}	1.4×10^{12}	5.6×10^{-3}	2.3×10^{12}
275	8.1×10^{-3}		4.2×10^{-3}	
265	7.2×10^{-3}		3.1×10^{-3}	
28 nm TTC				
285	1.1×10^{-2}	1.4×10^{12}	7.2×10^{-3}	2.3×10^{12}
275	9.0×10^{-3}		5.8×10^{-3}	
265	6.9×10^{-3}		4.0×10^{-3}	
PMMA				
280	1.5×10^{-3}	1.7×10^{12}	2.5×10^{-4}	2.7×10^{12}
267	9.0×10^{-4}		1.1×10^{-4}	
252	8.2×10^{-4}		7.8×10^{-5}	

Table 10.1: Characteristic parameters of the devices shown in fig. 10.3 determined by fits with the Levinson model.

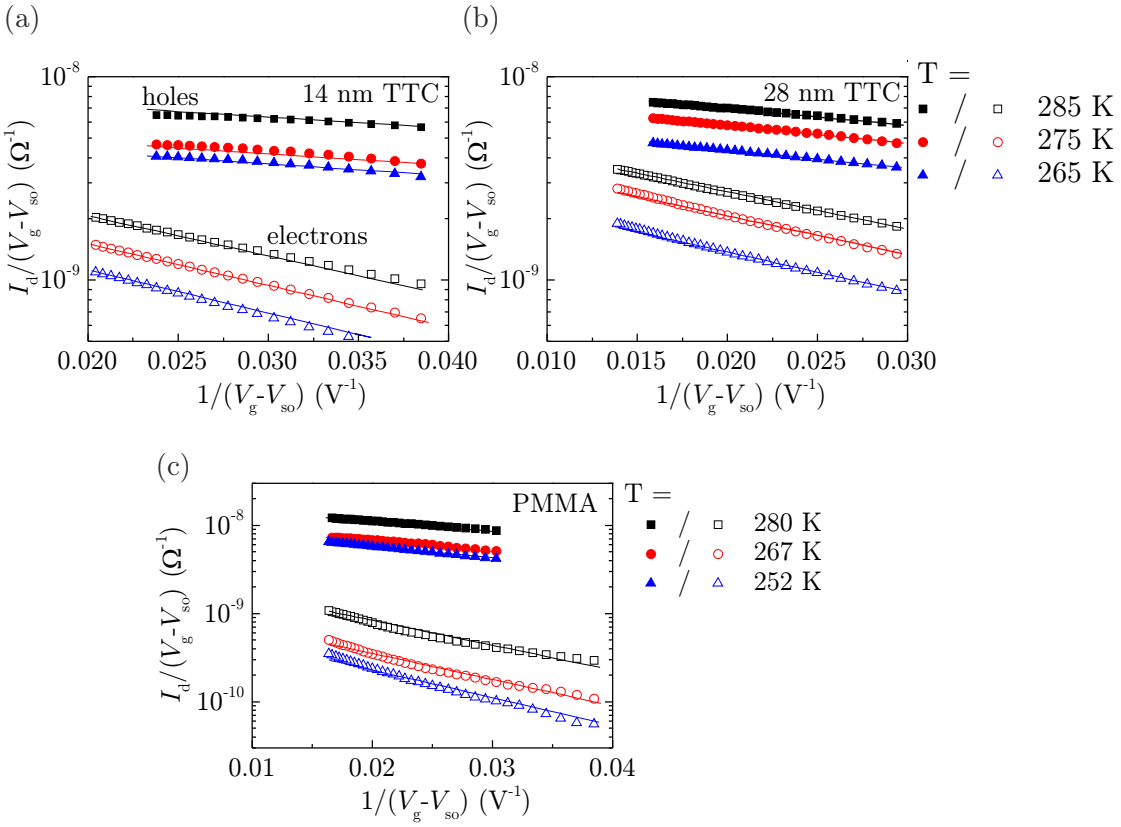


Figure 10.3: Analysis of transfer characteristics in the linear regime of three CuPc OFETs for various temperatures with the Levinson model. Passivation layers are (a) 14 nm annealed TTC, (b) 28 nm annealed TTC and (c) PMMA. Devices (a) and (b) are fabricated using layout 2 (see sec. 4.2.1), whereas device (c) features layout 1. The closed symbols stand for hole transport whereas the open symbols for electron transport. The lines are fits of the data using the Levinson model.

and hole mobility is observed for the PMMA-passivated OFET. This asymmetry is significantly reduced for the TTC-passivated devices. Highest charge carrier mobilities are determined for the 28 nm TTC layer, which is in good agreement with the data shown in chapters 7 and 8. This result suggests that the difference in grain boundary trap density cannot be the only effect contributing to the asymmetry between electron and hole transport depending on the TTC thickness as discussed in sec. 8.2. Hence, other effects, like polaronic interactions between the charge carriers in the organic semiconductor and induced polarization in the insulator or interface traps at the oxide surface must also have a strong influence.

In summary, it can be stated that fits with the Levinson model show that there is a

systematic difference between electron and hole transport but they cannot explain the difference between the individual transport regimes observed for annealed TTC layers in sec. 8.2. Contact resistances, which have considerable influence on the transfer characteristics especially for high gate voltages, are not considered in the Levinson model.

10.3.2 Fits with Horowitz model

The model for charge carrier transport in polycrystalline organic semiconductors by Horowitz *et al.* presented in sec. 10.1.2 is applicable both for FET and MIS data since no transistor-specific equations are used. Fig. 10.4 depicts charge carrier mobilities as a function of measurement temperature for OFETs and MIS diodes on as-grown TTC and on PMMA. OFETs and MIS diodes are fabricated on the same substrate for both cases to exclude deviations due to different fabrication conditions. A monotonic decrease of mobility with decreasing temperature is observed for all transport processes. This is an evidence for thermally activated hopping transport. FET-mobilities reflect the results already discussed in chapters 6 and 7 with higher mobilities for TTC-passivated OFETs than for PMMA as passivation layer. As already discussed in chapter 9, charge carrier mobilities perpendicular

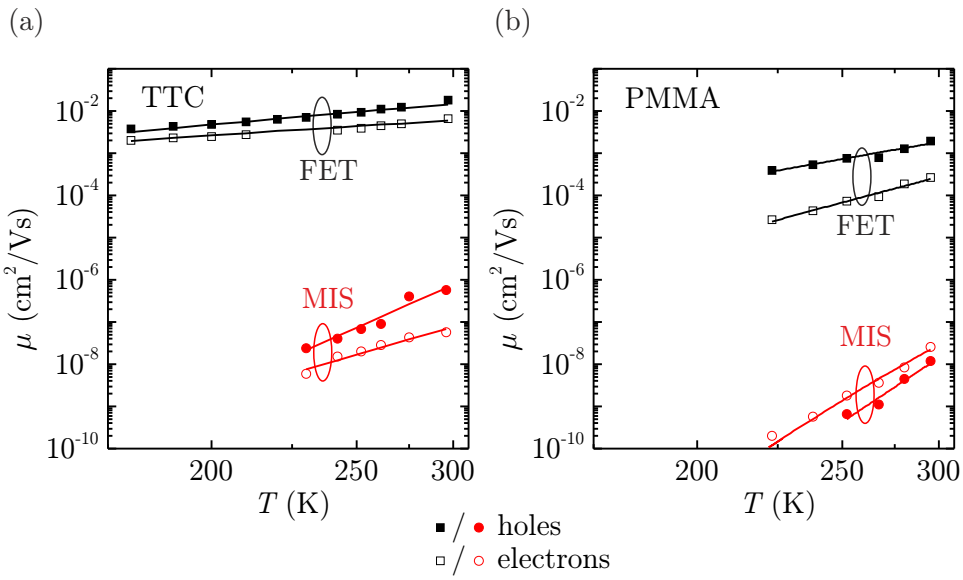


Figure 10.4: Charge carrier mobilities as a function of measurement temperature for OFETs and MIS diodes fabricated on one substrate. Passivation layer is (a) 10 nm non-annealed TTC and (b) PMMA. The solid lines are fits with the model by Horowitz *et al.* for polycrystalline organic semiconductors.

to the substrate-semiconductor plane are several orders of magnitude lower than parallel to it. The asymmetry between hole and electron transport is pronounced in FETs with PMMA passivation layer, whereas it is significantly reduced in FETs with TTC passivation layer and MIS diodes with PMMA. This behavior was attributed to the high number of grain boundaries which charge carriers have to cross and differing polaronic interactions in FETs with PMMA.

The mobility data is fitted using eq. 10.8 to extract the energy barrier at the grain boundaries (solid lines in fig. 10.4). The results of the fits are given in table 10.2. The most pronounced difference is the significantly higher energy barrier for MIS diodes than for OFETs. This effect might be caused by the lower molecular overlap perpendicular to the substrate than parallel to it, which hinders an efficient charge carrier transport. It is additionally noticeable that the TTC-passivated device exhibits lower values for E_b than the PMMA-passivated transistor. This can be attributed to a more "band-like" charge carrier transport behavior for CuPc on TTC than on PMMA due to less grain boundaries. Comparing the energy barriers for electron and hole transport, no clear tendency can be observed but they are of the same order of magnitude in each case. This might be an indication that there is no profound electronic difference between electron and hole transport in CuPc besides extrinsic trap states or polaronic effects.

This model does not account for the fact that the thickness of the CuPc layer is smaller than the average grain size which implies that there are practically no grain boundaries in perpendicular direction. For a comprehensive study, this parameter would have to be included.

	TTC, FET	TTC, MIS	PMMA, FET	PMMA, MIS
$E_{\mathrm{b,h}}$ (meV)	80	330	140	480
$E_{\mathrm{b,e}}$ (meV)	63	220	205	400

Table 10.2: Energy barrier at the grain boundaries for holes and electrons determined from the fits in fig 10.4.

10.3.3 Determination of the density of trap states

The technique by Lang *et al.* is applied to the temperature dependent data of CuPc OFETs with passivation layers of PMMA and 14 nm and 28 nm annealed TTC discussed in sec. 10.3.1. The calculated distributions of localized states in the band gap are depicted in fig. 10.5. The hole trap densities—displayed in (a)—are almost equal for all samples. Comparing the electron trap densities—shown in

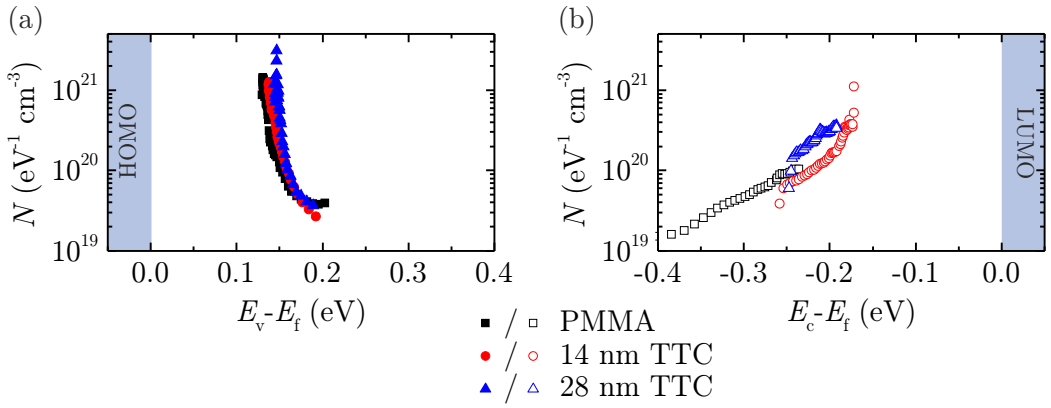


Figure 10.5: Densities of trap states determined with the technique by Lang *et al.* for holes (a) and electrons (b).

(b)—the trap distribution of the PMMA-passivated device extends further into the band gap, whereas both TTC-passivated transistors exhibit similar values.

A problematic issue of the calculated trap DOS are the large gaps between the edges of HOMO and LUMO and the first data points. Due to the limited measured gate voltage range, no data are available for these gap regions. It would be necessary to know the density of states within the HOMO and the LUMO to be able to interpret the data correctly. Kalb *et al.* determined trap densities at the valence band edge in pentacene thin films of $2 \times 10^{21}\,\mathrm{eV^{-1}cm^{-3}}$ with the same technique that is applied here [26]. Assuming that the DOS in CuPc is of the same order of magnitude, this could lead to two different possible scenarios depicted in fig. 10.6(a) and (b). On the one hand the large gap could be an artifact of the analysis method because the maximum of the calculated DOS is already $N \approx 2 \times 10^{21}\,\mathrm{eV^{-1}cm^{-3}}$. In this case, the determined data points correspond to the band tails directly next to the HOMO and LUMO, as illustrated schematically for the HOMO band tail in fig. 10.6(a). The LUMO band tail can be treated in the same way. This results in a higher depth of the electron trap distribution. Another possible interpretation is shown in (b). Here, the calculated data points could correspond to a maximum of trap states within the band gap.

The comparison of our results with the work of Celebi *et al.* even allows for a third interpretation. Celebi *et al.* determined the density of states in *p*-type CuPc thin films by Kelvin probe force microscopy [159]. Their key results are depicted schematically in fig. 10.6(c). They observed an exponential band tail further away from the band edges and, as in our case for the HOMO band tails, a strong, non-exponential increase. Due to the comparison of devices with different channel lengths they were able to show that this increase is an artifact due to non-uniform

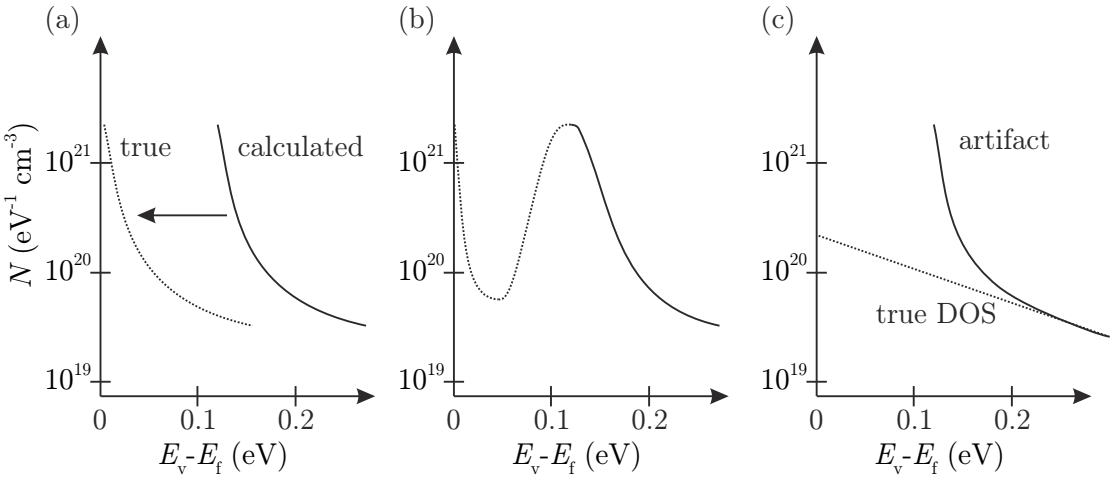


Figure 10.6: Different interpretations of the calculated trap DOS. Assuming a DOS of $N \approx \times 10^{21}\,\mathrm{eV}^{-1}\mathrm{cm}^{-3}$ at the band edge [26], the experimental data could be shifted along the horizontal axis due to an artifact of the analysis technique (a) or a maximum of trap states could be located in the band gap (b). A comparison of our results to data obtained by Celebi *et al.* leads to the assumption that the calculated strong increase could be an artifact and the true DOS follows and exponential dependence (c) [159].

channel potentials. The true DOS is given by the exponential part of the tail with a characteristic energy of 0.11 eV over a range of 0.5 eV and a trap density at the HOMO edge of $N \approx 10^{20}\,\mathrm{eV}^{-1}\mathrm{cm}^{-3}$ were obtained. This model would also be in agreement with our data and could be applied to both HOMO and LUMO band tails. However, due to the lack of comparable data for the trap DOS in CuPc and for higher gate voltages, it is not possible to investigate which of these models could be correct.

While these results can explain the high asymmetry between hole and electron transport, they cannot explain the differences between both TTC-passivated devices. A possible reason could be the fact that a TTC thickness of 14 nm is already at the upper limit of transport regime II and hence, the differences between both samples are expected to be small (see fig. 8.8). It also remains unclear why the large variations of the CuPc grain size are not reflected in different densities. Nevertheless, the results demonstrate again that charge carrier traps are not the only factor contributing to the differences between the individual passivation layers and to the asymmetries between hole and electron transport. Further effects, like polaronic interactions discussed in sec. 8.2.2, must also have a major influence.

10.4 Summary

This chapter focused on the examination of the physical origin of the measured transistor characteristics and charge carrier transport phenomena. At the beginning, several models that have been developed by various groups were introduced which describe charge carrier transport in polycrystalline organic TFTs. These models are based on the assumption that the transport is predominantly limited by localized trap states. The density of these traps is determined by analyzing the temperature dependence of transfer curves. A different model that can also be applied to MIS-diodes allows for the extractions of the energy barrier at the grain boundaries.

Subsequently, it was shown by simulations how contact resistance, charge carrier traps and varying temperature can affect the transistor characteristics. These simulations helped to interpret the FET measurements.

In the third part of this chapter the models were applied to the experimental data of various CuPc OFETs on PMMA and TTC. Comparing these models, it can be stated that there is no clearly preferential analysis technique. All show the same tendency that the trap density for electrons is higher than for holes. However, as known from the dependence of the charge carrier mobilities on the TTC thickness, additional effects are present which cannot be analyzed with these models. Kalb *et al.* concluded that the only useful method to solve this problem are computer simulations [26]. They used a simulation program that calculates transfer characteristics from a given trap density of states using Fermi-Dirac statistics. Subsequently, this density is varied until an agreement between the experimental and calculated transistor curves is reached. This method yields the best results because no simplifying assumptions—like a temperature-independent Fermi energy—are made.

A serious problem concerning the analysis of the transistor data with the Levinson model and the technique by Lang is the fact that the contact resistance is neglected. This problem could be solved by four point measurements where the current is measured independently of the applied voltage.

Chapter 11

Organic Inverters

11.1 Working principles

Inverters are basic devices for the realization of logic electronic circuits. They are used to perform a logic negation of an applied input signal and are consequently also referred to as "NOT gate". There are several electronic implementations, the complementary metal oxide semiconductor (CMOS) inverter being the most important one. A CMOS inverter, shown schematically in fig. 11.1(a), consists of two transistors, one n-type (with source S1 and drain D1) and one p-type (with source S2 and drain D2), with a common gate electrode connected to the input voltage V_{in}. The source electrode S2 of transistor 2 is grounded. The drain electrode of the first transistor D1 is connected to the drain electrode of the second transistor D2. These two electrodes are connected to the output voltage V_{out}. When a constant supply voltage V_{DD} is applied to the source S1 of transistor 1, the output voltage is measured as a function of the input voltage V_{in}. Two cases demonstrating that the output signal is the inversion of the input signal are relevant will be described in the following. Here, a constant supply voltage of $V_{\mathrm{DD}} = -90\,\mathrm{V}$ is assumed:

(i) When the input voltage is $V_{\mathrm{in}} = 0\,\mathrm{V}$, as sketched in fig. 11.1(b), the voltage drop between electrode S1 and the gate is $+90\,\mathrm{V}$. Consequently, electrons are accumulated in the n-type transistor, whereas the p-type transistor is depleted. A conducting channel between S1 and D1 is formed. Hence, D1 and D2 are on the same potential as S1. Thus, the measured output voltage

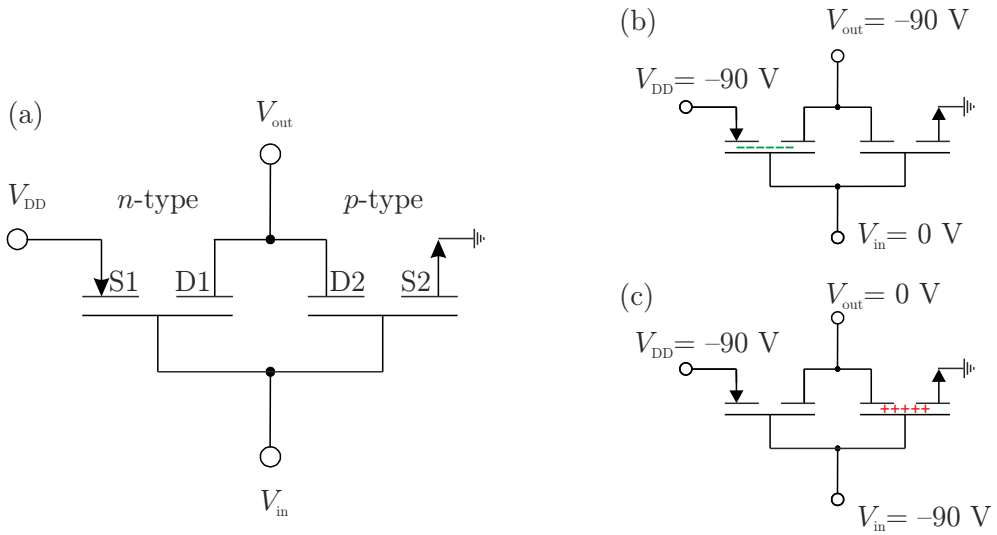


Figure 11.1: (a) Circuit diagram of a complementary inverter. S1 and D1 denote source and drain of transistor 1, S2 and D2 denote the respective contacts of transitor 2. (b) and (c) Inversion (V_{out}) of the input signal V_{in} at a constant supply voltage $V_{DD} = -90\,V$.

is $V_{out} = V_{DD} = -90\,V$.

(ii) For an input voltage of $V_{in} = V_{DD} = -90\,V$, as sketched in fig. 11.1(c), the n-channel FET is depleted because S1 and the gate are on the same potential and the p-channel FET is switched on. Thus, D2 and S2 are connected by a conducting channel and the measured output signal is $V_{out} = 0\,V$.

Inverters are fabricated with two different layouts in analogy to the OFET layouts described in sec. 4.2.1. The inverter configuration of layout 1, which is characterized by an unstructured CuPc layer, is depicted in fig. 11.2(a). Here, two neighboring OFETs with identical channel lengths form the inverter and V_{out} is measured at the common center electrode. Layout 2, drawn in fig. 11.2(b), comprises two separate OFETs where two electrodes are connected.

Inorganic complementary inverters are realized by the fabrication of a p-doped and an n-doped transistor on one substrate. In organic electronics, this complex patterning of the semiconductor layer is not necessary because the type of transistor can be controlled by the contact material. Principally, there are two possible realizations for organic inverters: complementary inverters, which consist of one p- and one n-type OFET and ambipolar devices, which consist of two ambipolar OFETs. For ambipolar inverters, contact materials that enable the injection of holes and electrons have to be chosen. Consequently, Au is used for the latter case as known from OFET data discussed in chapters 6 and 7. For complementary

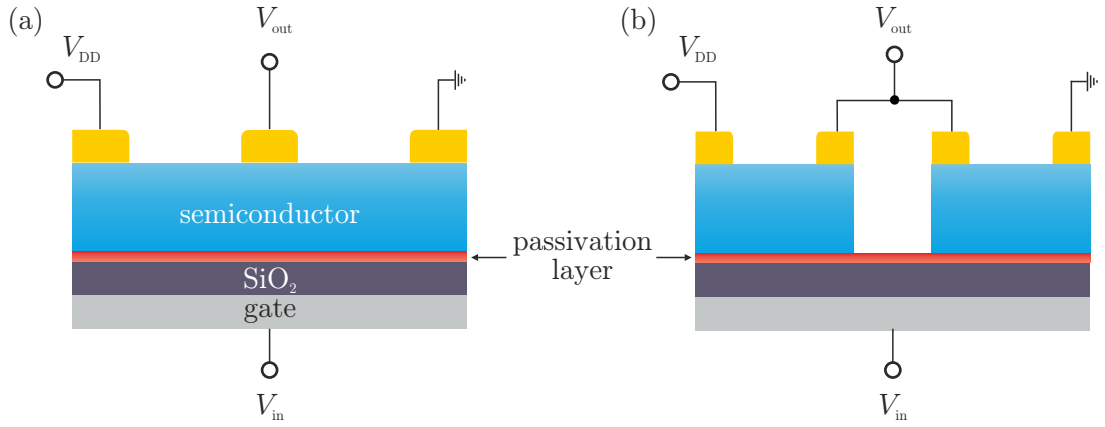


Figure 11.2: Schematic layout of the inverters used for the experiments discussed in this thesis. (a) Layout 1 with unstructured CuPc layer and (b) layout 2 with structured CuPc.

devices, the contacts of one OFET have to provide unipolar hole injection, which is realized by TTF-TCNQ, whereas the contacts of the other OFET have to feature unipolar electron injection, which is implemented by Al contacts.

The simulated characteristics of ideal complementary and ambipolar inverters are displayed in fig. 11.3(a) [111]. For the simulations, one uses eqs. 2.25 both for the *n*-type and the *p*-type FET. The output voltage can be calculated by equalizing both equations since the total drain current is identical in both devices. The

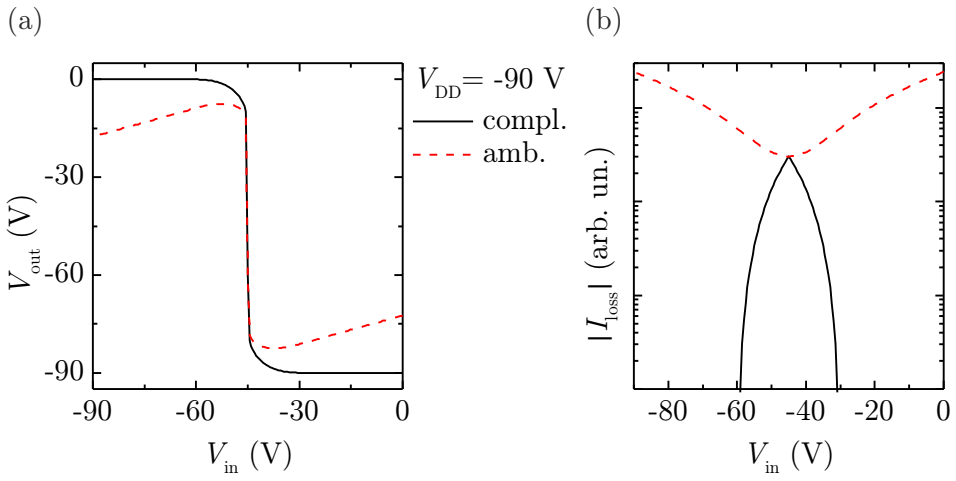


Figure 11.3: (a) Simulated inverter characteristics of a complementary and an ambipolar inverter for a constant supply voltage $V_{DD} = -90\,V$. (b) Loss currents for both cases. The data are replotted from ref. [111].

transistion between both logic states occurs at $V_{\mathrm{in}} = V_{\mathrm{DD}}/2$ in an ideal inverter. The corresponding loss currents are shown in fig. 11.3(b). The ambipolar current increase is suppressed in case of the complementary inverter. Whereas the fabrication of ambipolar inverters is simple, they feature some considerable disadvantages compared to their complementary counterparts. These problems are caused by the ambipolar increase of the drain current for high drain voltages. This effect reduces the switching efficiency as can be seen in fig. 11.3(a), so that neither of both logic states $V_{\mathrm{out}} = V_{\mathrm{DD}}$ and $V_{\mathrm{out}} = 0$ is fully reached. The ambipolar current increase is also reflected in the enlarged loss current displayed in fig. 11.3(b). Due to these two problems, complementary inverters are the preferred devices.

11.2 Experiments

11.2.1 Ambipolar inverters

PMMA as passivation layer

A simple approach for the fabrication of an ambipolar inverter based on CuPc is to connect two neighboring OFETs on one substrate with an unstructured CuPc layer, as shown in fig. 11.2(a). The inverter characteristics of a corresponding device with PMMA passivation layer are drawn in the upper part of fig. 11.4 for negative (a) and positive (b) supply voltages. The output curves are comparable to the simulations in fig. 11.3(a) except for the large hysteresis. This can be attributed to the relatively low supply voltages of $V_{\mathrm{DD,max}} = \pm 50\,\mathrm{V}$. Higher values of V_{DD} would be necessary to obtain better characteristics, as will be seen in the next paragraph. The switching between two regimes with $V_{\mathrm{in}} = V_{\mathrm{DD}}$ and $V_{\mathrm{in}} = 0\,\mathrm{V}$ is observable. However, the transition between both regimes does not occur at $V_{\mathrm{in}} = V_{\mathrm{DD}}/2$ but is shifted significantly towards more positive values of V_{in}. Simulations of inverter characteristics revealed that a higher mobility of holes than of electrons as well as a lower switch-on voltage for hole transport can be responsible for this shift [111]. Indeed, the hole mobility in PMMA-passivated devices is about one order of magnitude higher than the electron mobility as known from transistor measurements presented in chapter 6. The dependence of the loss current on the input voltage, depicted in fig. 11.4(b) agrees well with the simulations with a minimum at the switching point and increasing loss currents further away.

The measurements demonstrate that it is principally possible to construct ambipolar inverters with CuPc on PMMA and Au top contacts but the performance of these devices is limited due to the shift of the transition region, non-constant values

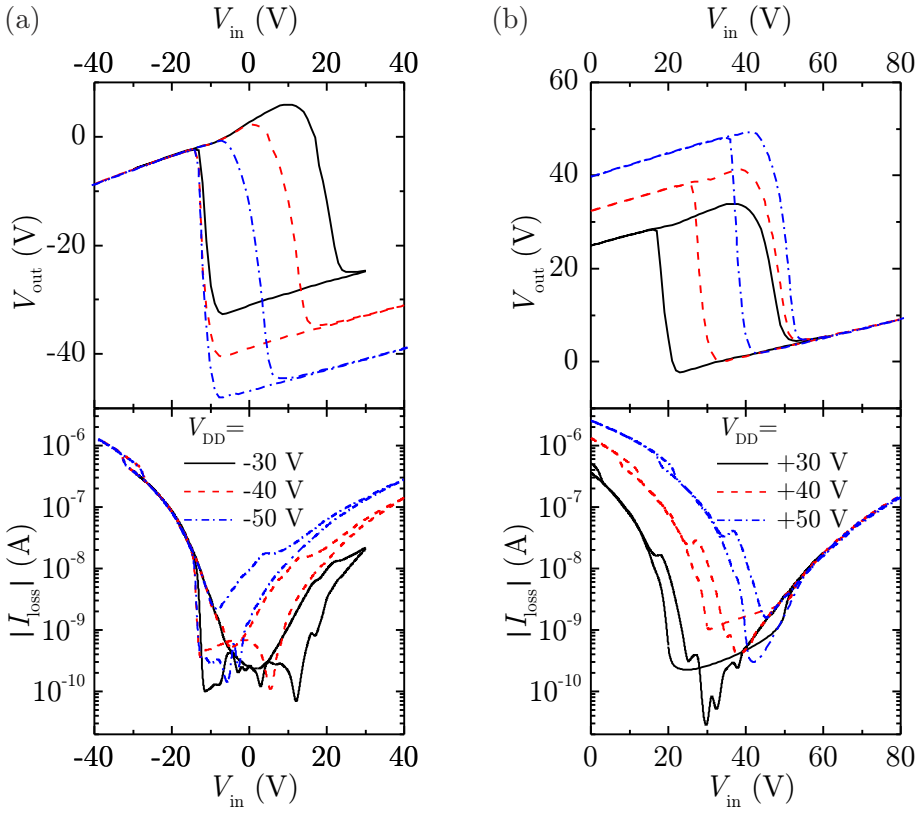


Figure 11.4: Inverter characteristics and loss currents of an ambipolar CuPc inverter with PMMA passivation layer and Au top contacts. The devices are fabricated using layout 1 (see fig. 11.2(a)) with channel lengths of 100 µm. Negative supply voltages are shown in (a), positive in (b).

of V_{out}, large hysteresis and high loss currents.

TTC as passivation layer

In order to minimize the disadvantages caused by asymmetric charge carrier mobilities, TTC is used as passivation layer. The characteristics of an ambipolar inverter with 15 nm annealed TTC and Au top contacts fabricated in layout 2, shown in fig. 11.2(b), are given in fig. 11.5. An important improvement of the device characteristics compared to PMMA as passivation layer can be observed: the transition between both logic states is sharp and occurs close to $V_{in} = V_{DD}/2$. Almost no hysteresis is observable. Nevertheless, typical problems of ambipolar inverters remain: V_{out} does not remain constant for values of V_{in} further away from the transition region and the loss currents are high due to the increase of the transistor currents in the ambipolar regime.

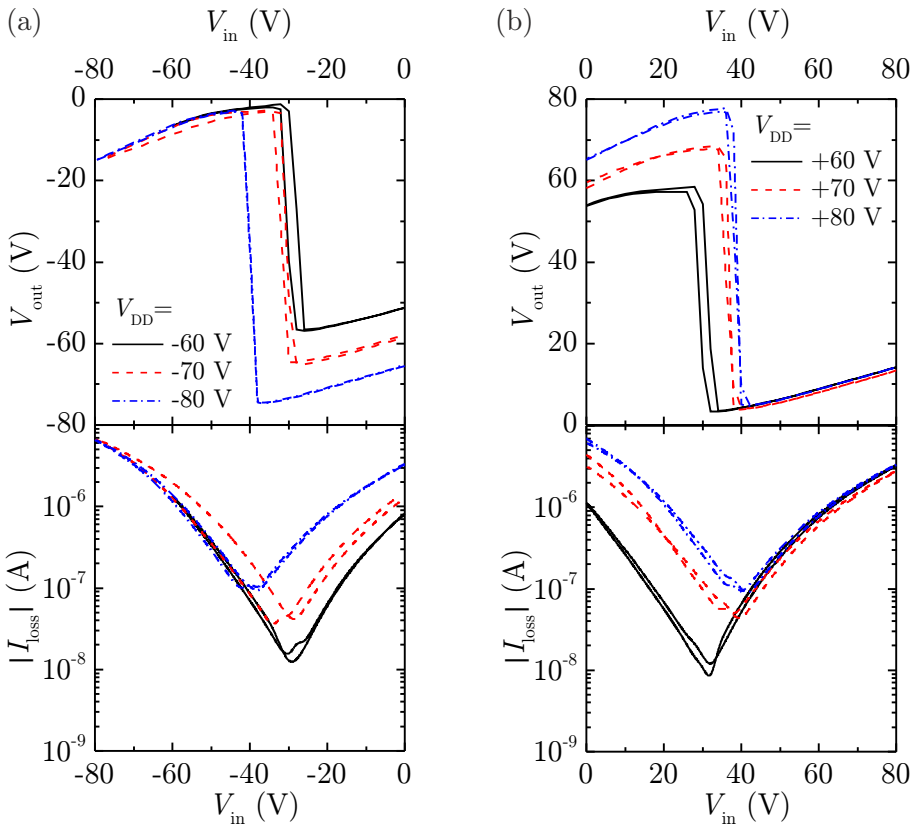


Figure 11.5: Inverter characteristics and loss currents of an ambipolar CuPc inverter with TTC passivation layer and Au top contacts. The devices are fabricated using layout 2 (see fig. 11.2(b)) with channel lengths of 70 µm. Negative supply voltages are shown in (a), positive in (b).

11.2.2 Complementary inverters

In order to achieve a further improvement of the devices, complementary inverters are investigated. Fig. 11.6 depicts the inverter characteristics of a complementary CuPc inverter with 15 nm annealed TTC built in layout 2 (illustrated in fig. 11.2(b)). One OFET is fabricated with Al top contacts, the other one with TTF-TCNQ top contacts. The inverter curves are comparable to ideal, simulated curves. The hysteresis is small and the loss currents are reduced by two orders of magnitude compared to the ambipolar inverter. However, a shift of the transition region from $V_{in} = V_{DD}/2$ towards more positive values is detected. For negative supply voltages, the device features a good switching behavior with stable plateau regions at $V_{out} = 0\,V$ for $V_{in} < V_{DD}/3$ and $V_{out} = V_{DD}$ for $V_{in} > V_{DD}/3$. For positive supply voltages, $V_{out} = 0\,V$ is determined for $V_{in} > 2/3 \cdot V_{DD}$ and $V_{out} = V_{DD}$ for $V_{in} < 2/3 \cdot V_{DD}$. This shift can be attributed to an asymmetry of the switch-on

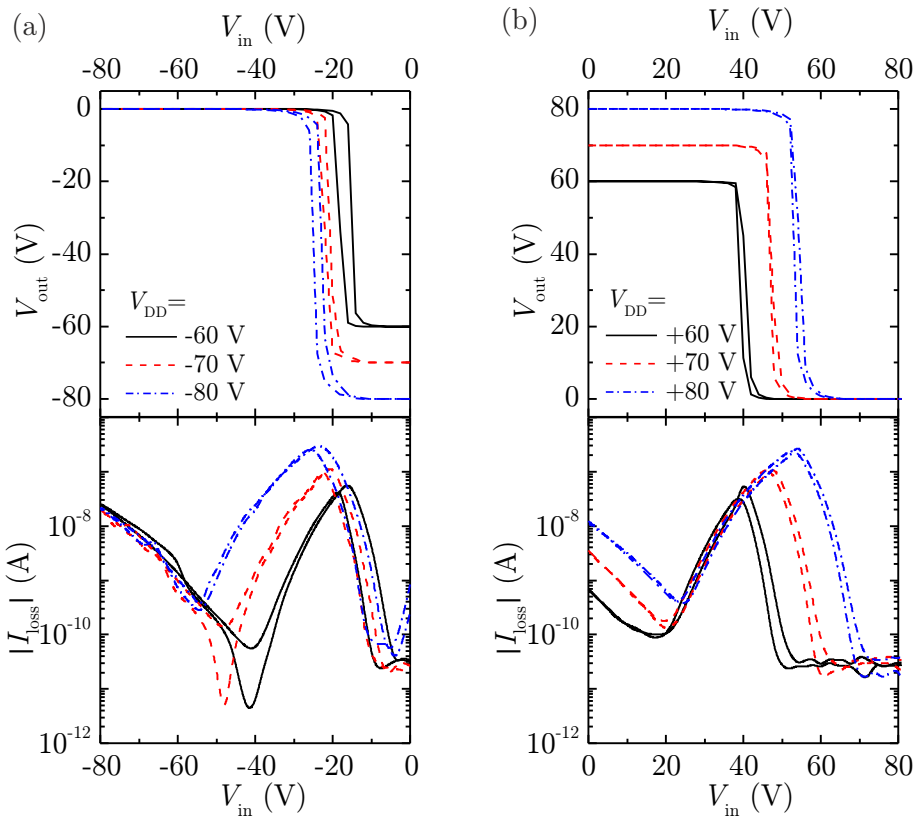


Figure 11.6: Inverter characteristics and loss currents of a complementary CuPc inverter with TTC passivation layer and Al and TTF-TCNQ top contacts. The devices are fabricated using layout 2 with channel lengths of 70 µm. Negative supply voltages are shown in (a), positive in (b).

voltages of the individual OFETs, where TTF-TCNQ features a significantly reduced switch-on voltage as demonstrated in sec. 7.3. This asymmetry does not occur for Au contacts in the case of ambipolar inverters. The increase of the loss current for negative input voltages is caused by a slightly ambipolar behavior of the Al transistor. This device exhibits an increase of the drain current for high negative gate voltages, as already depicted in fig. 7.11.

11.3 Summary

In this chapter it was demonstrated that OFETs with CuPc as active material can be used to fabricate inverters, i.e. logic electronic devices. Two different device types were investigated: ambipolar and complementary inverters. Both classes show clear inversion of the input voltage, but the inverter characteristics of comple-

mentary devices are significantly better than those of ambipolar ones: they feature a clear switching between both logic states, stable output voltages and low loss currents. These results demonstrate the importance of the experiments discussed in chapters 6 and 7 to realize unipolar *p*- and *n*-type OFETs by contact modification as well as balanced charge carrier mobilities by suitable passivation layers as discussed in chapter 8.

Chapter 12

Unipolar *n*-type transistors based on F_{16}CuPc

F_{16}CuPc, the perfluorinated analogue of CuPc, has been introduced in sec. 4.1.2. In the following, the growth and morphology of F_{16}CuPc on SiO_2 will be discussed briefly. Thereafter, transistor measurements of F_{16}CuPc OFETs with PMMA and TTC as passivation layers will be presented. Finally, CuPc OFETs doped with F_{16}CuPc and vice versa will be investigated.

12.1 Morphology

AFM measurements

Fig. 12.1 depicts AFM images of F_{16}CuPc deposited on PMMA (a) and on nominally 15 nm annealed TTC (b) and (c). Round-shaped grains, comparable to the growth of CuPc on PMMA are observed in (a) and elongated crystallites on TTC terraces can be seen in (b) and (c), similar to the case of CuPc on TTC. Typical lateral dimensions of the individual grains are $200\,\mu m \times 50\,\mu m$, which is comparable to the size of CuPc grains for the given TTC thickness. However, the alignment of the crystallites is not as regular as for CuPc and no growth along some preferential directions is observable. It is likely that the different lattice parameters of F_{16}CuPc are responsible for these deviations. Nevertheless, TTC is suitable to obtain polycrystalline F_{16}CuPc films with grain sizes comparable to CuPc.

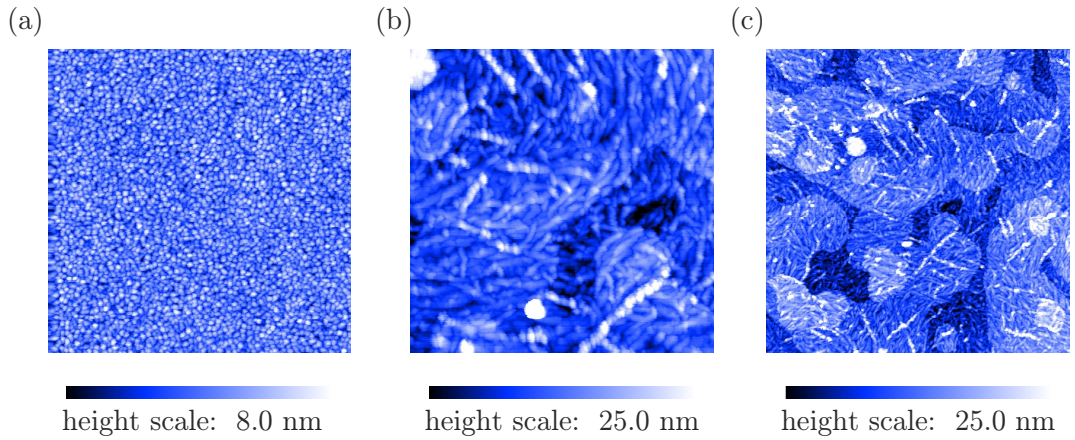


Figure 12.1: AFM images of 20 nm $F_{16}CuPc$ on PMMA (a) and on nominally 15 nm annealed TTC (b) and (c). Sizes are $2\times2\,\mu m^2$ for (a) and (b) and $5\times5\,\mu m^2$ for (c).

XRD measurements

XRD measurements of $F_{16}CuPc$ films for various substrate treatments performed in our group revealed that the β_{bilayer}-phase with a lattice spacing of $d = 14.2 - 14.3\,\text{Å}$ is formed [84,160]. Hence, the morphologies of CuPc and $F_{16}CuPc$ are comparable with identical molecular arrangements but a slightly increased lattice spacing in the case of $F_{16}CuPc$ is observed. This can be attributed to the larger dimensions of the terminating fluorine atoms in the case of $F_{16}CuPc$ compared to the hydrogen atoms in the case of CuPc.

12.2 Transistor measurements

12.2.1 Unipolar n-type OFETs

Measurements

Fig. 12.2 shows transfer characteristics in the linear electron transport regime (a) and output characteristics (b) of an $F_{16}CuPc$ OFET with a PMMA passivation layer, respectively. The device is unipolar n-type. Linear and saturation regimes are well pronounced. The average threshold voltage determined by linear fits of the transfer curves is $V_t = 12\,V$. The electron mobility determined by TLM is $\mu_e = 1.1 \times 10^{-3}\,cm^2/Vs$. For comparison, figs. 12.2(c) and (d) depict the corresponding graphs of a specimen with 10 nm non-annealed TTC as passivation layer.

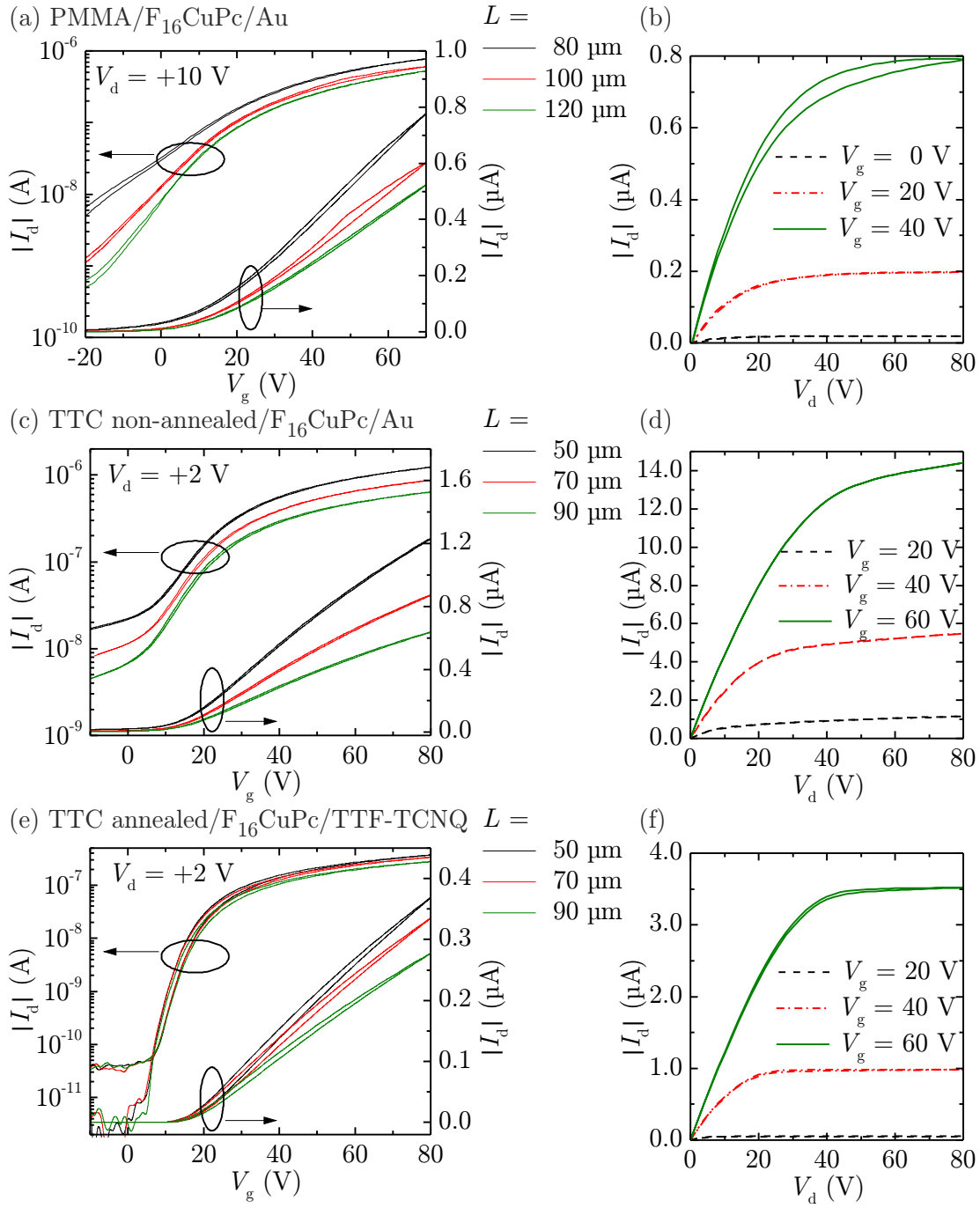


Figure 12.2: (a) Transfer characteristics of an F_{16}CuPc OFET with Au contacts on a PMMA passivation layer. (b) Output characteristics of the device with $L = 100\,\mu m$ shown in (a). (c) Transfer curves of an F_{16}CuPc OFET with Au contacts on 10 nm as-grown TTC. (d) Output curves of the device with $L = 50\,\mu m$ shown in (c). (e) Transfer curves of an F_{16}CuPc OFET with TTF-TCNQ contacts on 15 nm annealed TTC. (f) Output curves of the device with $L = 50\,\mu m$ shown in (e).

OFET layout	V_t (V)	μ_{TLM} (cm^2/Vs)	μ_{sc} (cm^2/Vs)	$R_{c,sc}$ (MΩ)
PMMA/Au contacts	+12	1.1×10^{-3}	2.0×10^{-3}	70
10 nm TTC as-grown/Au contacts	+12	1.8×10^{-2}	1.7×10^{-2}	5.0
15 nm TTC annealed/Au contacts	+12	1.2×10^{-2}	2.1×10^{-2}	4.8
15 nm TTC annealed/ TTF-TCNQ contacts	+16	1.1×10^{-2}	6.6×10^{-3}	21

Table 12.1: Transistor characteristics of F_{16}CuPc OFETs. Electron mobilities are determined by TLM (μ_{TLM}) and by gate bias-dependent single-curve analysis (μ_{sc}). The contact resistance $R_{c,sc}$ is determined by single-curve analysis. All parameters correspond to $V_{eff} = 20\,V$.

The shape of the curves is similar with an identical threshold voltage, but the electron mobility is by a factor of 10 higher. The OFET characteristics of a specimen with Au contacts fabricated on 15 nm annealed TTC are almost identical and are therefore not shown in fig. 12.2. Transfer and output characteristics of an F_{16}CuPc OFET with 15 nm annealed TTC and TTF-TCNQ contacts are displayed in figs. 12.2(e) and (f). This device exhibits a significantly reduced sub-threshold swing of $S \approx 3\,V/dec$ and almost textbook-like output characteristics. The sub-threshold swing of all other transistors is larger than 15 V, which might be an indication of the good energetic alignment of the Fermi level of TTF-TCNQ and the F_{16}CuPc LUMO. Table 12.1 gives an overview of the device characteristics of all four devices.

Discussion

Due to the similar lattice parameters of CuPc and F_{16}CuPc, the growth behaviors of both semiconductors on PMMA and TTC are comparable, which explains the increase in charge carrier mobility and reduction of contact resistance when TTC is used instead of PMMA. Electron mobilities observed on PMMA and TTC agree well with data obtained by Bao *et al.* for F_{16}CuPc deposited on SiO_2 with substrates kept at room temperature and at 125°C, respectively [85]. The threshold voltage of electron transport in F_{16}CuPc ($V_{t,F_{16}CuPc} = +12\,V$) is considerably lower than in CuPc ($V_{t,CuPc} = +50\,V$). This effect can be attributed to a lower injection barrier for electrons and a lower number of electron traps in the F_{16}CuPc film than in a comparable CuPc layer, e.g. at grain boundaries [161]. As illustrated in fig. 4.5(b), ionization potential ($I_P = 6.3\,eV$) and electron affinity ($E_A = 4.5\,eV$) of F_{16}CuPc are significantly higher than the corresponding values of CuPc. Hence, the work function of Au top contacts can be considered as well aligned to the

LUMO of F_{16}CuPc and unipolar electron injection occurs. When TTF-TCNQ is used as contact material, unipolar electron transport is observed, too. Hence, the injection barrier from the Fermi level of TTF-TCNQ ($\phi \approx 4.8 - 5.0\,\mathrm{eV}$) to the HOMO of F_{16}CuPc is too large to inject holes. However, it remains unclear why the charge carrier mobilities determined by TLM for annealed TTC with Au and TTF-TCNQ contacts are equal, whereas the mobility determined by gate voltage-dependent single-curve analysis is lower in case of the sample with TTF-TCNQ contacts. One reason might be inaccuracies related to the single-curve analysis since only one channel length is considered using this technique. Hence, the values calculated by TLM seem to be more reliable.

Up to now, no systematic behavior of the off-current I_{off} could be observed since some devices with F_{16}CuPc active layer exhibit high values and others low values of the off-current, as can be seen in fig. 12.2. Nevertheless, charge carrier mobilities are comparable regardless of the off-current.

12.2.2 Doping experiments

Measurements

In the following, the influence of doping F_{16}CuPc molecules into a CuPc OFET and vice versa will be discussed. Due to the similarity of the crystal structure of CuPc and F_{16}CuPc, the respective doping molecules do not disturb the crystal lattice of the host matrix too much but are incorporated into it [84, 121]. The devices used for these experiments are fabricated with 10 nm non-annealed TTC and Au top contacts. Two doping ratios are realized: A CuPc matrix with 1% F_{16}CuPc and an F_{16}CuPc matrix with 1% CuPc. Pure CuPc and F_{16}CuPc OFETs are also measured for comparison. Transistor characteristics in the linear hole and electron transport regimes of all four devices are displayed in fig. 12.3. The corresponding threshold voltages and field-effect mobilities determined by TLM are summarized in table 12.2.

The OFET with pure CuPc, shown in fig. 12.3(a) exhibits ambipolar charge carrier transport with hole mobilities of the order of $1.4 \times 10^{-2}\,\mathrm{cm^2/Vs}$ and slightly lower electron mobilities. Threshold voltages are highly asymmetric. These values agree well with the data known from chapter 7. The device with pure F_{16}CuPc, fig. 12.3(d), is the same device discussed in sec. 12.2.1 and exhibits unipolar electron transport. It can be seen from the transistor curves of the two doped devices that doping has an important influence on the respective device characteristics. On the one hand, electron transport is completely suppressed when 1% F_{16}CuPc is doped into the CuPc matrix, the hole mobility is lowered approximately by a

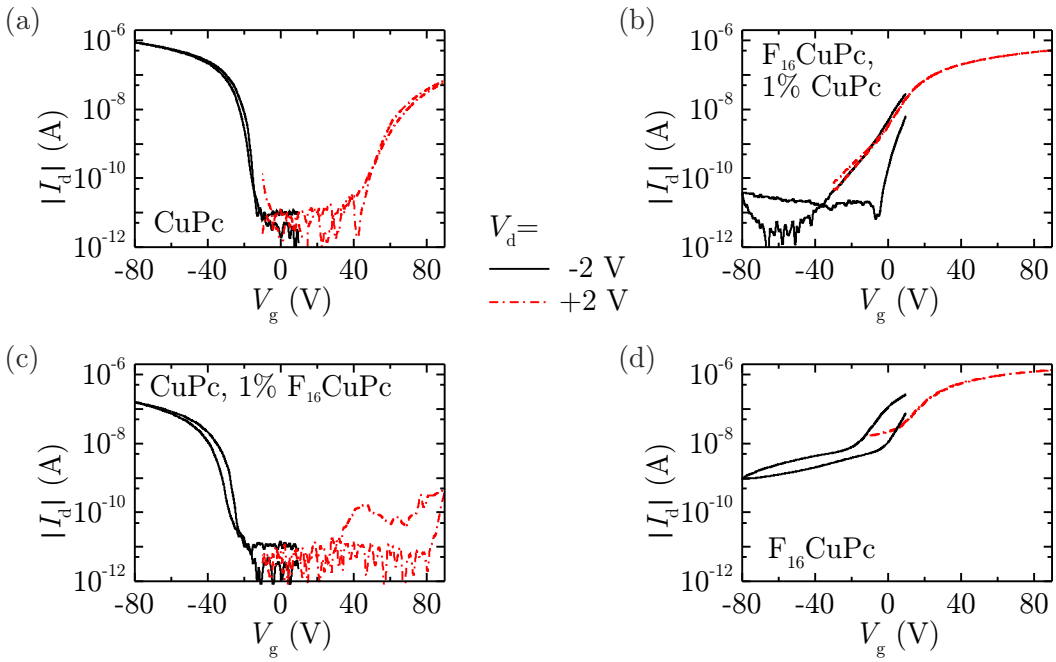


Figure 12.3: Transfer characteristics in the linear hole and electron transport regimes of OFETs with (a) CuPc, (b) F_{16}CuPc with 1% CuPc (c) CuPc with 1% F_{16}CuPc and (d) F_{16}CuPc. All devices are fabricated on 10 nm non-annealed TTC with Au top contacts.

factor of 5 and the threshold voltage is increased (fig. 12.3(c)). On the other hand, when CuPc is doped into F_{16}CuPc, the effect is considerably less pronounced, as can be seen in fig. 12.3(b). The electron mobility is only slightly reduced and the threshold voltage is increased by 3 V.

active material	$V_{t,h}$ (V)	$V_{t,e}$ (V)	μ_h (cm^2/Vs)	μ_e (cm^2/Vs)
CuPc	−25	+70	1.4×10^{-2}	5.2×10^{-3}
CuPc with 1% F_{16}CuPc	−38	—	3.0×10^{-3}	—
F_{16}CuPc with 1% CuPc	—	+15	—	1.6×10^{-2}
F_{16}CuPc	—	+12	—	1.8×10^{-2}

Table 12.2: Transistor properties of the doping series shown in fig. 12.3. Charge carrier mobilities are determined by TLM.

Discussion

The measured transistor characteristics can be explained by the schematic energy diagram depicted in fig. 12.4. The charge carrier transport in CuPc OFETs doped with F_{16}CuPc is schematically drawn in fig. 12.4(a). The F_{16}CuPc molecules form localized electron trap states in the CuPc matrix. When electrons, which are transported in the CuPc LUMO, reach the F_{16}CuPc molecules, they are trapped by these states, which are energetically below the LUMO of CuPc. Consequently, F_{16}CuPc molecules act as electron traps and electron transport is suppressed in devices consisting of CuPc doped with F_{16}CuPc. The energetic position of the HOMO of F_{16}CuPc does not represent a trap for holes. Hence, hole transport is supposed to be unaffected by F_{16}CuPc doping with only 1%. However, it remains unclear for the moment why the hole mobility is decreased by almost one order of magnitude in the case of the device doped with F_{16}CuPc.

When F_{16}CuPc is doped with CuPc, the energy level difference is vice versa, as depicted in fig. 12.4(b). The energetically higher lying HOMO of CuPc acts as trap state for holes in F_{16}CuPc. However, this effect has no influence in the present case since holes cannot be injected into F_{16}CuPc from Au contacts. These states should have no influence on electron transport which is supported by equal electron mobilities in neat F_{16}CuPc OFETS and devices doped with 1% CuPc. The reduction of the off-current is not assumed to be due to the doping with CuPc since this effect is also observed in neat F_{16}CuPc OFETs as discussed in sec. 12.2.1.

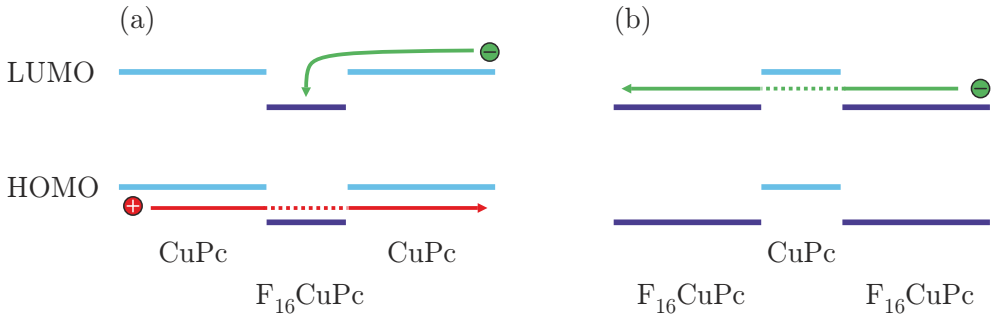


Figure 12.4: Schematic charge carrier transport processes in CuPc OFETs doped with F_{16}CuPc (a) and F_{16}CuPc OFETs doped with CuPc (b).

12.3 Summary

F_{16}CuPc, the perfluorinated analogue of CuPc was discussed in this chapter. Due to the similarity of these two organic semiconductors regarding crystal lattice param-

eters, the growth behavior on PMMA and TTC is almost identical. As with CuPc, F_{16}CuPc forms polycrystalline films with small round-shaped grains on PMMA and elongated grains on TTC. This effect is directly reflected in transistor measurements where the charge carrier mobility is increased by one order of magnitude on TTC compared to PMMA. Identical results have been described for CuPc in chapter 7. These results demonstrate that CuPc and F_{16}CuPc behave in a comparable way with the difference that ionization potential and electron affinity of F_{16}CuPc are considerably increased. This results in electron-only operation of OFETs with F_{16}CuPc and Au top contacts. Up to now, no hole transport could be realized in F_{16}CuPc. Even with TTF-TCNQ top contacts, unipolar n-type characteristics are obtained.

Doping experiments show that F_{16}CuPc acts as electron trap in CuPc which can be explained by the relative positions of HOMO and LUMO of both materials. These measurements demonstrate the importance of highly pure organic semiconductors when ambipolar transport should be achieved.

Chapter 13

Conclusion and outlook

Ambipolar charge carrier transport is a characteristic feature of most organic semiconductors. It is the capability to transport both electrons and holes in the same semiconducting layer. Thereby, considerable asymmetries between both charge carrier types, e.g. regarding the dependence of the charge carrier mobility on semiconductor grain size or temperature, are observed. Although this is a well-known problem and has been reported by numerous groups, the physical origins of these asymmetries have not yet been investigated systematically. However, a fundamental understanding and a potential control of these effects is important since they are crucial for the application of organic FETs e.g. in complementary logic circuits. Apart from the technological point of view, a general understanding of the physical processes that lead to electron and hole transport in organic semiconductors is highly desirable to obtain a better insight into charge carrier transport in organic semiconductors.

The motivation of this thesis was to perform a systematic study of electron and hole transport in the organic semiconductor CuPc. CuPc can be seen as some kind of model system for ambipolar molecular organic semiconductors. OFETs and MIS-diodes have been investigated for this purpose. Three main conditions have to be fulfilled to enable ambipolar charge carrier transport: a trap-free dielectric-semiconductor interface, a trap-free semiconductor and sufficiently low injection barriers for both charge carrier types. The influence of substrate treatment, various dielectric interlayers, different contact materials, grain size and measurement temperature on the charge carrier transport has been investigated. At the beginning it has been shown that transistors with CuPc layer deposited directly on the

SiO_2 gate dielectric exhibit unipolar hole transport due to the presence of electron traps on the SiO_2 surface. PMMA has turned out to provide a trap-free interface so that CuPc OFETs with a thin PMMA interlayer and Au or Ag top contacts showed stable ambipolar transistor characteristics. Morphological investigations with AFM and XRD revealed that CuPc forms a polycrystalline layer with small round grains (diameter approximately 50 nm) and many grain boundaries. Due to this reason one observes low charge carrier mobilities with electron mobilities that are one order of magnitude below hole mobilities.

An important improvement of the crystalline quality of the CuPc layer could be achieved by using tetratetracontane (TTC) as alternative interlayer. Charge carrier mobilities could be increased by approximately one order of magnitude. Additionally, the asymmetry between both charge carrier types has been reduced. This can be attributed to an increased grain size of the CuPc film when deposited on TTC compared to PMMA. High TTC columns, which have been observed for TTC thicknesses larger than two monolayers, turned out to limit the performance of the devices. In order to improve the TTC film, annealing of the TTC-coated substrates in nitrogen atmosphere at 60°C for 120 min turned out to provide optimum growth conditions. The resulting TTC films exhibited smooth terraces due to a redistribution of molecules from high columns to lower layers which are highly crystalline. The dependence of the charge carrier mobilities on the thickness of the TTC film could be correlated to the growth of TTC on SiO_2 and to the morphology of CuPc on TTC. In the sub-monolayer regime, TTC forms islands on the SiO_2 substrate, so that the charge carrier transport is limited by those parts where CuPc grows directly on SiO_2. This results in unipolar hole transport with low mobilities due to the small grain size and presence of electron traps. The hole mobility increases with increasing TTC coverage of the substrate until a closed TTC layer is formed. Subsequently, ambipolar transport could be observed with slightly lower electron mobilities. Upon increasing the TTC thickness, both charge carrier mobilities increase and the asymmetry eventually vanishes. This can be explained by a strong increase of the grain size of the CuPc layer and the formation of a new CuPc crystal phase, which is related to a reduction of the number of grain boundaries, as well as by the diminishing influence of polaronic interactions with the SiO_2 substrate. Finally, for TTC thicknesses larger than approximately three monolayers, balanced charge carrier mobilities were observed with record values for electron transport in CuPc. This is an important result for possible technological applications and yields insight into the different behaviors of electron and hole transport. With the help of simulations and fits to theoretical models, it could be demonstrated that a differing grain boundary trap density is one of the parameters that contributes to the asymmetry.

For the application of OFETs in complementary logic devices it is necessary to realize unipolar *p*-type and *n*-type transistors on one single substrate. This can be done by varying the electrode material. Due to the differing work functions, top electrodes of Al and Ca have been identified to provide unipolar electron injection, whereas electrodes of the organic metal TTF-TCNQ provide unipolar *p*-type characteristics. The respective mobilities remain unchanged compared to ambipolar Au or Ag contacts. However, the contact resistances could be decreased due to lower injection barriers. With the help of this technique it is possible to fabricate complementary inverters with good properties on a TTC-passivated substrate, an active layer of CuPc and one OFET with Al and one with TTF-TCNQ contacts.

TTC also turned out to be provide optimized growth conditions for F_{16}CuPc, the perfluorinated analogue of CuPc. Morphology and growth behavior are comparable to CuPc due to the similar crystal structure. However, the fluorination causes a considerable increase of electron affinity and ionization potential, so that only unipolar electron transport can be observed in F_{16}CuPc. Additionally, the results of doping F_{16}CuPc into CuPc OFETs and vice versa has been studied. F_{16}CuPc doped into CuPc OFETs suppresses electron transport, whereas CuPc doped into F_{16}CuPc OFETs has almost no effects.

As a conclusion, it was possible to obtain ambipolar charge carrier transport in CuPc. Thereby, the importance of the work function of the electrodes for the injection of the respective charge carrier type was demonstrated. The observed effects could be correlated well with density function theory calculations. With the help of systematic studies of the growth of CuPc on TTC in combination with electrical transport measurements, a deeper understanding of electron and hole transport in polycrystalline thin films of CuPc was obtained. It could be shown that the asymmetry between both charge carrier types is affected by various contributions like grain size, grain boundary traps and polaronic interactions and differences in molecular overlap.

As an outlook, the results obtained with CuPc on TTC can also be extended to other semiconductors. Diindenoperylene, which is a promising material for organic photovoltaic cells also exhibits ambipolar transport characteristics when grown on TTC, as measurements of our group demonstrate [162, 163]. Pentacene and its derivatives are further examples, where TTC is a suitable passivation layer to achieve ambipolar OFETs [74]. In contrast to CuPc, no increase of the grain size is observed in all these materials, which shows that there is a special relation between the crystalline phases of TTC and CuPc. In-plane X-ray measurements would be interesting to investigate the lattice parameters more thoroughly. Another aspect that has to be clarified is the correlation between grain size and charge carrier mobilities in the case of CuPc layers. Our experiments on annealed TTC layers

discussed in chapter 8 show that at a certain TTC thickness, the charge carrier mobility saturates although the grain size increases further. A possible reason for this effect might be the 5 nm steps of the TTC layer which can impede efficient charge carrier transport. Hence, an alternative passivation layer has to be chosen for these experiments, which is smooth and enables the formation of large crystals, e.g. due to substrate heating. Since PMMA and TTC are not stable at elevated temperatures, parylene seems to be a promising candidate for these experiments. Preliminary OFET measurements with CuPc exhibited stable ambipolar characteristics comparable to non-annealed TTC layers. In order to improve the validity of the applied models discussed in chapter 10, a contact resistance-free measurement of transfer characteristics would be necessary. This can be done with the help of four point measurements. Further on, ambipolar CuPc MIS diodes with a series of different TTC layer thicknesses might give information if the increased hole mobility observed in chapter 9 is due to the new crystal phase of CuPc which was found on thick, annealed layers of TTC. An alternative approach to avoid the formation of steps in the TTC layer could be the fabrication of the TTC layers from solution. TTC should be soluble in alkane solvents and a spin-coated TTC layer could be free of these steps. However, it is important to sustain the high crystallinity of the TTC layer because it is crucial for the growth of the large CuPc grains. With the help of these experiments one could obtain a better insight into the different temperature dependencies of inter- and intra-grain charge carrier transport.

Beyond the experimental methods used for this thesis, additional techniques could be of interest. Ultraviolet photoelectron spectroscopy (UPS) is a tool to investigate injection barriers of metals on organic semiconductors. It could be used to analyze the differences of the injection barriers for different metal top contacts and to compare these results to the OFET data. Further on, additional DFT calculations would be useful to check if the increased hole mobility in MIS diodes with TTC passivation layer can be due to the new CuPc phase. DFT calculations concerning the orbital overlap with the corresponding molecular stacking would be interesting. It would also be interesting to analyze the effect of the displacement of the CuPc molecules at the TTC steps discussed in chapter 8 by DFT calculations. Hence, there are still a couple of open questions that are worth to be investigated in the near future.

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List of publications

- C. Bihler, M. Kraus, H. Huebl, M.S. Brandt, S.T.B. Gönnenwein, M. Opel, M.A. Scarpulla, P.R. Stone, R. Farshchi, and O.D. Dubon
  "Magnetocrystalline anisotropy and magnetization reversal in $Ga_{1-x}Mn_xP$ synthesized by ion implantation and pulsed-laser melting"
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- Y. Tanaka, Y. Noguchi, M. Kraus, W. Brütting, and H. Ishii
  "Displacement current measurement of a pentacene metal-insulator-semiconductor device to investigate both quasi-static and dynamic carrier behaviors using a combined waveform"
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Curriculum vitae

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