Monolithically Integrated Circuits from Functional Oxides

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Monolithically Integrated Circuits from Functional Oxides

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The rich array of conventional and exotic electronic properties that can be generated by oxide heterostructures is of great potential value for device applications. However, only single transistors bare of any circuit functionality have been realized from complex oxides. Here, monolithically-integrated n-type metal-oxide-semiconductor logic circuits are reported that utilize the two-dimensional electron liquid generated at the $LaAlO_3/SrTiO_3$ interface. Providing the capability to process the signals of functional oxide devices such as sensors directly on oxide chips, these results illustrate the practicability and the potential of oxide electronics.

1. Introduction

A particularly intriguing aspect of oxide electronics is the combination of functional oxides with Si-CMOS (complementary metal-oxide semiconductor) technology, which has the potential to extend greatly the performance of silicon devices. Integrated circuits (ICs) built from functional oxides are needed to fully exploit the functionality of oxides. Whereas ZnO-based ICs have been demonstrated,[1–3] they solve this issue only partially, because the mobile electron system of ZnO is based on s and p electrons and therefore bears the traits of standard, mean-field semiconductors such as Si and GaAs. Much richer functional electronic properties are provided by complex oxides with electron systems based on d or f electrons. Electronic correlations are found in such systems[4,5] and the materials display functional properties that include magnetism of many kinds, memristive effects, multiferroicity, and sensor functions (for overviews see, for example, refs. [6–9]). Electronic correlations offer, for example, the capability to realize phase-transition transistors such as Mott transistors[10–12] or capacitors with large quantum capacitance.[13,14] Resistors, transmission lines, inductors, and capacitors are straightforward to realize from complex oxides; diodes, sensors, transducers, and individual transistors, for example, have already been demonstrated.[6,10,15–19] Numerous devices have been written with the biased tips of scanning force microscopes, even at length scales smaller than 10 nm.[20] However, it has not yet been possible to fabricate transistors that switch other transistors, which is a prerequisite for integrating functional oxides into ICs.

To fabricate oxide field-effect transistors (FETs) with a voltage gain large enough for the devices to be used as building blocks of integrated circuits, materials with conductances that show a strong response to transverse electric fields have to be found for the drain-source channels. Among others, ultrathin and two-dimensional (2D) electron systems induced in oxide heterostructures appear to be promising candidates. First, the electric-field response of such systems is expected to be high, because their electrostatic screening lengths usually exceed the thickness of the conducting sheet. Second, some of these 2D-systems undergo a metal-insulator transition as a function of carrier density, making them candidates for phase-transition transistors.

Electron systems that are ultrathin and in many cases even two-dimensional have been induced in heterostructures of complex oxides, as pioneered by A. Ohtomo and H. Hwang.[21] While electron-phonon scattering limits the room-temperature mobilities in these heterostructures to order 10 $cm^2\ V^{-1}\ s^{-1}$, low-temperature mobilities well above 1000 $cm^2\ V^{-1}\ s^{-1}$ have been achieved in some of the heterostructures.[22–29] Using the 2D electron system at $LaAlO_3$-$SrTiO_3$ interfaces[30] which forms a two-dimensional electron liquid (2DEL)[31] as drain-source channels, n-channel field effect devices have been fabricated using back-gating,[32] side-gating,[33] and top-gating,[18,34,35] and voltage gains larger than one have recently been obtained.[18] In such heterostructures the voltage gain is particularly large because the drain-source channels are embedded in materials with high electronic susceptibilities, the room-temperature small-field dielectric constants of $LaAlO_3$ and $SrTiO_3$ equaling ≈24 and ≈300, respectively. However, as complex oxides usually

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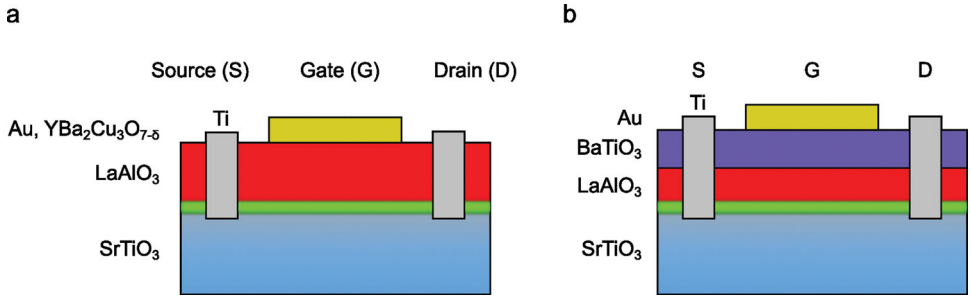

Figure 1. Cross-sectional sketches of two of the FET structures explored. In both cases the DS-channel is formed by the conducting interface (green) between $LaAlO_3$ and a TiO_2-terminated $SrTiO_3$ substrates. The interface is contacted by Ti plugs.

comprise several different kinds of cations, have a complex lattice structure, may easily form unwanted phases, and may have high densities of oxygen vacancies or oxygen interstitials,[36] such heterostructures of complex oxides can harbor many kinds of electronically active defects that may inhibit device functioning. Nonetheless, it may also be expected that in some cases oxides mitigate the impact of defects on their electronic properties. Owing to their typically narrow bands and rather high effective carrier masses, for example, the electron systems in oxides have a more local character than those in semiconductors, such that the electronic perturbation created by defects is confined to a smaller volume. In addition, with usually smaller mean free paths, scattering at defects tends to be less detrimental in oxides than in semiconductors.

2. Results

Motivated by the promising properties of the top-gated $LaAlO_3$-$SrTiO_3$ FETs, we employed them to build NMOS (n-type metal-oxide-semiconductors) ring-oscillators. Starting from the individual transistors presented in ref. [18] we first explored the manufacturability and robustness of devices with various gate configurations by fabricating arrays with increasingly larger numbers of individual transistors. Examples of such devices are given in the cross sectional sketches and photographs of **Figure 1** and **2**, respectively. Figure 2a is a micrograph of part of an array consisting of 81 FETs that use 9 unit cells (uc) of $LaAlO_3$ as gate insulator as shown in Figure 1a. Figure 2b shows a test chip composed of the FETs that are sketched in Figure 2b. The gate dielectric of these FETs consists of a $BaTiO_3$ (8 uc)-$LaAlO_3$ (5 uc) bilayer. The $BaTiO_3$ layer is used to avoid direct tunneling to the gate and to strengthen the samples against electrostatic surges while keeping the capacitance as high as possible. The device characteristics did not show signs of ferroelectricity in the $BaTiO_3$ layer. As shown by scanning transmission electron microscopy (STEM) cross-sectional imaging of the patterned devices (see Figure S1 of the Supporting Information), as expected from the lattice mismatch the layer contains edge dislocations with cores oriented parallel to the interface (**Figure 3**). We attribute the suppression of the ferroelectricity, specifically of the device-relevant out-of-plane ferroelectricity, to the strain field around the cores of such dislocations to which the $BaTiO_3$ is exposed, much as has been reported for $PbZr_{1-x}Ti_xO_3$ nanostructures[37] and to possible further defects of the $BaTiO_3$. Electron energy loss spectroscopy (EELS) spectroscopic images were collected on all the cations simultaneously demonstrating that intermixing was confined to one unit cell at the $LaAlO_3$/$SrTiO_3$ interface and one-to-two unit cells at the $BaTiO_3$/$LaAlO_3$ interface. The slightly lower signal in the $BaTiO_3$ film is due to the disorder caused by the dislocations. These studies revealed the defect rates of Au–$BaTiO_3$–$LaAlO_3$–$SrTiO_3$ devices to be sufficiently small to start the exploratory fabrication of complete integrated circuits covering areas of several mm^2.

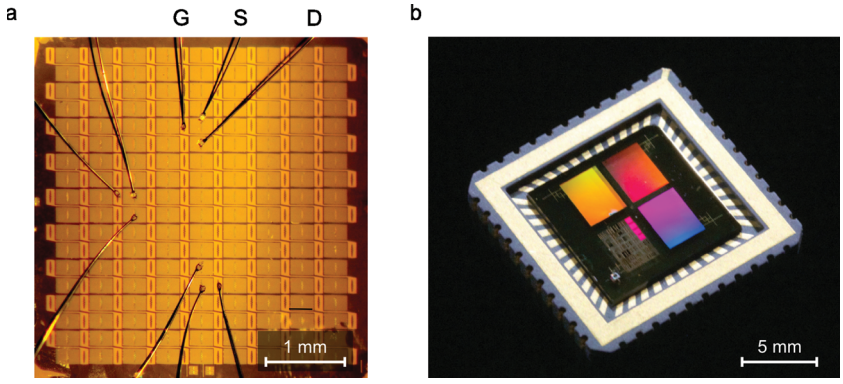

Figure 2. a) Photograph of an array of $LaAlO_3$–$SrTiO_3$ FETs with a design according to Figure 1a. Source (S), Drain (D), and Gate (G) of three FETs are contacted via wirebonding. b) Photograph of a $LaAlO_3$–$SrTiO_3$ chip carrying arrays with more than 700 000 FETs with a design as shown in Figure 1b with channel lengths as small as ≈350 nm. The colors are interference colors arising from the transistor patterns (see the Experimental Section).

To facilitate the fabrication of the integrated circuits, FETs with gate lengths of tens or hundreds of micrometer were used. **Figure 4** shows the current-voltage characteristics $I_D(V_{DS})$ and $I_D(V_{GS})$, the gate leakage current $I_G(V_{GS})$, and the V_{GS} dependence of the subthreshold swing S (the V_{GS} change required to change I_D by a factor ten, see supplementary) calculated from the $I_D(V_{GS})$ data of such FETs. Except for a small hysteresis (see Figure S2a of the Supporting Information), which is attributed to the charging of defects, the characteristics compare well with those of semiconductor FETs (compare, e.g., the $I_D(V_{DS})$ characteristics with the model

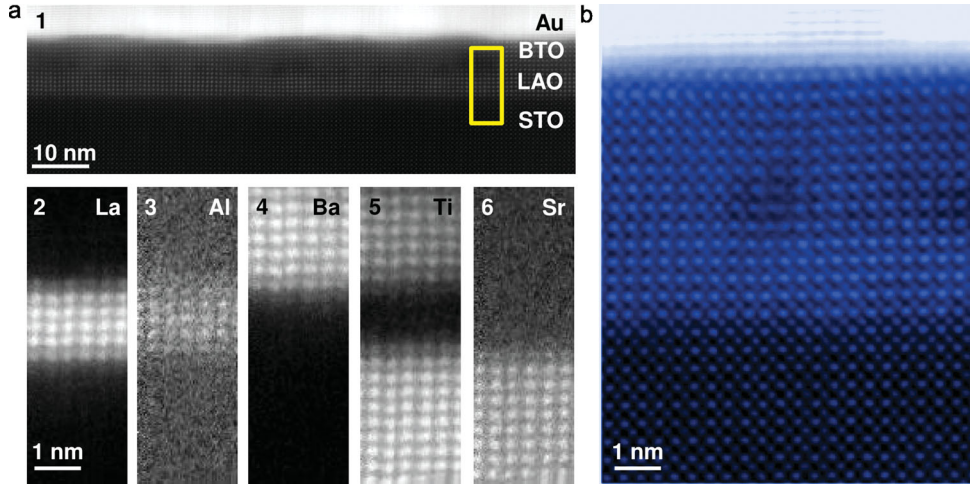

Figure 3. Cross-sectional transmission electron microscopy of the Au/$BaTiO_3$/$LaAlO_3$/$SrTiO_3$ interfaces from a region under the gate. a) Subpanel 1 shows an overview HAADF-STEM of the region under the gate. Edge dislocations are observed at the $BaTiO_3$/$LaAlO_3$ interface, consistent with a relaxation of the $BaTiO_3$ layers. The elemental concentrations of La, Al, Ba, Ti and Sr obtained from EELS spectroscopic mapping are shown in subpanels (2–6) respectively. b) HAADF-STEM image showing the $LaAlO_3$/$SrTiO_3$ interface is coherent, but the $BaTiO_3$/$LaAlO_3$ interface is relaxed, with the edge dislocation residing on the $BaTiO_3$ side of the interface.

calculation of ideal semiconductor MOSFETs as discussed in ref. [38]. With mobilities of ≈5 cm^2 V^{-1} s^{-1} and typical gain factors of β ≈10^{-5} A V^{-2} (300 K), their saturation current densities are ≈10 mA cm^{-1} (V_{GS} = 0 V) and their subthreshold swings are as small as 60–70 mV dec^{-1} (Figure 4d). These swing-values match the theoretical limit of conventional semiconductor FETs.[39] Figure 4e shows the variation of the threshold voltage V_T of several devices. The scatter in the device parameters, for example of V_T or of β, we attribute to the inhomogeneities of the defect distribution in the $SrTiO_3$ substrates and to slight spatial variations of the carrier concentrations across the samples. Gate leakage was found to be insignificant (Figure 4b), and we conclude that in the gate barrier defects are present only in insignificant numbers or do not cause conducting paths. Indeed, self-sealing of pinholes in the gate has to be expected, as for the 2DEL to exist at small V_G, the $LaAlO_3$ layer needs to be structurally intact across a thickness of at least 4 uc.[32] Therefore, as illustrated in Figure 4b (inset), the $LaAlO_3$-$SrTiO_3$ interface below $LaAlO_3$ pinholes is insulating. Rather than providing shorts, the pinholes are thus isolated from the 2DEL. In this case, the balance between the competing interface phases in a complex oxide system facilitates its use in devices. This self-healing effect cannot be operative for gate voltages that are positive and sufficiently large to induce by themselves the 2DEL.

NMOS-type inverters were built by connecting switching-FETs and load-FETs in series (**Figure 5**). To obtain the different saturation currents required for NMOS-inverters, we used switching-FETs and load-FETs of different channel lengths l (l = 50 or 100 µm for the load FETs; l = 100, 150, or 200 µm for the switching-FETs) and kept the channel width w = 600 µm fixed. The transfer characteristics of one inverter are shown in Figure 5b, which again reveal hysteretic behavior as caused by the hysteresis of the FETs. For V_{neg} = 0, the output voltage range of the inverters is shifted by ≈1 V to positive values with respect to the input voltage range. This shift primarily arises due to the finite resistances of the DS-channels, from the $LaAlO_3$–$SrTiO_3$ 2DEL forming the line that connects the transistors with each other, and from the line that connects the switching FET's source to ground.

The ring-oscillators consist of three cascaded inverter stages and an output stage. Each chip fabricated carries six oscillators. These circuits had a minimum feature size (widths of the resistors) of 40 µm. The circuit diagram, the chip layout, and micrographs of the ring-oscillators are shown in **Figure 6** and **7**a–c. Enabled by the voltage gain of the inverter stages (e.g., ≈5 at an input voltage of 150 mV for V_{DD} = 5 V and V_{neg} = –1 V), the outputs of the inverters were coupled to the inputs of the subsequent stages with voltage dividers. To match the threshold voltages of the FETs, the voltage shift described above was compensated by means of the additional negative supply voltage V_{neg} (see Figure 6). Each oscillator comprises eight FETs as well as eight $LaAlO_3$-$SrTiO_3$ 40 kΩ resistors, forming four 1:1 voltage dividers. They were fabricated by structuring rectangular-shaped conductors from the 2DEL (see **Figure** 7c). As shown in Figure 7d, the oscillators work with an output voltage swing of ≈300 mV, and an *RC* time-constant-controlled oscillation frequency of 1.4 kHz, both values matching the expectation.

3. Conclusion

The successful operation of integrated circuits based on $LaAlO_3$-$SrTiO_3$ heterostructures proves that with the deposition and patterning processes available, monolithically integrated, active circuits of functional oxides can be fabricated, despite the defects present in heterostructures of complex oxides. The fabricated circuits consists of oxide FETs, oxide resistors, and oxide interconnects. Diodes and capacitors based on the same

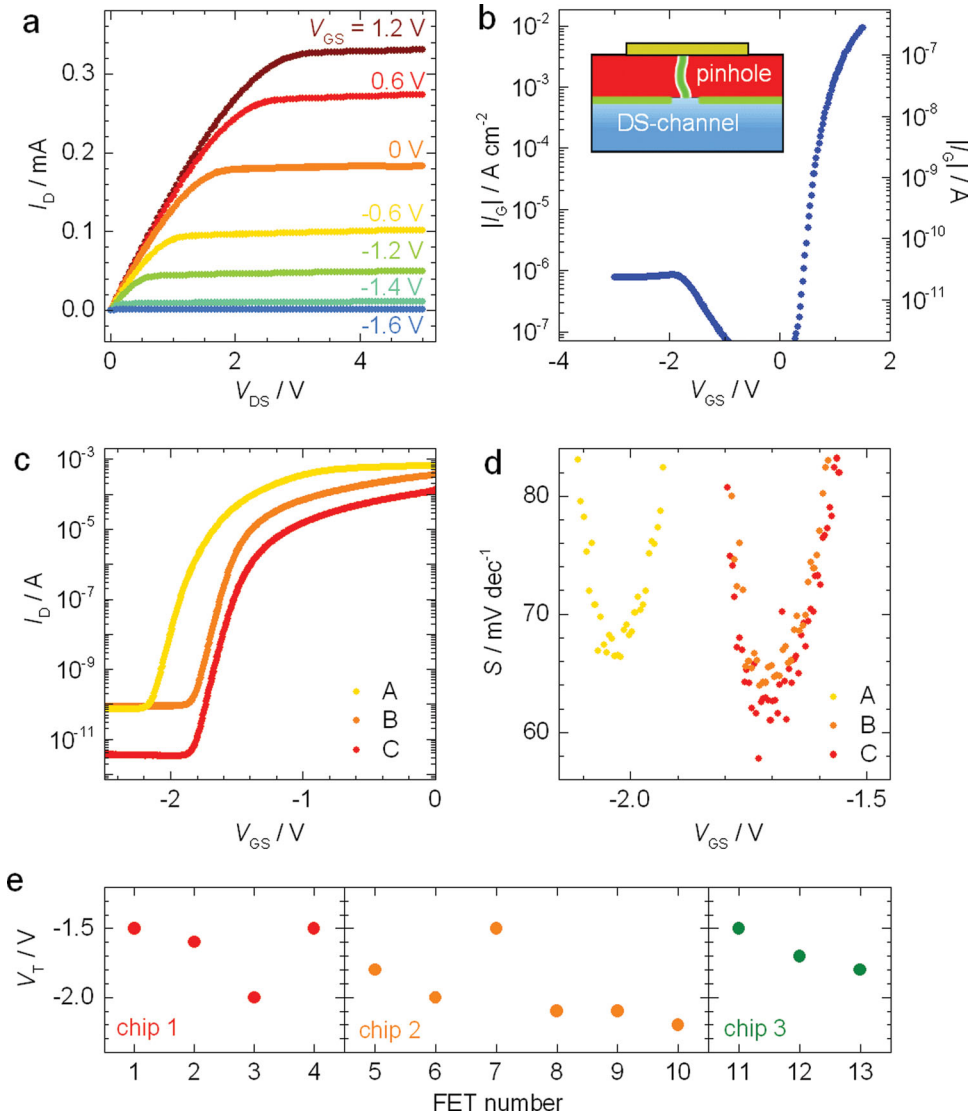

Figure 4. Transport characteristics of FETs with structures as shown in Figure 1b measured at room temperature. a) Drain current versus drain-source voltage for constant gate-voltages of a self-conducting device. The device had a gate length of $l = 30$ µm and a gate width of $w = 300$ µm. b) Gate current and gate-current density as a function of gate voltage ($l = 10$ µm, $w = 300$ µm). Throughout the study the gate currents were much smaller than the drain-source currents. The inset illustrates the self-sealing mechanism supposedly responsible for the generally low leakage currents observed (see text). At negative gate voltages the gate current is suppressed by the electric-field-induced reduction of the interface carrier concentration.[18] c) Drain current versus gate-source voltage at 3 different constant drain-source voltages V_{DS} and channel dimensions. (A: $V_{DS} = 2$ V, $w = 1500$ µm, $l = 10$ µm; B: $V_{DS} = 1$ V, $w = 200$ µm, $l = 20$ µm; C: $V_{DS} = 1$ V, $w = 100$ µm, $l = 20$ µm). Within a gate-voltage range of 2 V on/off-ratios of 10^6–10^8 are obtained. d) Subthreshold swing values $S(V_{GS})$ calculated from the data shown in c). Typical minimum values range from 60 to 100 mV. e) Illustration of the spread of the threshold voltages, showing data of 13 devices grown on several chips.

material system have already been demonstrated.[14,19] While these results were obtained with one specific heterostructure system, the $LaAlO_3$-$SrTiO_3$ interface, they indicate the viability of oxide components and devices to complement Si CMOS technology. We expect that faster devices and CMOS circuits can be implemented once suitable materials with a higher room-temperature mobility[40] and also hole-based oxide interface systems are implemented and optimized. Here, a wide spectrum of possibilities is offered by the large variety of oxide materials systems that is available and by the freedom of choosing the architecture of the heterostructures. Oxide electronic circuits will be characterized by the high functionality characteristic of the oxides and by the fact that their fundamental properties, such as the possible presence of phase transitions or the existence of strong electronic correlations, differ from those of conventional semiconductors.

4. Experimental Section

Sample Preparation: The $LaAlO_3$ films were deposited by RHEED-controlled pulsed laser deposition (PLD) at a growth temperature of

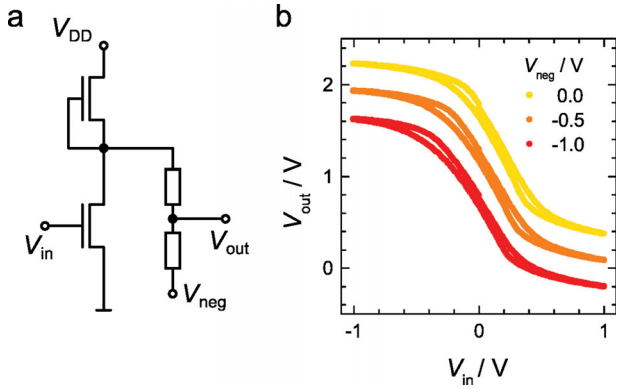

Figure 5. a) Circuit diagram of an inverter based on two self-conducting $LaAlO_3$-$SrTiO_3$ FETs. b) Transfer characteristics of an inverter measured at room temperature (switching-FET: $w = 600$ µm, $l = 200$ µm; load-FET: $w = 600$ µm, $l = 100$ µm; voltage divider resistors: 2×40 kΩ provided by the 2DEL; $V_{DD} = 5$ V).

$T = 780$ °C in an O_2 atmosphere of $p = 1 \times 10^{-4}$ mbar using a laser fluence of ≈2 Jcm^{-2}. The Au films were grown in situ by sputter-deposition in an Ar atmosphere of $p = 0.1$ mbar with an rf-sputtering power of $P = 10$ W. $BaTiO_3$ films were grown by RHEED-controlled PLD in an O_2 pressure of $p = 3 \times 10^{-3}$ mbar at $T = 650$ °C. Lithographically defined interface contacts to the 2DEL were provided by Ar-ion milling and refilling with Ti that was dc-sputtered at $p = 0.05$ mbar and $P = 30$ W.

Patterning: The $LaAlO_3$ films were patterned as described elsewhere.[41] The Au films were patterned by Ar-ion etching or by wet-etching with an aqueous KI:I_2 solution. The electron-beam-lithography was done with a Jeol (JBX-6300FS) 100 kV system. Spin-coated PMMA was used as resist. A slightly conductive solution (ESPACER) was spin-coated on top of the PMMA, to prevent negative influences due to charging of the insulating substrate during patterning. After exposure, the ESPACER was removed in H_2O and the resist was developed with MIBK.

STEM-Imaging and EELS: A cross-sectional TEM specimen was prepared from an area on the patterned wafer under the gate using the FEI Strata 400 focused ion system. HAADF-STEM images and EELS spectroscopic images were acquired on the 100 keV Nion UltraSTEM.[42] The Quefina Dual-EELS spectrometer was used to simultaneously record the signal from the Ti-$L_{2,3}$, Al-$L_{2,3}$, Ba-$M_{4,5}$, La-$M_{4,5}$ and Sr-$L_{2,3}$ edges.

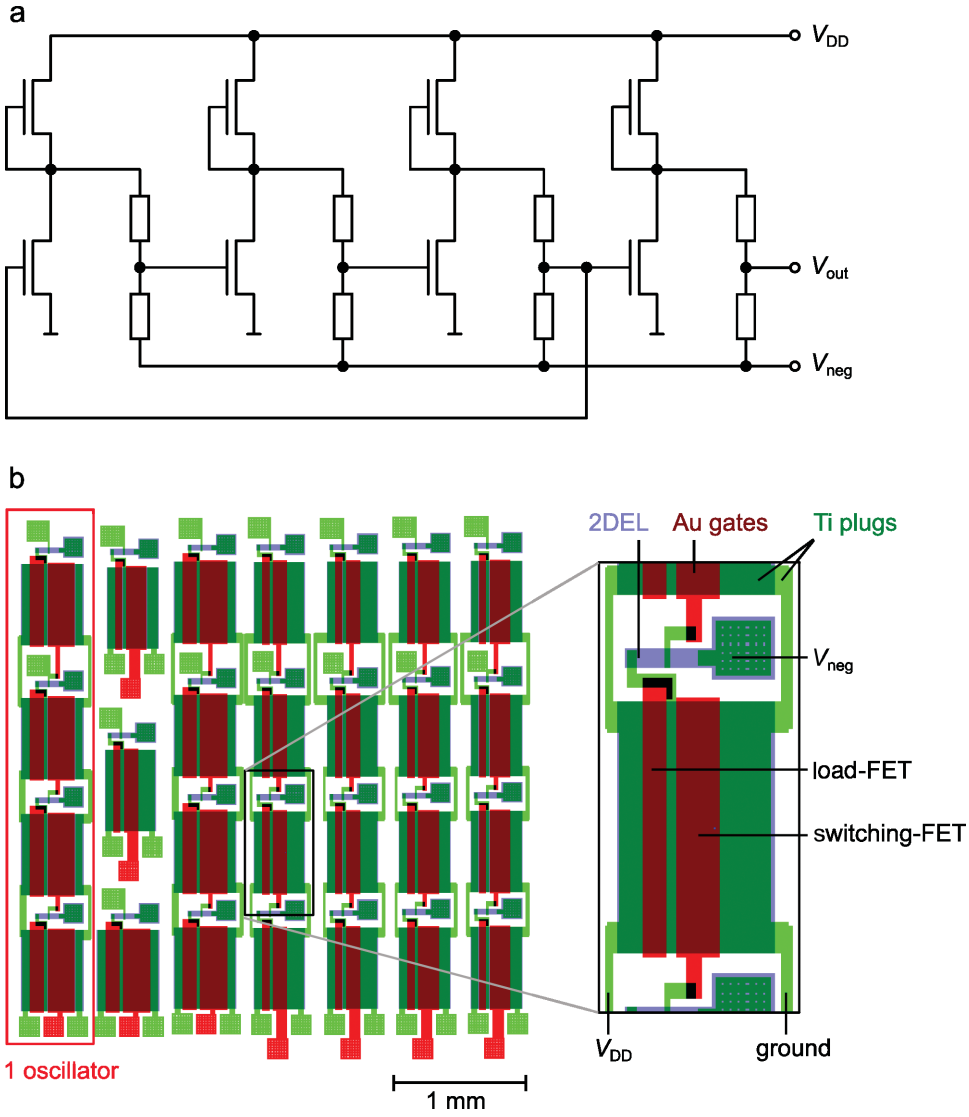

Figure 6. a) Circuit diagram of a ring-oscillator containing three inverter stages and one output stage. Each inverter stage is built as shown in Figure 5. b) Sample design layout containing six ring-oscillators and three additional inverters. The layout is rotated 90° counterclockwise with respect to (a).

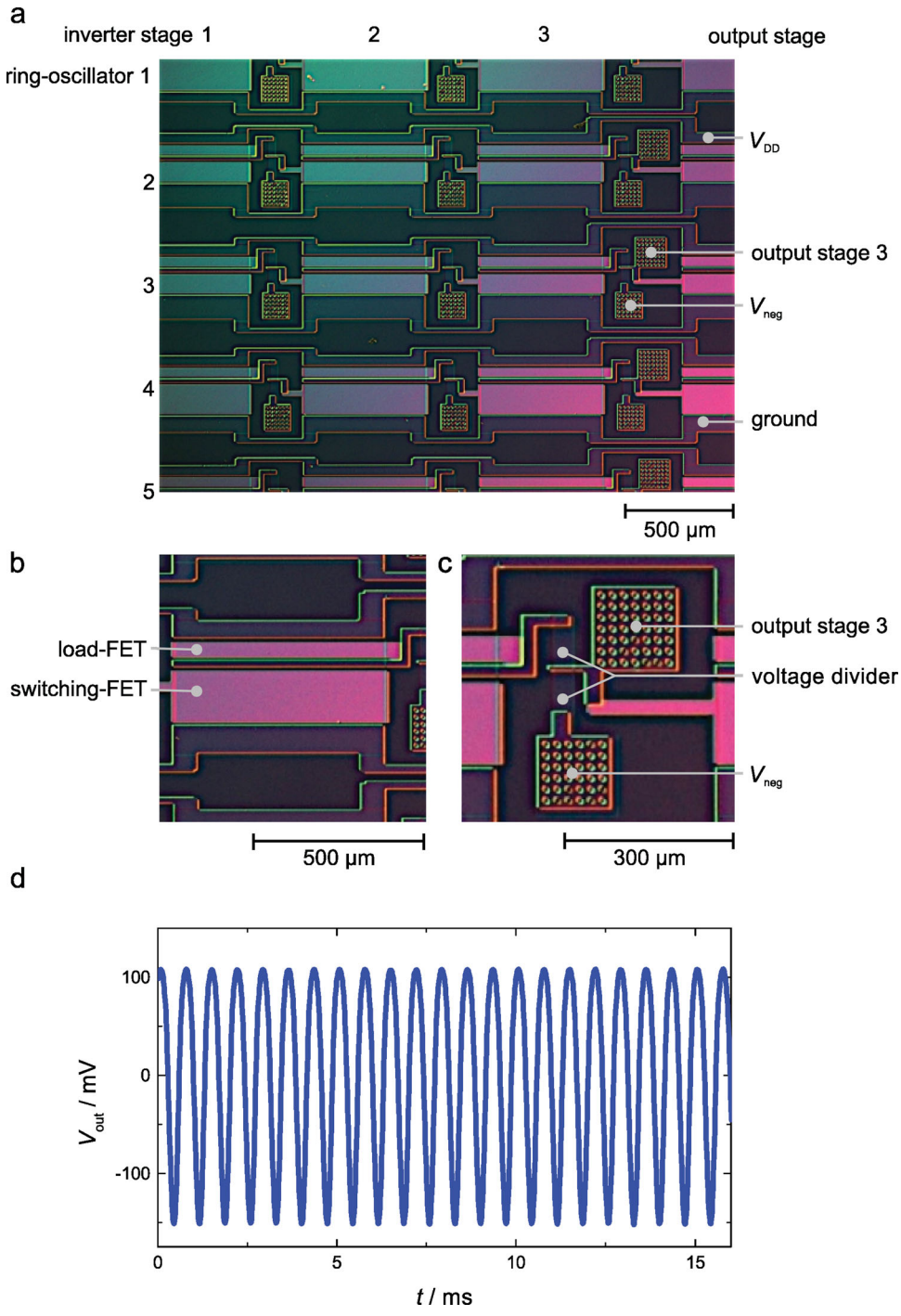

Figure 7. a) Optical microscopy image (interference contrast) of a $LaAlO_3$–$SrTiO_3$ ring-oscillator chip, showing parts of five oscillators. b) Two FETs of one inverter stage. c) One voltage divider and the output of stage 3. d) Output signal of a $LaAlO_3$–$SrTiO_3$ ring-oscillator operated at room temperature (V_{DD} = 6.5 V, V_{neg} = –1.9 V).

Properties of FETs on the Chip Shown in Figure 1b: On this chip, FETs with gate lengths of 550 nm (yellow field in Figure 2b) and larger were found to work well. The FETs with ≈350 nm gate lengths (violet field in Figure 2b) were also operational but had worse $I_D(V_{DS})$ characteristics (see Figure S2b–d, Supporting Information), presumably due to the resistances of the source and drain contacts as well as to an enhanced relative contribution of parasitic conduction of the $SrTiO_3$ at the edges of the ion-edged patterns. The ≈200 nm transistors seen as the third, orange field in Figure 2b did not function due to an alignment problem during e-beam lithography.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

R.J., C.R., G.P., B.F. optimized the growth process and grew the heterostructures, C.W., M.R., T.R., U.W., J.W. optimized and performed the electron-beam-lithography, R.J., C.R., J.Ma. developed the circuits and analyzed with H.B. the data, J.Mu., D.A.M. performed the STEM and EELS studies and R.J., C.W., C.R., B.F. the electric characterizations of the devices. R.J., H.B., J.Ma. wrote the paper with support of the other authors, J.Ma. guided the project. The authors gratefully acknowledge helpful discussions with H. Klauk, J. Maier, and D.G. Schlom. R.J., C.R., B.F., and J.Ma. acknowledge financial support by the Deutsche Forschungsgemeinschaft (TRR80). Electron microscopy research was supported by the U.S. Department of Energy, Office of Basic Energy Sciences, Division of Materials Sciences and Engineering under Award #DE-SC0002334. This work made use of the electron microscopy facility of the Cornell Center for Materials Research (CCMR) with support from the National Science Foundation Materials Research Science and Engineering Centers (MRSEC) program (DMR 1120296) and NSF IMR-0417392. J.Mu. acknowledges financial support from the Army Research Office in the form of a National Defense Science & Engineering Graduate Fellowship.

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