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Achievement of balanced electron and hole mobility in copper-phthalocyanine field-effect transistors by using a crystalline aliphatic passivation layer

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Abstract

Ambipolar charge carrier transport of copper phthalocyanine (CuPc) field-effect transistors with an aliphatic and insulating tetratetracontane (TTC) interlayer are investigated systematically. The TTC interlayer provides a dielectric-semiconductor interface that is free of electron traps. The growth mechanisms of TTC on SiO_2 and CuPc on TTC are studied and charge carrier transport properties are analyzed in dependence of the TTC morphology. Different growth regimes for as-grown and temperature-annealed TTC layers are identified and correlated to the behavior of the respective charge carrier mobilities. Additionally, the thickness of the TTC passivation layer has turned out to influence the grain size of the polycrystalline CuPc layer significantly. Hole and electron transport are affected differently. This behavior can be explained qualitatively with the help of simulations taking into account a difference in grain boundary trap density for electrons and holes. By optimizing the TTC film, balanced charge carrier mobilities can be achieved with $\mu \approx 3 \times 10^{-2}$ cm^2/Vs, which are record values for electron transport in CuPc.

Keywords: Organic Field-Effect Transistors, Ambipolar Charge Carrier Transport, Aliphatic Passivation Layer, Copper-Phthalocyanine, Tetratetracontane

1. Introduction

In recent years, electron and hole transport has been found to be an intrinsic feature for many organic semiconductors. First, this behavior was observed in very pure single crystals by time-of-flight measurements with photo excited charge carriers [1]. Later on it was also found in thin-film organic electronic devices. By choosing electrode materials with an appropriate work function the type of charge carriers injected into the accumulation channel of an organic field-effect transistor (OFET) can be varied [2, 3]. Additionally one has to provide a trap-free interface between the gate insulator and the semiconductor. Electron traps are known to prevent *n*-type operation on widely used oxide insulators [4]. This can be realized by thin inorganic or organic passivation layers [3, 4]. Apart from bipolar transport with appropriate electron or hole injecting electrodes, one can also achieve ambipolar behavior, i.e. transport of electrons and holes at the same time inside the channel [5]. Using different electrode materials *p*-type, *n*-type or ambipolar transport can be obtained for example in copper-phthalocyanine (CuPc - chemical structure in figure 1a) based OFETs. Thereby an asymmetry between electron and hole mobilities was measured for charge carrier transport in thin-films and in single crystals of CuPc [6, 7]. In this paper we demonstrate that balanced charge carrier mobilities are possible in polycrystalline thin-films of the organic semiconductor CuPc using the insulating long-chain alkane $C_{44}H_{90}$ tetratetracontane (TTC) as passivation layer on SiO_2, which has been shown to be highly suitable for the elimination of electron traps [8, 9]. The analysis of the growth behavior of the passivation layer and thereupon the organic semiconductor led to an optimal morphology with respect to the roughness of the TTC layer, leading to balanced mobilities for electrons and holes up to 3×10^{-2} cm^2/Vs which are record values for electron transport in CuPc.

2. Experimental

We fabricated top-contact bottom-gate organic field-effect transistors with varying TTC thickness and 25 nm

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Figure 1: (a) Chemical structure of the organic semiconductor (OrgSC) CuPc, (b) schematic layout of top-contact OFETs and (c) transfer characteristics of devices with channel length L = 50 μm, channel width W = 3.0 mm and TTC thicknesses d_{TTC} of 2 nm, 12 nm and 20 nm.

Figure 2: (a) AFM images of nominally 2 nm (left), 6 nm (center) and 14 nm (right) TTC on SiO_2 and (b) the same as (a) but with TTC annealed at 60°C for two hours. Black colored areas in the 2 nm and 6 nm images of (a) and (b) symbolize bare SiO_2. (c) AFM images of 5 nm of CuPc on TTC layers prepared as in case (b) (all sizes 5×5 μm^2). The numbers in circles represent the transport regimes described in the text. The insets show zoomed areas (0.25×0.25 μm^2) of the CuPc crystallites on the first TTC layer (I), on the second layer (II) and on the third layer (II*).

of CuPc on heavily p-doped silicon wafers with 310 nm thermally grown SiO_2 acting as gate dielectric. TTC, CuPc and the gold top contacts were fabricated by thermal evaporation. TTC layers are highly hydrophobic with a water contact angle of approximately 105°. We determined a dielectric constant of $\varepsilon_{TTC} \approx 2.5$ by capacitance measurements. A systematic sketch of the sample can be seen in figure 1b. On each substrate, there are six individual transistors with channel length ranging from 50 μm to 130 μm and a channel width of 3.0 mm. A detailed description of the fabrication and analysis of the OFETs is given elsewhere [9]. We found that the transistor characteristics depend strongly on the thickness and the post-deposition treatment of the TTC passivation layer. We note that the TTC thicknesses of the investigated devices are nominal thicknesses obtained from the deposited amount on the quartz monitor during evaporation, but not taking into account film roughness (see below).

3. Growth of CuPc on TTC

In figure 1c transfer characteristics of samples with 2, 12 and 20 nm of TTC are displayed. The sample with 2 nm TTC shows unipolar hole transport, whereas all other samples are ambipolar. The sample with 12 nm TTC reveals the best characteristics, while the 20 nm sample has a significantly reduced performance. In order to understand this behavior the TTC morphology was analyzed. As already known from previous work TTC forms crystalline terraces where the molecules are standing upright [9]. The height of one terrace (i.e. one individual TTC layer) is approximately 5 nm which agrees with the length of the molecule. For the following analysis of the charge carrier transport three thickness regimes are relevant. Figure 2a shows atomic force microscopy (AFM) images of 2, 6 and 14 nm of TTC on SiO_2 being representative for each of these three regimes. Region I, TTC thickness lower than one monolayer, corresponds to the growth of islands of TTC on SiO_2 which are not connected to each other. On some islands even the formation of a second layer can already be seen. Region II represents TTC thicknesses between one and about three monolayers. Here, the SiO_2 is covered completely and additional TTC layers are being formed. In region III, i.e. layer thickness larger than about three monolayers, very high columns of TTC appear [10]. For a nominal thickness of 14 nm some of these columns can reach a height of 100 nm. Thus, the growth of TTC on SiO_2 can be described by a Stranski-Krastanov scenario. To determine the influence of these different growth regimes on charge carrier transport we fabricated OFETs with TTC thicknesses between 0 and 22 nm. Charge carrier mobilities were evaluated in the linear regime using the so-called transmission line method (TLM) [11]. The corresponding charge carrier mobilities are shown in figure 3a.

Figure 3: (a) Field-effect mobility determined by TLM for holes (closed symbols) and electrons (open symbols) as a function of TTC thickness for as-deposited TTC layers and (b) for TTC layers annealed at 60°C for two hours (the lines are guides for the eye). (c) Schematic sketches of the charge carrier transport regimes.

The three growth regimes can be correlated very well with three distinct transport regimes. Figure 3c explains schematically the transport processes in the individual regimes I, II and III. In regime I the TTC layer is not fully closed. This leads to the presence of electron traps on bare SiO_2, so that there is no electron transport below roughly one complete monolayer of TTC. For 4 nm TTC there is already a percolation path for electrons, which leads to the onset of electron transport but with rather low mobility. Hole mobility is increasing with TTC thickness from around 2×10^{-4} cm^2/Vs on bare SiO_2 to approximately 2×10^{-2} cm^2/Vs for 8 nm TTC due to the larger grain size of CuPc on TTC as compared to SiO_2 [9]. Larger grains lead to less grain boundaries, which are a key limiting factor for charge carrier transport [12, 13]. In regime II the TTC layer is fully closed and hole and electron mobilities remain relatively constant, however, the electron mobility is by a factor of 2 lower than the hole mobility. In regime III the high columns of insulating TTC begin to hinder the charge carrier transport along the interface. A larger nominal TTC thickness leads to an increase of the area occupied by these columns. Thus, electron and hole mobility decrease again with increasing TTC thickness due to a reduction of the effective area available for the transport

channel at the insulator-semiconductor interface, resulting in a decrease of the current [14].

4. Effects of annealed TTC layers

From these results it can be concluded that the morphology of the TTC-CuPc interface is limiting the charge carrier transport and needs to be improved. Therefore we fabricated a series of TTC-covered SiO_2 substrates and annealed them prior to the deposition of CuPc in an oven at 60°C for 120 min in N_2 atmosphere. Figure 2b shows the corresponding AFM images of nominally 2, 6 and 14 nm of annealed TTC on SiO_2. For 2 nm, there are also TTC islands with a height of one monolayer, like in the non-annealed case. However, the area of the islands is larger and no second layer is formed. In the 6 nm picture, significant changes to the non-annealed samples occur: the height distribution becomes more homogeneous and the TTC terraces are enlarged. This effect is much more pronounced in the case of 14 nm and at even larger thicknesses: the previous extremely high TTC columns in the non-annealed case disappear completely and large, flat TTC terraces of constant height are being formed. We fabricated OFETs using annealed TTC passivation layers with a TTC thickness in the range from 2 to 28 nm. The rest of the fabrication was identical to the samples described above. The resulting field-effect mobilities can be seen in figure 3b and, again, be distinguished in three regimes: In regime I, 0 - 2 nm, there is only hole transport with increasing mobility and no electron transport. In regime II, for TTC thicknesses between 4 and 16 nm, the hole mobility increases very slowly until it reaches its maximum value ($\mu_{ho} \approx 2.0 \times 10^{-2}$ cm^2/Vs), whereas the increase of the electron mobility up to comparable values is more pronounced. In contrast to the non-annealed case there is no regime III with diminishing charge carrier transport for large TTC thicknesses. Instead, for a thickness larger than 16 nm TTC - regime II* - electron and hole mobility are equal at $\mu \approx 2.0 - 3.0 \times 10^{-2}$ cm^2/Vs and stay constant with increasing TTC thickness. We note that this is the highest reported value for electron mobility in CuPc and comparable to the highest reported hole mobilities in thin-film transistors with heated CuPc layers and silanization of SiO_2 surfaces [14] but still lower than the hole mobility in single-crystals ($\mu_{sc,ho} \approx 0.5 - 1$ cm^2/Vs) [15, 16]. Ambipolar transport has been reported for single-crystal FETs but hole mobilities were significantly lower than other values reported for single-crystals ($\mu_{sc,ho} \approx 10^{-3} - 10^{-1}$ cm^2/Vs) and electron mobilities were even lower than in our thin-film devices ($\mu_{sc,el} \approx 10^{-5} - 10^{-3}$ cm^2/Vs) [7]. The fact that the mobilities do not decrease for large TTC thicknesses can be explained very well with the disappearance of the high TTC columns. However, this model cannot explain why the electron mobility still increases in the range from 4 to 16 nm TTC. AFM images show that TTC forms a closed film already for 6 nm annealed TTC so that all electron traps should be passivated. Thus, the reason must be another effect on the insulator-semiconductor interface, namely in the CuPc. To investigate the effects of increasing TTC thickness on the transport channel in CuPc we performed AFM measurements with only 5 nm CuPc on nominally 2, 6 and 14 nm annealed TTC films. The results are shown in figure 2c. CuPc forms polycrystalline layers where the CuPc grains are very well visible and the TTC terraces can still be identified. Details about the crystalline structure of CuPc on TTC have been reported elsewhere [9]. It can clearly be seen that the CuPc grain size increases steadily with the thickness of the underlying TTC layer. On the first TTC monolayer CuPc forms round grains with an average diameter of 100 nm. On thicker TTC layers the grains become more and more elongate, e.g. on 14 nm TTC the CuPc grains have an average length of 200 - 230 nm. We observed a saturation of the grain size for TTC thicknesses beyond 16 - 18 nm with crystallite lengths up to 300 nm. This high degree of crystallinity shows that the growth of CuPc on TTC can be considered as some kind of "pseudoepitaxial" growth [9]. The reason for the increase of the crystallite size is not yet fully understood. It is imaginable that TTC grows in a slightly distorted way on SiO_2 and needs some three or four monolayers to relax to its original crystal structure, which then promotes optimum CuPc growth. Or, as indicated by preliminary x-ray diffraction measurements (not shown here), a different CuPc phase, that exhibits larger crystals, could be formed on higher TTC layers. The increase and the subsequent saturation of the CuPc grain size are coincident with the behavior of the electron mobility in the annealed devices. This effect is illustrated in figure 3c (II*).

The CuPc films in the presented devices are clearly polycrystalline. This limits the charge carrier transport [12, 13] and explains why the mobilities in these devices are smaller than the reported values in single crystal OFETs [15, 16]. Due to our simultaneous analysis of electron and hole transport in the same device a differentiation for the two charge carrier types is possible. Levinson et al. suggested a model to analyze the grain boundary trap density in polycrystalline films which can

also be applied for organic semiconductors [18, 19]. In our case the temperature dependent analysis for samples with 14 nm (regime II) and 28 nm (regime II*) annealed TTC lead to electron trap densities at the grain boundaries of about 2.6×10^{12} cm^{-2} for both devices. The trap density for holes is by a factor of 1.6 lower than the trap density of electrons (see the supplementary information for a detailed analysis). These observations can explain that there is a general difference between electron and hole transport but cannot explain the difference between regime II and II*. A difference in the mobility prefactor is observed which is related to a higher scattering rate for electrons at the grain boundaries or to a lower electron mobility inside the crystalline grains [18]. This could be an indication for a different electrostatic interaction between the charge carriers and the SiO_2 interface. Thereby, the interaction of the charge carriers in the organic semiconductor to induced polarization in the oxide insulator or to interface traps at the oxide surface, can be different for electrons and holes since the traps can be charged and thus affect electrons and holes differently. Additionally, the effective mass of the polaron can be different for negative and positive charges. Both effects will decrease with increasing distance between SiO_2 and CuPc [17]. Further investigations concerning the growth behavior and the electronic interaction are required to quantify these effects.

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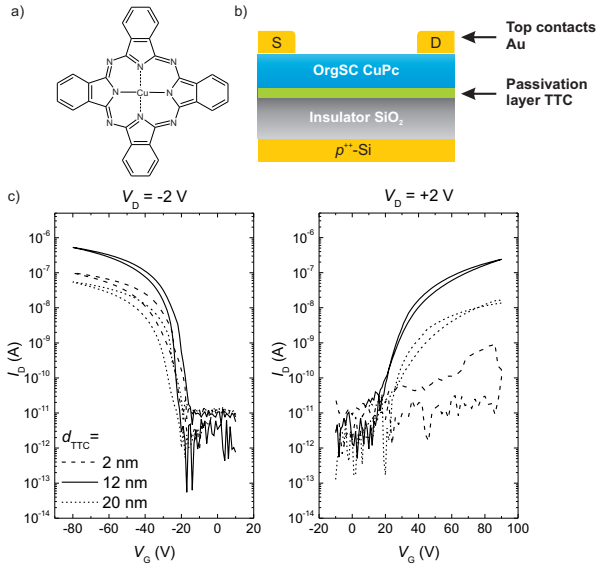

Figure 4: (a) Chemical structure of the organic semiconductor (OrgSC) CuPc, (b) schematic layout of top-contact OFETs and (c) transfer characteristics of devices with channel length L = 50 μm, channel width W = 3.0 mm and TTC thicknesses d_{TTC} of 2 nm, 12 nm and 20 nm.

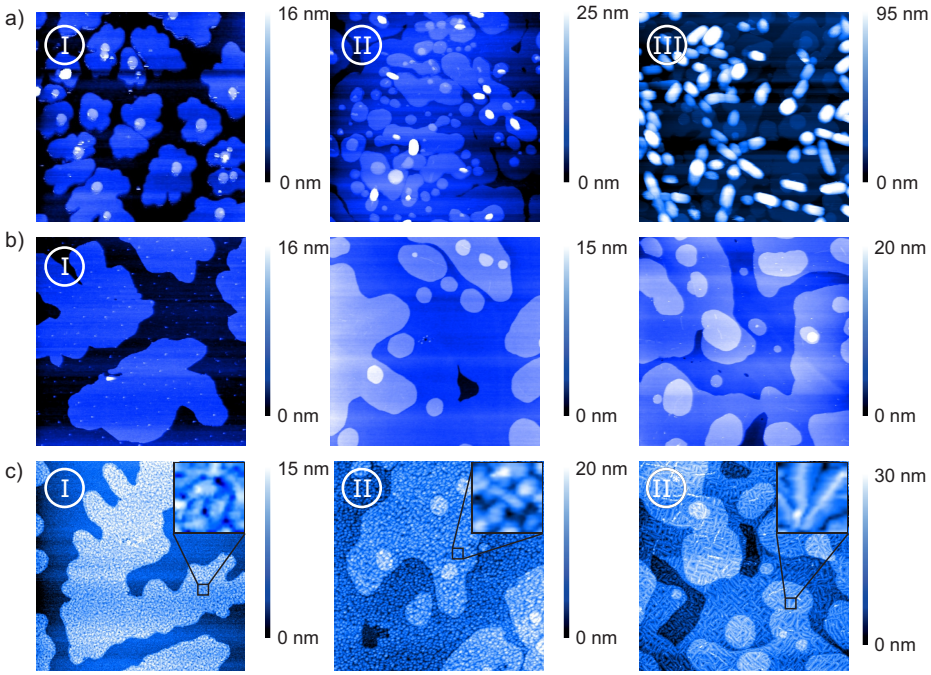

Figure 5: (a) AFM images of nominally 2 nm (left), 6 nm (center) and 14 nm (right) TTC on SiO_2 and (b) the same as (a) but with TTC annealed at 60°C for two hours. Black colored areas in the 2 nm and 6 nm images of (a) and (b) symbolize bare SiO_2. (c) AFM images of 5 nm of CuPc on TTC layers prepared as in case (b) (all sizes $5\times5\,\mu m^2$). The numbers in circles represent the transport regimes described in the text. The insets show zoomed areas ($0.25\times0.25\,\mu m^2$) of the CuPc crystallites on the first TTC layer (I), on the second layer (II) and on the third layer (II*).

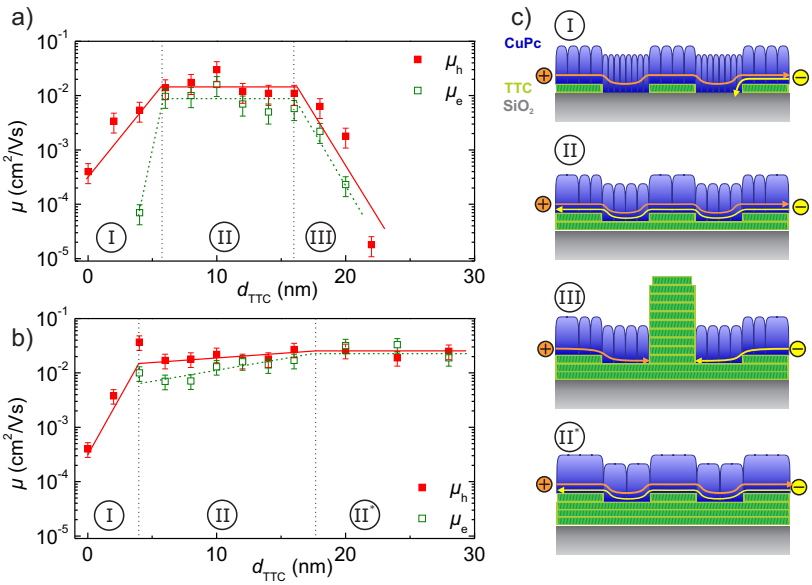

Figure 6: (a) Field-effect mobility determined by TLM for holes (closed symbols) and electrons (open symbols) as a function of TTC thickness for as-deposited TTC layers and (b) for TTC layers annealed at 60°C for two hours (the lines are guides for the eye). (c) Schematic sketches of the charge carrier transport regimes.