Effect of the electromagnetic environment on the single electron transistor

Gert-Ludwig Ingold[1], Petra Wyrowski[1], and Hermann Grabert[1,2]

[1] Fachbereich Physik der Universtäts-GHS, Universitätsstrasse 5, W-4300 Essen, Federal Republic of Germany
[2] Service de Physique de l'Etat Condensé, Centre d'Etudes de Saclay, F-91191 Gif-sur-Yvette, France

The influence of environmental impedances on tunneling rates in a single electron transistor circuit is investigated. Effects of the finite gate capacitance and of stray capacitances at the tunnel junctions are considered. For the case of a low impedance environment the electron tunneling rates reduce to the so-called global rule rate while for a high impedance environment a modification of the so-called local rule rate arises from the stray capacitances. Special emphasis is given to the dependence of the current on the gate voltage which determines the sensitivity of electrometers based on the transistor setup. It is found that a higher sensitivity of the electrometer can be achieved by means of asymmetric transistors.

1. Introduction

In small capacitance tunnel junctions the tunneling of electrons can be hindered by a Coulomb barrier [1, 2]. Provided the charging energy $e^2/2C$ of a single electron exceeds the energy $k_B T$ of thermal fluctuations and the tunneling resistance of the junctions exceeds the resistance quantum $R_K = h/e^2$ a variety of new phenomena arise [3]. The present state of the art of single charge tunneling allows one to sincerely think about applications of the new effects. The controlled transfer of electrons one-by-one [4, 5] might lead to a high precision current standard, and a very sensitive electrometer can be built by means of ultrasmall tunnel junctions [6, 7]. Further applications of single charge tunneling (SCT) are being thought of [8]. The basic unit of many of these applications is the single electron transistor [1] composed of two tunnel junctions in series and a gate electrode capacitively coupled to the common electrode of the junctions. Transistor type circuits have been built not only with oxide layer metal tunnel junctions but were also studied in channels of a two-dimensional electron gas with constrictions [9–11]. In these latter systems the discrete spectrum of the electron states on the common electrode can lead to additional effects that are not discussed here.

Since a small circuit of tunnel junctions with capacitances in the fF range is in some sense a mesoscopic system, it can generally not be considered as being isolated from its electromagnetic environment. The leads attached to the circuit do not only provide the externally imposed voltages but they also couple the electromagnetic fluctuations in the leads to the tunnel junctions [12–14]. For the frequency range of interest the electromagnetic environment can usually be described in terms of a lumped circuit model. The circuit as seen from the junctions is then described by voltage sources and external impedances [13, 15]. In this article was discuss the influence of these impedances on the single electron transistor. In the following section we introduce a rather general circuit to describe the environment and give some results for this model. For the more specific discussion in Sect. 3 we reduce the circuit while retaining the essential features. Some aspects of this model were also addressed by Odintsov et al. [16]. In the last section we present our conclusions.

2. Network considerations and electron tunneling rates

A. Network analysis

To discuss the influence of the electromagnetic environment on a single electron transistor we start by considering the circuit depicted in Fig. 1. It consists of two tunnel junctions in series characterized by capacitances and tunnel resistances C_1, R_1 and C_2, R_2, respectively. To form a SET transistor a gate branch is coupled to the island between the two junctions via a gate capacitance C_G. The transistor may be controlled by the gate voltage V_G which allows for a shift of the island charge. Two voltage sources $V/2$ symmetric to the gate branch lead to a transport voltage V across the double junction. The connections between the voltage sources and the transistor setup are modelled by the impedances $Z_1(\omega)$, $Z_2(\omega)$,

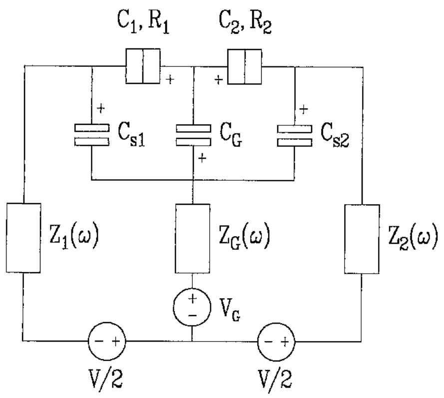

Fig. 1. A model circuit describing a single electron transistor coupled to its electromagnetic environment

and $Z_G(\omega)$. We also include the stray capacitances C_{s1} and C_{s2} formed by the leads leading to the island.

The charges Q_1, Q_2, and Q_G on the capacitors C_1, C_2, and C_G undergo large quantum fluctuations due to the leads attached to the transistor. However, these fluctuations are not independent and the charge on the transistor island $q=Q_1+Q_2-Q_G$ decouples from the electromagnetic environment for $R_1, R_2 \gg R_K$ [15]. The island charge is quantized in units of the elementary charge since it may change only by tunneling of electrons to or from the island. In the absence of background charges the island charge is $q=ne$. If the charges on the capacitors are in electrostatic equilibrium with the applied voltages we have for the average charges

$$Q_1=\frac{C_1}{C_\Sigma}\left[\left(C_2+\frac{C_G}{2}\right)V+C_G V_G+q\right] \tag{1}$$

$$Q_2=\frac{C_2}{C_\Sigma}\left[-\left(C_1+\frac{C_G}{2}\right)V+C_G V_G+q\right] \tag{2}$$

$$Q_G=-\frac{C_G}{C_\Sigma}\left[\tfrac{1}{2}(C_2-C_1)V-(C_1+C_2)V_G+q\right] \tag{3}$$

with $C_\Sigma=C_1+C_2+C_G$. For the charges on the stray capacitances we find

$$Q_{s1}=-C_{s1}\left(\frac{V}{2}+V_G\right) \tag{4}$$

$$Q_{s2}=C_{s2}\left(\frac{V}{2}-V_G\right). \tag{5}$$

The influence of the various impedances (including the capacitances) in the circuit on the tunneling of an electron through one of the junctions may be described in terms of an effective impedance. This impedance is obtained by network considerations which were explained in detail in [15]. The application to the transistor circuit considered here is straighforward if one uses the transformation between T- and π-networks [17] in addition to the rules explained in [15]. For tunneling through the first junction we find the effective single junction circuit shown in Fig. 2. The capacitance C_Σ describes the charging energy $q^2/2C_\Sigma$ corresponding to the island

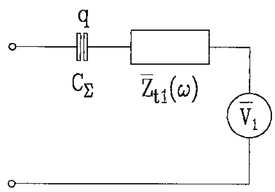

Fig. 2. The effective single junction circuit for the first tunnel junction

charge. From the effective voltage

$$\bar{V}_1=\frac{1}{C_\Sigma}\left[\left(C_2+\frac{C_G}{2}\right)V+C_G V_G\right] \tag{6}$$

one gets the work $e\bar{V}_1$ done by the voltage sources while reestablishing charge equilibrium after an electron has tunneled. The effective total impedance is given by

$$\bar{Z}_{t1}(\omega)=\frac{1}{\mathrm{i}\omega\bar{C}_1+\bar{Y}_1} \tag{7}$$

with the effective total capacitance

$$\bar{C}_1=\frac{C_\Sigma[(C_1+C_{s1})C_{\sigma2}^2+C_1 C_{s1}(C_2+C_{s2})]}{(C_G+C_2)C_{\sigma2}^2+C_2^2 C_{s1}} \tag{8}$$

where $C_{\sigma2}^2=C_2 C_G+C_2 C_{s2}+C_G C_{s2}$ is a capacitance formed by the loop containing the second stray capacitance. The effective admittance is found to read

$$\bar{Y}_1=\frac{C_\Sigma^2\, y_1+\mathrm{i}\omega y_2}{y_1\, y_3+\mathrm{i}\omega y_4} \tag{9}$$

with the coefficients

$$y_1=(C_2+C_G)C_{\sigma2}^2+C_2^2 C_{s1} \tag{10a}$$

$$y_2=C_2^2 C_{s1}^2 Z_1+C_{\sigma2}^4 Z_2+(C_{\sigma2}^2+C_2 C_{s1})^2 Z_G \tag{10b}$$

$$y_3=(C_2+C_G)^2 Z_1+C_2^2 Z_2+C_G^2 Z_G \tag{10c}$$

$$y_4=y_1(Z_1 Z_2+Z_1 Z_G+Z_2 Z_G). \tag{10d}$$

The decomposition of the effective total impedance into a capacitive part and a remaining admittance according to (7) is only correct if the high frequency behavior of the external impedances $Z_1(\omega)$, $Z_2(\omega)$, and $Z_G(\omega)$ is not determined by a capacitance. While this will be so in most cases we shall give an example in Sect. 3A where the environment changes the effective total capacitance $\bar{C}_1$.

B. Electron tunneling rates

Given the effective single junction circuit in Fig. 2 which is described by the island capacitance C_Σ, the voltage $\bar{V}_1$ defined in (6) and the total impedance $\bar{Z}_{t1}$ determined by $\bar{C}_1$ and $\bar{Y}_1$ as given by (8) and (9), respectively, one may calculate electron tunneling rates through the first junction. Following the line of reasoning explained in

[15] one finds the forward tunneling rate

$$\vec{\Gamma}_1(V, V_G, q) = \frac{1}{e^2 R_1} \int_{-\infty}^{+\infty} \mathrm{d}E \int_{-\infty}^{+\infty} \mathrm{d}E' f(E) \cdot [1 - f(E')]\, P_1(E + E_1(V, V_G, q) - E') \tag{11}$$

with the Fermi function $f(E) = 1/[1 + \exp(\beta E)]$ taken at the inverse temperature $\beta = 1/k_B T$. The function

$$P_1(E) = \frac{1}{2\pi\hbar} \int_{-\infty}^{+\infty} \mathrm{d}t \exp\left[J_1(t) + \mathrm{i}\frac{E}{\hbar} t\right] \tag{12}$$

gives the probability that the energy E is exchanged between the tunneling electron and the environment. In (12) the environmental influence is described by means of the function

$$J_1(t) = \int_{-\infty}^{+\infty} \frac{\mathrm{d}\omega}{\omega} \frac{\mathrm{Re}\, Z_{t1}(\omega)}{R_K} \cdot [\coth(\beta\hbar\omega/2)(\cos(\omega t) - 1) - \mathrm{i}\sin(\omega t)] \tag{13}$$

which is given in terms of the total impedance (7) taken relative to the resistance quantum R_K. The energy $E_1(V, V_G, q)$ appearing in (11) represents the energy difference according to the so-called global rule. It is given by

$$E_1(V, V_G, q) = \frac{q^2}{2C_\Sigma} - \frac{(q-e)^2}{2C_\Sigma} + e\bar{V}_1 \tag{14}$$

and contains contributions from the change in charging energy of the island caused by the tunneling of an electron and the work done by the voltage sources while restoring equilibrium between the charges on the capacitors and the applied voltages. The backward tunneling rate $\overleftarrow{\Gamma}_1(V, V_G, q)$ for the first junction can be calculated by means of the relation

$$\overleftarrow{\Gamma}_1(V, V_G, q) = \vec{\Gamma}_1(-V, -V_G, -q). \tag{15}$$

The forward tunneling rate through the second junction is

$$\vec{\Gamma}_2(V, V_G, q) = \frac{1}{e^2 R_2} \int_{-\infty}^{+\infty} \mathrm{d}E \int_{-\infty}^{+\infty} \mathrm{d}E' f(E) \cdot [1 - f(E')]\, P_2(E + E_2(V, V_G, q) - E') \tag{16}$$

where $P_2(E)$ and $E_2(V, V_G, q)$ are obtained from $P_1(E)$ and $E_1(V, V_G, q)$ by interchanging indices 1 and 2 and changing the signs of q and V_G. The backward tunneling rate is connected to the forward rate by a relation analogous to (15).

C. Relation to double junction

Many features of the tunneling rates in a single electron transistor can easily be understood in terms of the behavior of a double junction [1, 15]. Let us first have a closer look at the energy $E_1(V, V_G, q)$. Using the definition (6) of $\bar{V}_1$ we get

$$E_1(V, V_G, q) = \frac{e}{C_\Sigma}\left[\left(C_2 + \frac{C_G}{2}\right) V + C_G V_G + q - \frac{e}{2}\right]. \tag{17}$$

As a consequence, the work done by the gate voltage when transferring charge after an electron has tunneled has the same effect on $E_1(V, V_G, q)$ as a shift of q by an offset charge $Q_0 = C_G V_G$. We may look upon Q_0 as a charge (independent of the gate capacitance) which is imposed externally by choosing the proper gate voltage. Basically, a transistor can be looked upon as a double junction with an effective island charge $q + Q_0$. The effective charge can take a discrete set of values which may be shifted continuously by changing V_G. This externally controlled shift represents the main difference between a single electron transistor and a double junction where $Q_0 = 0$. The combination of the island charge ne and the charge Q_0 leads to a periodicity in Q_0 with period e since the integer part of Q_0 can always be absorbed in n. The remaining dependence of $E_1(V, V_G, q)$ on the gate capacitance can be taken into account by replacing $C_i (i = 1, 2)$ by $C_i + C_G/2$ in the corresponding formulae for the double junction. It should be noted, however, that C_G modifies the effective total impedances Z_{ti} $(i = 1, 2)$.

D. Low impedance limit

We now discuss some general properties of the circuit introduced in Fig. 1 starting with a very low impedance environment $(Z_1, Z_2, Z_G \ll R_K)$ which turns out to be particularly simple. In this case and for not too large transport voltages, the probabilities $P_i(E)$ can be approximated by $\delta(E)$ since there are no environmental modes to which energy could be transferred [15]. The forward tunneling rate through the first junction then becomes

$$\vec{\Gamma}_1(V, V_G, q) = \frac{1}{e^2 R_1} \frac{E_1(V, V_G, q)}{1 - \exp[-\beta E_1(V, V_G, q)]}. \tag{18}$$

At zero temperature the rate is only nonvanishing if $E_1(V, V_G, q) > 0$. As a consequence there exists a gap voltage V_g below which no current can flow. For a symmetric transistor with $C_1 = C_2 = C$ this gap voltage is given by

$$V_g = \frac{e - 2|Q_0|}{2C + C_G} \tag{19}$$

where the charge Q_0 may vary between $-e/2$ and $e/2$. Beyond this range we may use the argument given in the previous section to extend (19) by periodic continuation with a period of e in Q_0. According to (19) the maximum gap is reached for $Q_0 = 0$ while it vanishes for $Q_0 = e/2$. For an asymmetric transistor with $C_1 < C_2$ the situation is slightly more complicated. At $Q_0 = 0$ the gap voltage is $e/(2C_2 + C_G)$ and with increasing Q_0 it decreases linearly down to zero which is reached for $Q_0 = e/2$. The maximum gap voltage, however, is reached for $Q_0 = -e(C_2 - C_1)/4C_\Sigma$. This leads to an asymmetry of the gap voltage as function of Q_0 which is a direct consequence of the asymmetry of the transistor.

E. High impedance limit

In the opposite limit, we assume that the impedances are very large compared to the resistance quantum. To obtain this limit it is sufficient to have $Z_1, Z_2 \gg R_K$. Then, at zero temperature $P_1(E)$ for the first junction is given by the shifted delta function $P_1(E)=\delta(E-e^2/2\bar{C}_1)$. This is a consequence of the high frequency behavior of the impedance (7) which is determined by the capacitance $\bar{C}_1$ defined in (8). For finite temperatures $P_1(E)$ is given by a Gaussian like in the case of a double junction [15]. Evaluating the forward rate through the first junction at zero temperature one finds from (11)

$$\vec{\Gamma}_1(V, V_G, q)=\frac{1}{e^2 R_1}\left[E_1(V, V_G, q)-\frac{e^2}{2\bar{C}_1}\right] \cdot \Theta\left(E_1(V, V_G, q)-\frac{e^2}{2\bar{C}_1}\right). \tag{20}$$

The energy difference occurring in this rate formula may be rewritten as

$$E_1(V, V_G, q)-\frac{e^2}{2\bar{C}_1}=\frac{e}{\bar{C}_1}\left(Q_1-\frac{e-\delta}{2}\right) \tag{21}$$

with

$$\delta=eC_{s1}\frac{C_2C_{s2}+C_GC_{s2}+C_2C_G}{C_2C_{s2}(C_1+C_{s1})+C_1C_{s1}(C_2+C_{s2})+C_G(C_1+C_{s1})(C_2+C_{s2})}. \tag{22}$$

In the absence of stray capacitances δ vanishes, and the energy difference (21) becomes the one appearing in the local rule rate where only the difference in charging energy before and after the tunneling process at the respective junction is considered. The critical charge $e/2$ which according to the local rule has to be exceeded in order to get a nonvanishing rate is diminished by the influence of the stray capacitances. Therefore, stray capacitances become important in the high impedance regime. As can be seen from Fig. 1, the capacitances C_1, C_2, and C_{s1} as well as C_2, C_G, and C_{s2} form loops and therefore the change of the charge Q_1 due to the tunneling process is not independent of the other capacitances. The shift (22) corresponds to the charge which has to be transferred in the left loop after an electron has tunneled in order to satisfy Kirchhoff's law for both loops. The modified local rule thus takes into account all changes in charging energy enforced by the internal equilibrium of the circuit, while, as usual, the equilibrium with the external voltage sources has no effect on the rates in the high impedance limit. Of course, in the limit $C_{s1}\to 0$ the conventional local rule is recovered.

3. Current-voltage characteristics for a reduced model

A. A reduced model

In many real transistor-like circuits the impedances Z_1, Z_2, and Z_G are only of the order of 100 Ω. According to (9) and (10), the effective impedance at zero frequency is reduced further by a factor which for vanishing gate capacitance becomes $(C_2/C_\Sigma)^2$ for the first junction. Therefore, one may often apply the theory in the low impedance limit. However, one should be aware of the fact that for sufficiently large voltages a crossover to the high impedance behavior occurs except in the case of vanishing external impedance [15]. Furthermore, in transistor setups using a channel of a two-dimensional electron gas the impedances Z_1 and Z_2 will typically be in the MΩ range. In the sequel, we shall discuss the effect of higher impedances only in connection with the assumption $Z_1, Z_2 \gg Z_G$. This will usually be the case. From the form of the admittance (9) and its coefficients (10) one finds that Z_G may then be neglected.

For arbitrary impedances Z_1 and Z_2 but vanishing Z_G one may account for the stray capacitances by replacing Z_i by $Z_i/(1+\mathrm{i}\omega C_{si}Z_i)$. This shows that for vanishing impedances the stray capacitances become unimportant since they are shorted out while in the high impedance limit they will affect the rates. As remarked in Sect. 2A this is a situation where the high frequency behavior of the external impedances is determined by a capacitance. Accordingly, the effective total capacitance $\bar{C}_i$ will depend on the stray capacitances C_{si}. In the following we neglect the stray capacitances bearing in mind that, if necessary, we always can reintroduce them by means of the replacement of impedances given above provided that Z_G may be neglected with respect to Z_1 and Z_2. We thus arrive at the simplified circuit shown in Fig. 3 where the environment is determined by the impedances Z_1 and Z_2. We shall not neglect the effect of the gate capacitance C_G which in some experiments is comparable to the junction capacitances C_1 and C_2 [9]. In other experiments C_G is much smaller than C_1 and C_2. One can then drop C_G in C_Σ and $\bar{Z}_{ti}$ but has to keep the product $Q_0=C_G V_G$ finite in order to be able to control the transistor by means of Q_0. For the circuit of Fig. 3

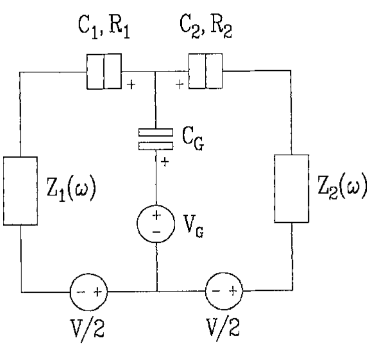

Fig. 3. A reduced model circuit for a single electron transistor coupled to its electromagnetic environment

the effective total capacitance (8) reduces to

$$\bar{C}_1 = \frac{C_1\, C_\Sigma}{C_2 + C_G}. \tag{23}$$

The admittance (9) simplifies to read

$$\bar{Y}_1 = \frac{1}{\kappa_1^2} \frac{1 + i\omega\, C_{2G}\, Z_2}{Z_1 + (C_{2G}/C_G)^2\, Z_2 + i\omega\, C_{2G}\, Z_1\, Z_2} \tag{24}$$

where $C_{2G} = C_2\, C_G/(C_2 + C_G)$ describes the capacitances C_2 and C_G in parallel. The factor

$$\kappa_1 = \frac{C_2 + C_G}{C_\Sigma} \tag{25}$$

accounts for the reduced coupling of this multijunction circuit to the environment [15]. For much of the following discussion we shall assume Ohmic resistances $Z_1 = Z_2 = R/2$. In this case the impedance $\bar{Z}_1 = 1/\bar{Y}_1$ decreases from $\kappa_1^2(R/2)\,[1 + (C_{2G}/C_G)^2]$ at $\omega = 0$ to $\kappa_1^2 R/2$ for $\omega \to \infty$ since the gate capacitance is shortening out the resistance in the branch leading to the second tunnel junction for frequencies $\omega \gg (2/RC_{2G})$. This effect does not occur if C_G is neglected. Then $\bar{Z}_i$ is given by $Z_1 + Z_2 = R$ for all frequencies.

Also for the reduced model, the explicit calculation of tunneling rates requires numerical methods as explained in [15] and [18]. The precision of the numerics can be checked very accurately from the low and high energy behavior of $P_i(E)$. Analytically, these limits can readily be obtained from the corresponding results for a single junction. Using (23) and (24) and defining the dimensionless conductance $g_i = R_K\, \bar{Y}_i(0)$ and the frequency $\omega_{ci} = \bar{Y}_i(0)/\bar{C}_i$, one finds at zero temperature for small energies [13]

$$P_i(E) = \frac{\exp(-2\gamma/g_i)}{\Gamma(2/g_i)} \frac{1}{E} \left[\frac{E}{\hbar\omega_{ci}}\right]^{2/g_i} \quad \text{for } E \to 0 \tag{26}$$

where $\gamma = 0.577\ldots$ is the Euler constant. The behavior for high energies is determined by the high frequency behavior of the admittance according to [19]

$$P_i(E) = \frac{2\hbar^2}{R_K\, \bar{C}_i^2} \frac{\mathrm{Re}\, \bar{Y}_i(E/\hbar)}{E^3} \quad \text{for } E \to \infty. \tag{27}$$

Figure 4 shows a numerically calculated $P(E)$ for a symmetric transistor with $C_1 = C_2$ and $R_1 = R_2$ together with its low and high energy asymptotes. Because of the finite gate capacitance the effective resistances that determine the low and high energy asymptotes are different.

B. Current-voltage characteristics

The rates given in the previous sections may be used to calculate the current-voltage characteristic of the single electron transistor much in the same way as for a double junction by solving the master equation for the occupation probabilities of the different island charge states [1, 15]. In the following we present some numerical results illustrating the behavior of a single electron transistor. In this and the next section we consider the circuit of Fig. 3 with symmetric junction parameters $C_1 = C_2 = C$ and $R_1 = R_2$. Figure 5 shows current-voltage characteristics at zero temperature for a transistor with a gate capacitance $C_G = 2C$, $Q_0 = 0$, and an Ohmic environment for various values of the external resistance $R = 2Z_1(\omega) = 2Z_2(\omega)$. For a finite resistance the gap is always given by the low impedance gap (19). However, for larger resistances one finds a strong suppression of the current also at voltages between the low impedance gap and the high impedance gap.

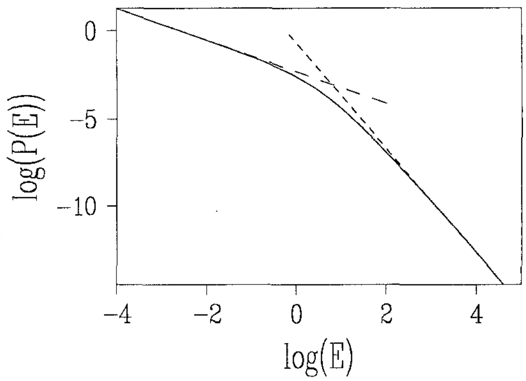

Fig. 4. Double logarithmic plot of $P(E)$ together with the asymptotic behavior for small and large energies according to (26) and (27). This $P(E)$ was calculated for a symmetric single electron transistor with $C_1 = C_2 = C$, a gate capacitance $C_G = 0.5\,C$, and impedances $Z_1 = Z_2 = 0.1\, R_K$ at zero temperature

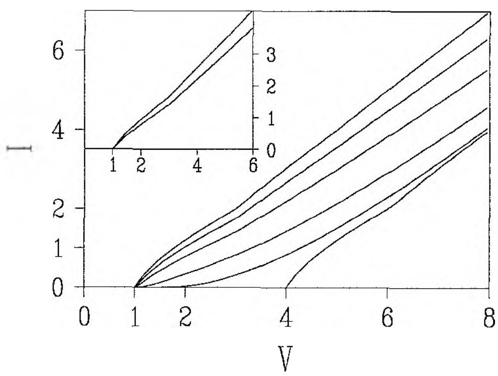

Fig. 5. Zero temperature current-voltage characteristic for a symmetric transistor with $C_G = 2C$. From left to right the impedances $Z_1 = Z_2 = R/2$ are given by $R/R_K = 0, 0.05, 0.2, 1, 5, \infty$. The voltage is given in units of the low impedance gap voltage $V_{g0} = V_g(Q_0 = 0) = e/C_\Sigma$. The current is given in units of $V_{g0}/(R_1 + R_2)$. The insert shows the $I - V$ characteristics for two symmetric transistors with $C_G = 0$ and $C_G = 2C$, respectively, for environmental impedances $Z_1 = Z_2 = 0.1\, R_K$

C. Gate capacitance scaling

For a symmetric transistor in a symmetric environment, i.e., $Z_1(\omega) = Z_2(\omega)$, a change of the gate capacitance C_G leads to a simple scaling of the $I - V$ characteristics. Introducing the capacitance ratio $c = C_G/C$ we may rewrite the rates. For instance, from the rate (18) valid in the low impedance limit we obtain

$$\vec{\Gamma}_1(V, V_G, q) = \frac{1}{1+c/2} \frac{1}{e^2 R_1} \frac{E_1'(V', q')}{1-\exp[-\beta' E_1'(V', q')]} \tag{28}$$

where

$$E_1'(V', q') = \frac{e}{2C}\left[CV' + q' - \frac{e}{2}\right] \tag{29}$$

is the energy difference of a double junction circuit without gate branch [15]. The voltage is scaled according to $V' = (1+c/2)\,V$ and the effective charge $q' = q + C_G V_G$ accounts for the shift of the island charge due to the gate voltage. The inverse temperature is rescaled according to $\beta' = \beta/(1+c/2)$. Since the multiplicative factor $1/(1+c/2)$ of the rate appears also in the current, we find that the current-voltage characteristic for nonvanishing C_G can be obtained from the $I-V$ characteristic for $C_G = 0$ by a proper rescaling of parameters. If $I_0(V_0)$ is the current-voltage characteristic for $C_G = 0$ and temperature T_0 the current-voltage characteristic for finite C_G and temperature T is given by $I(V) = I_0((1+c/2)\,V)/(1+c/2)$ with $T = T_0/(1+c/2)$. Therefore, a finite gate capacitance results in an effectively increased temperature. The same kind of reasoning may be applied to the case of finite impedances where one finds the same scaling of parameters. In addition, the frequency scale of the total impedance $\bar{Z}_{ti}(\omega)$ is changed by a factor $(1+c/2)$. While for vanishing impedance the shape of the $I-V$ characteristic is preserved when C_G is changed this is no longer so for finite impedance since the parameters of the effective impedance are modified due to the frequency scaling.

In Fig. 5 the current-voltage characteristics are presented in terms of current and voltage units reflecting this scaling behavior. The insert compares the $I-V$ characteristics for vanishing gate capacitance and $C_G = 2C$. In the absence of an external impedance these curves would coincide. For finite external resistance we find that the characteristics in these scaled units differs only little for low voltages. On the other hand, for large voltages one reaches the high impedance asymptotes which depend on the gate capacitance in this representation. Accordingly, the two curves in the insert of Fig. 5 separate as the voltage is increased.

D. Q_0-dependence of the current

In the previous section we have discussed the influence of the gate capacitance on the current-voltage characteristic for $Q_0 = 0$. Now, in Fig. 6 we show the dependence of the current on Q_0 for various fixed transport voltages V. This is of particular relevance if the transistor is operated as an electrometer where one determines Q_0 via a current measurement [6, 7]. At zero temperature and for voltages below the gap a current flows only for a certain range of Q_0 while for voltages above the gap one can continuously measure a charge by measuring the current through the tunnel junctions. Figures 6a and 6b show the $I-Q_0$ characteristics for a symmetric tran-

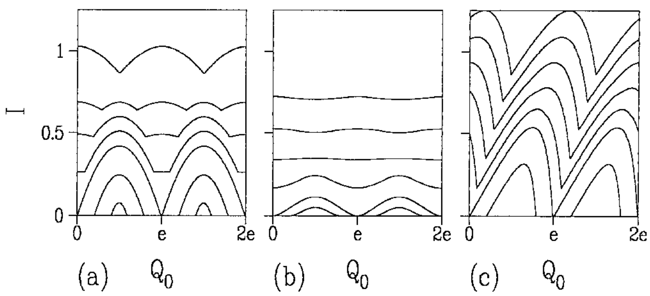

Fig. 6a–c. $I-Q_0$ characteristics at zero temperature for transistors with gate capacitance $C_G = 2C$ and Ohmic environment $Z_1(\omega) = Z_2(\omega) = R/2$. **a** Symmetric transistor with $R/R_K = 0.05$. The transport voltages in units of the gap voltage $V_{g0} = V_g(Q_0 = 0) = e/C_\Sigma$ are from bottom to top $V = 0.2$, 0.6, 1.0, 1.2, 1.4, 1.6, 2.0. **b** Symmetric transistor with $R/R_K = 1$. The transport voltages are $V = 0.6$, 1.0, 1.6, 2.0, 2.4, 2.8. **c** Asymmetric transistor with $R_1/R_2 = 10$ and external resistance $R/R_K = 0.05$. The transport voltages are $V = 0.6$. 1.0, 1.2, 1.4, 1.6, 1.8, 2.0. The current is given in units of $V_{g0}/(R_1 + R_2)$

sistor with low and moderate external resistances, respectively. As discussed earlier, the curves are periodic in Q_0 with period e [1]. The electrometer has its highest sensitivity if biased at the gap voltage. For increasing external resistance the sensitivity strongly decreases as is expected from the suppression of the current above the low impedance gap. In Fig. 6c the $I-Q_0$ characteristics for an asymmetric transistor with $R_1/R_2 = 10$ are shown. At the gap voltage one finds that the range of charges for which the characteristic is basically linear is enlarged as compared to the symmetric case. The reason is that for an asymmetric transistor one of the junctions acts as a bottleneck determining the rate while in the symmetric case two rates combine to yield the current. Another interesting feature is that for the asymmetric transistor one finds a very high sensitivity for a certain range of charges. This could be of considerable interest in connection with the optimization of the performance of SCT electrometers.

The results presented here do not take into account the phenomenon of co-tunneling, a simultaneous tunneling of two electrons. If the tunneling resistances are not large compared to R_K, co-tunneling will lead to important corrections which might be qualitatively similar to the effect of larger external resistances (cf. Fig. 6b). For high tunneling resistances, however, our results should describe the electrometer rather well.

4. Conclusions

We have discussed the influence of the electromagnetic environment on the current-voltage characteristic of a single electron transistor. Starting from a general circuit including stray capacitances, a finite gate capacitance, and environmental impedances, an effective single junction circuit was derived which allows for the calculation of tunneling rates and the Coulomb gap. In the low impedance limit the global rule rate is recovered while in the high impedance limit stray capacitances lead to a modification of the local rule. Current-voltage characteristics were calculated for a simplified model without stray capacitances. It was found that the effect of a finite gate capacitance on a symmetric transistor can be taken into account for a low impedance environment by appropriately scaling the current, the voltage, and the temperature. The current was also studied as a function of the charge induced by the gate which is of importance for the understanding of electrometers based on single electron transistor circuits. External impedances lead to a suppression of the sensitivity. A built-in asymmetry may provide desirable features like a linear characteristic and a higher sensitivity in certain ranges of charges. Corrections to our results will arise from co-tunneling, especially if the tunnel resistances are not sufficiently high. The influence of the environment on co-tunneling and related higher order processes above the gap voltage has not been addressed as yet and remains as an open problem.

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