Nanostructured SiGe thin films obtained through MIC processing

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1. Introduction

Silicon-germanium (SiGe) alloys are thermoelectric materials suited for high temperature application in the range of 600 - 1000 °C [1]. They have long been used in space missions for energy generation converting radio-isotope heat into electricity [1,2] and are promising candidates for future terrestrial applications such as waste heat recovery [3,4]. However widespread use of thermoelectric materials in general could not be achieved due to their still low efficiencies.

In this regard, research on thermoelectric SiGe alloys often focuses on a nanostructuring approach trying to increase the figure of merit

$$Z = \frac{S^2 \sigma}{\lambda}$$

by decoupling the thermoelectric coefficients of Seebeck coefficient S, electrical conductivity σ, and thermal conductivity λ [5,6]. One approach is to utilize polycrystalline materials with grain sizes in the range of microns or below. It has been shown that grain boundaries are able to reduce the lattice contribution to the thermal conductivity by scattering phonons [6,7] or increase the Seebeck coefficient by filtering low energy electrons [5,8]. However, special attention needs to be paid to possible detrimental side effects like impairing the electrical conductivity when reducing the grain size to the nanometer scale as these would compensate any increase in the figure of merit [9,10].

Production of nanostructured SiGe bulk materials often follows a bottom-up approach synthesizing nanoparticles by means of mechanical grinding [10-12] or plasma enhanced chemical vapor deposition [13] followed by sintering. The sintering process itself is usually pressure assisted to ensure that the produced bulk material has no voids and exhibits the best possible conjunction between the nanoparticles. Therefore, this method is unlikely to be applicable to thin films.

In this work, we present an approach to produce nanograined SiGe thin films via sputter deposition of Al/SiGe multilayers and subsequent annealing. The multilayer structure was chosen with the effect of metal induced crystallization (MIC) to be utilized. MIC is a diffusion driven process lowering the crystallization temperature of amorphous semiconductors being in contact with a metal [14]. Two forms of MIC are known with one being compound-forming and the other exhibiting an eutectic system between the semiconductor and metal with Al and Si/Ge being the latter case [15,16]. Control over both the crystallization temperature and crystallite size of the SiGe can be achieved through adjustment of the Al interlayer thickness [17]. Crystallization temperatures as low as 150 °C have been reported [18] and thus would enable the use of flexible substrates like Kapton offering possibilities for future applications at moderate temperatures [19]. An additional advantage of MIC is that parts of the metal get incorporated into the semiconductor. In the case of Al and SiGe hole concentrations in the range of 10^{18} - $5 \cdot 10^{19}$ cm^{-3} can be reached easily [20].

2. Experiment

Samples were magnetron sputter deposited in the form of 50 bilayer stacks as $Si_{80}Ge_{20}$(10 nm)/ [Al(d_{Al})/$Si_{80}Ge_{20}$(10 nm)]$_{50}$ on thermally oxidized Si(001) substrates. The SiO_2 layer (200 nm thick) is needed as an electrical isolation between the SiGe film and Si substrate. For the deposition of SiGe, a $Si_{80}Ge_{20}$ alloy target was used. Samples with four different Al interlayer thicknesses of d_{Al} = {1.8; 3.6; 5; 10} Å were prepared.

All the deposited films are amorphous and were annealed in a hot-wall furnace inside of a steel tube recipient at temperatures between 300 and 600 °C for 1 h. The recipient was pumped down to a vacuum of p = 10 mbar while being flushed with a flow of dry N_2 to make sure no oxidation took place. The microstructure of the as-deposited and annealed films was investigated by transmission electron microscopy (TEM), secondary neutral mass spectrometry (SNMS), x-ray photoelectron spectroscopy (XPS), and x-ray diffraction (XRD). SNMS measurements were carried out using direct bombardment with Ar^+ ions extracted from a RF Ar plasma. In all cases, to avoid charging, the applied bias on the sample was 350 V using a 100 kHz square signal generator with duty cycle of 80%. X-ray diffractograms were obtained with Cu-Kα radiation using a Ni filter. Transport properties in the form of

specific electrical resistivity ρ and Seebeck coefficient S were measured in the temperature range of 300 to 750 K with a home-built system operating at pressures $p < 10^{-6}$ mbar. Resistance measurements were conducted in van-der-Pauw geometry on samples of size 1 x 1 cm². For Seebeck measurements samples of size 0.2 x 1 cm² were exposed to a temperature gradient ΔT generated by two heaters and the resulting voltage ΔU was measured. The temperature gradient was varied such that the Seebeck coefficient could be evaluated from the slope of $\Delta U/\Delta T$.

Samples in the following will be addressed by codenaming: First the used substrate will be given, second the Al interlayer thickness d_{Al} and last the annealing temperature in units of °C with 000 indicating the as-deposited state. Hence, the sample deposited on Si with 10 Å of Al interlayer thickness annealed at a temperature of 600 °C is named Si-10Al-600.

3. Structural Properties

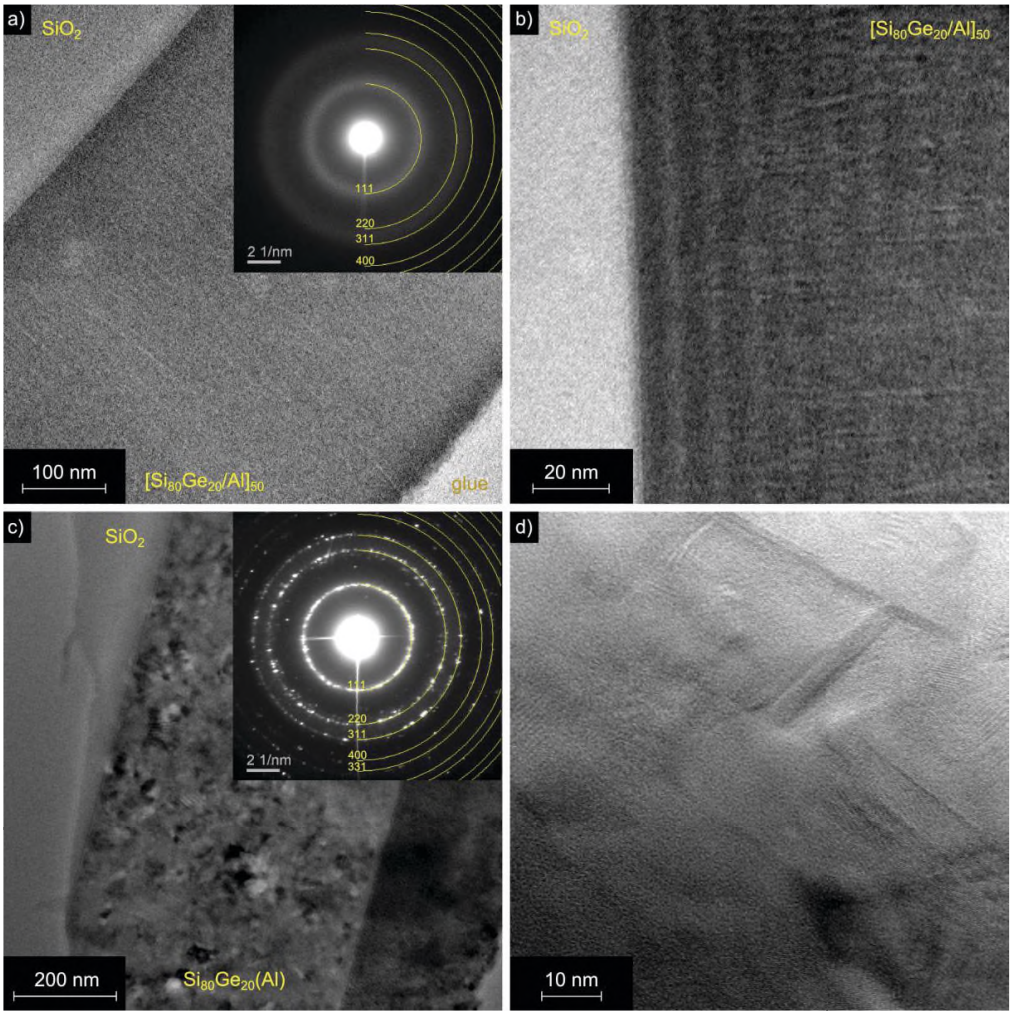

Fig. 1: a), b) TEM bright field images of sample Si-10Al in the as-deposited state and c), d) after annealing at 600 °C at low and high magnifications, respectively. The insets in a) and c) show SADPs taken at the area of the $Si_{80}Ge_{20}$ with yellow lines representing the theoretical diffraction rings of $Si_{80}Ge_{20}$.

3.1 TEM investigation

The microstructure of the samples Si-10Al-000 and Si-10Al-600 was studied by TEM. For the as-deposited state no distinctive features can be distinguished at low magnification in fig. 1a). The inset shows a selected area diffraction pattern (SAPD) of the Al/$Si_{80}Ge_{20}$ multilayer area with only amorphous diffraction halos being present. For comparison theoretical diffraction rings of crystalline $Si_{80}Ge_{20}$ have been added. At higher magnification (fig. 1b)) multilayer structures become visible near the substrate, which match the periodic length of 11 nm. No multilayer structures could be detected far away from the substrate most probably due to increasing roughness of the single layers and non-perfect alignment of the sample in the imaging electron beam.

The annealed sample Si-10Al-600 shows distinct dark-bright contrast in the film region at low magnification originating from different crystallite orientations with respect to the electron beam (fig. 1c)). The SAPD reveals polycrystalline diffraction rings, which correlate well to the theoretical values of $Si_{80}Ge_{20}$. At higher magnifications, defect and grain structures become visible in fig. 1d) and no multilayer structures could be observed over the whole sample area.

3.2 SNMS depth profiling

For further insight on the structural changes induced by the crystallization process, SNMS depth profiles of sample Si-10Al were conducted after different annealings. The depth profile of the as-deposited state depicted in fig. 2a) reflects the multilayer structure in the Al signal clearly with 6 layers distinguishable. The Si signal only shows small intensity variations with perhaps 3 layers distinguishable while no structures are apparent in the Ge signal due to the limited depth resolution compared to the distance d_{Al} of the SiGe layers. The depth profile of the sample annealed at 300 °C still reveals a layered structure in fig. 2b). These are less pronounced compared to the as

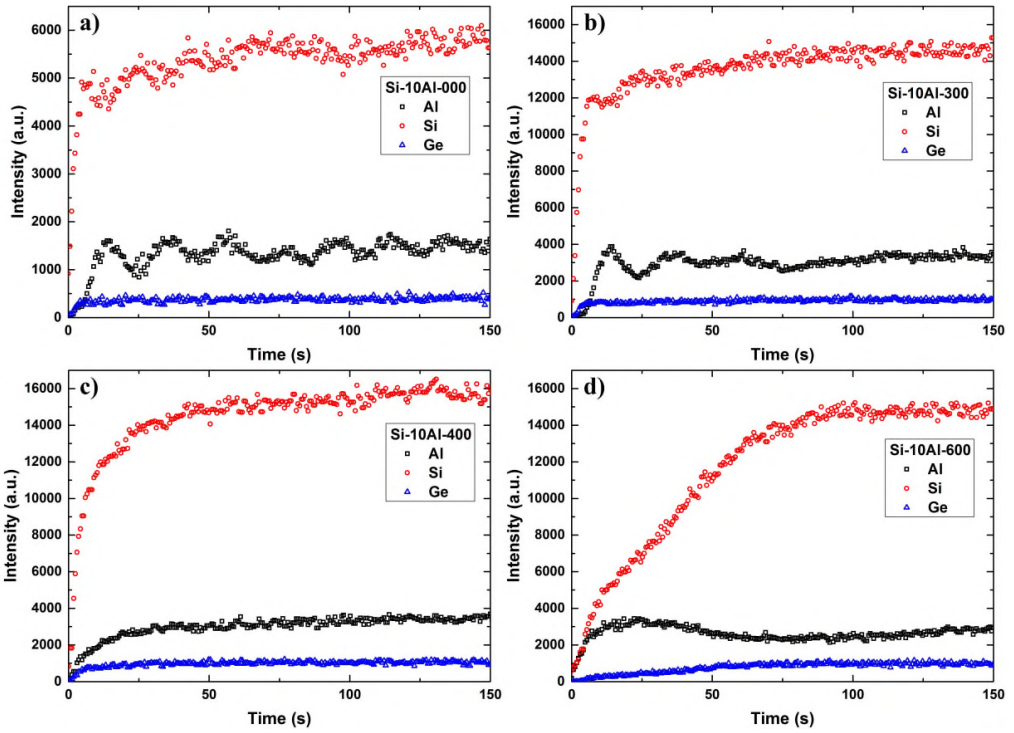

Fig. 2: SNMS depth profiles of sample Si-10Al a) in the as-deposited state and after annealing at different temperatures of b) 300 °C, c) 400 °C, and d) 600 °C.

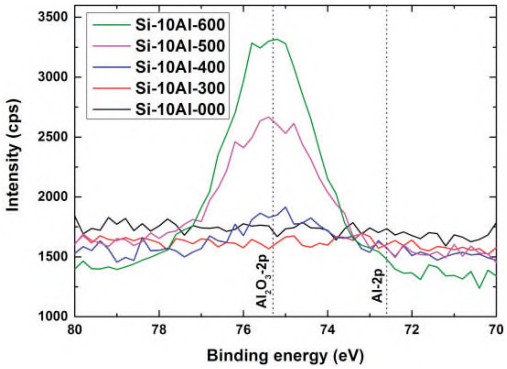

Fig. 3: XPS measurements of the Al-2p peak of sample Si-10Al obtained after different annealing conditions.

deposited state because of intermixing. After annealing at 400 °C no multilayer structure is visible and the sample appears to be homogenous (fig. 2c)). The depth profile of the sample annealed at 600 °C in fig. 2d) also has no signs of a remaining layered structure, but reveals strong surface segregation of Al.

Additional XPS measurements were conducted to verify the evolution of the Al surface segregation. Results of the XPS measurements for the Al-2p peak are shown in fig. 3. For the as-deposited case and samples annealed at 300 °C no Al-2p peak can be detected. For higher temperatures, the Al-2p peak develops providing further evidence for Al surface segregation. Please note that a shift of the Al-2p peak is observed, which corresponds to oxidized Al [21].

3.3 XRD phase analysis

All samples were characterized by XRD regarding their crystal structure and phase composition. Diffractograms for the annealing temperature series of sample Si-10Al are shown in fig. 4a). In the as-deposited case no peaks indicating crystalline phases can be observed. The peak at about 62° observed for all XRD measurements relates to the Cu-Kβ excitation of the Si(004)-substrate peak and occurs due to the limited absorption of the Ni filter. Also in the case of the sample annealed at 300 °C no peaks were observed showing that no crystallization has taken place. This correlates with the SNMS and XPS measurements with respect to the still intact layered structure and non-existent Al-2p peak at the surface for this annealing temperature, respectively. First crystalline diffraction peaks appear at an annealing temperature of 400 °C and become more pronounced for higher temperatures. The theoretical diffraction angles for crystalline $Si_{80}Ge_{20}$ were calculated with respect to Vegard's law [22] and added as dashed

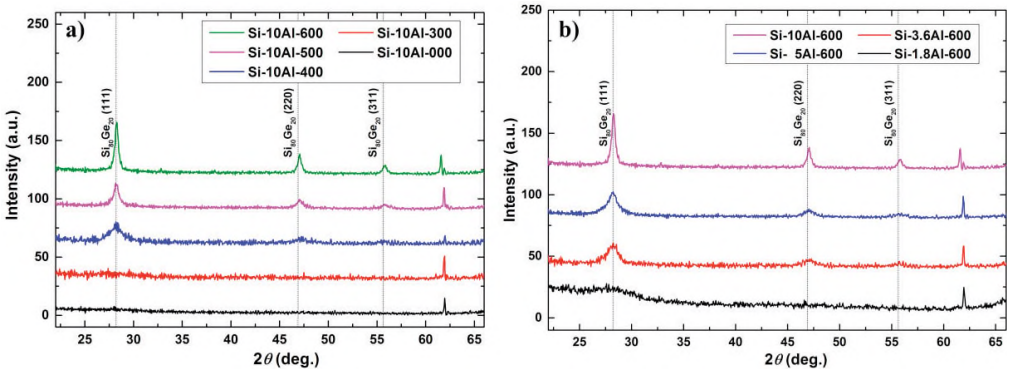

Fig. 4: X-ray (θ–2θ) diffractograms of samples annealed a) at different annealing temperatures and b) with varied Al interlayer thickness d_{Al}.

lines to the diffractograms for comparison. All observed peaks can be allocated to crystalline $Si_{80}Ge_{20}$. The crystallization temperature of SiGe is reported to be around 650 °C varying with composition and annealing conditions [23]. But as crystalline SiGe was already detected at an annealing temperature of 400 °C, the occurrence of MIC is clearly demonstrated. Since the eutectic temperatures of the Al-Si and Al-Ge system are 577 °C and 420 °C, respectively [24,25], it is noteworthy that no phase separation was observed for any annealing above the respective eutectic temperatures.

The diffractograms of all samples annealed at 600 °C are compared in fig. 4b) to elucidate the influence of the Al interlayer thickness on the crystallization process. For the thinnest Al thickness of d_{Al} = 1.8 Å no peaks could be observed, but already for d_{Al} = 3.6 Å crystalline $Si_{80}Ge_{20}$ was detected. For thicker Al interlayers the $Si_{80}Ge_{20}$ peaks become even more pronounced proving the supportive influence of Al on SiGe crystallization through MIC.

The grain size of all annealed samples was estimated via the Debye-Scherrer method [26] and the results were summarized in table 1. All grain sizes are in the range of nanometers, where an increase in Al interlayer thickness d_{Al} and annealing temperature leads to larger sized grains demonstrating control over the crystallization process with respect to the crystallite size.

Table 1: $Si_{80}Ge_{20}$ grain size in nm estimated by Debye-Scherrer method. Please note that samples where the grain size could not be determined are amorphous.

d_{Al} (Å)	Annealing temperature			
	300 °C	400 °C	500 °C	600 °C
1.8	-	-	-	-
3.6	-	-	-	5
5	-	-	5	11
10	-	7	7	18

4. Transport Properties

Resistance measurements were conducted on all samples, but revealed that the resistance of non-crystallized samples (compare table 1) was too high, because of the still amorphous state of the SiGe. Therefore, electrical transport properties will be discussed exemplarily on samples of various Al content crystallized at 600 °C for 1h.

In fig. 5a) the measured specific electrical resistance at temperatures between 300 and 750 K is compared and reveals decreasing resistance with increasing temperature indicating semiconductor-like behavior for all samples. It is also apparent that for increasing Al interlayer thickness the resistance is decreased significantly again proving the supportive influence of Al on the SiGe crystallization. For all resistance curves the same principle temperature dependence is observed having a kink in the temperature range of 500 to 600 K. For a better understanding in terms of thermal activation, the measured resistances are shown in an Arrhenius-plot in fig. 5b). It becomes apparent that

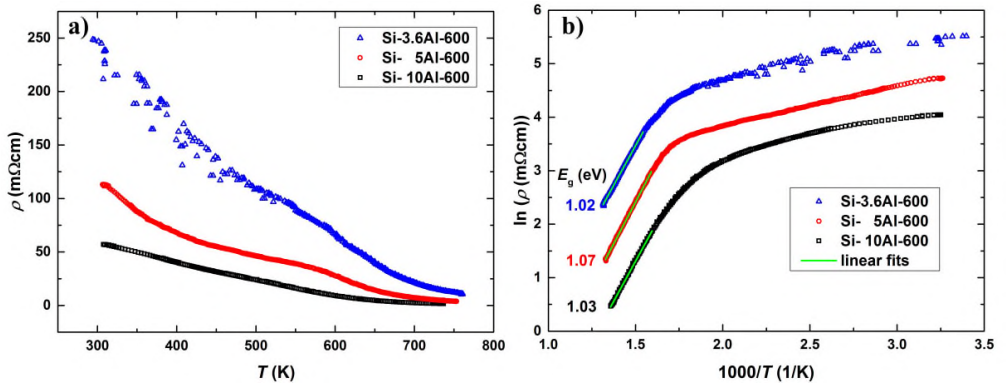

Fig. 5: a) Comparison of the resistance for samples crystallized at an annealing temperature of 600 °C. b) Arrhenius plot of the resistance with linear fits in the high temperature range representing the intrinsic excitation energy of the Si substrate.

for temperatures below and above 600 K two different linear regions are observed indicating two different kinds of thermally activated transport processes. For intrinsic conduction in Si, it was shown that the specific electrical resistance follows the relation

$$\rho = \rho_0 \cdot \exp\left(\frac{E_g}{2k_B T}\right)$$

with E_g and k_B being the band gap and Boltzmann constant, respectively [27]. Hence, it follows the following relation for an Arrhenius-plot of the specific electrical resistance

$$\ln \rho = \ln \rho_0 + \frac{E_g}{2k_B}\frac{1}{T}$$

showing that the band gap energy E_g of Si can be directly evaluated from the linear slope. Linear fits have been added for the high temperature regions in fig. 5b) and from the slope calculated, the respective band gap energies can be extracted having values in the range of 1.02 - 1.07 eV. Using the approximation for the temperature dependence of the band gap energy of Si [27], a value of E_g(600K) = 1.04 eV is obtained, which is in agreement to the measured band gap energy. This hints at intrinsic conduction via the Si substrate for temperatures above 500 K.

Further on Seebeck coefficients measured for all three samples also show a kink around 500 K in fig. 6a) indicating an increase of the charge carrier density n with respect to the Mott equation in approximation for degenerated semiconductors [28]. To rule out systematic measurement errors of our home-built system, comparison measurements for ρ and S at the Fraunhofer Institute for Physical Measurement Techniques (IPM) were conducted on sample Si-10Al-600. Qualitative agreement regarding a substrate-film shortcut for temperatures above 500 K could be achieved, but as different sample pieces were used for the measurements differing degrees of coupling between substrate and film led to quantitative deviations. Additionally, Hall effect measurements were done to elucidate the changes in the charge carrier concentration n shown in fig. 6b). For temperatures up to 450 K a constant carrier concentration $n = +2.5 \cdot 10^{19}$ cm^{-3} was detected. Negative carrier concentrations of $n = -1.5 \cdot 10^{19}$ cm^{-3} indicate electrons as majority charge carriers for temperatures above 450 K. The ongoing exponential rise in absolute value of n further supports the assumption of intrinsic conduction of the used Si substrate as electrons dominate the electronic transport in intrinsic Si due to their greater mobility than holes [29].

Since a 200 nm thick layer of SiO_2 was used as isolation between substrate and film no electrical contact is expected. Therefore, conduction channels have to exist along the SiO_2 acting as shortcuts. In this regard, it is well

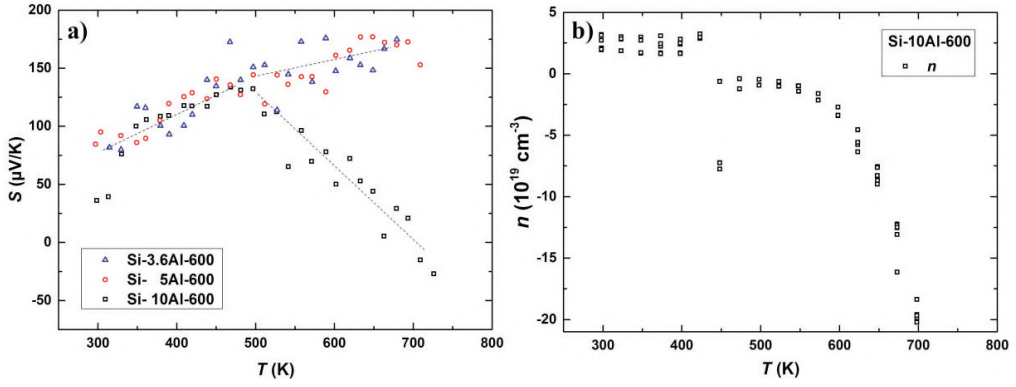

Fig. 6: a) Seebeck coefficient for samples crystallized at 600 °C with guides to the eye added for respective temperature regions. b) Hall effect measurement conducted on sample Si-10Al-600.

known that Al is capable of reducing SiO_2 to Si [30,31] and even a model was suggested for MIC processed Al/Si bilayers deposited on thermally oxidized SiO_2 explaining the evolution of conduction channels between substrate and film [32]. Therefore, all transport properties measured at temperatures higher than 500 K are expected to be dominated by the Si substrate and all further research on this system needs to be conducted on electrically isolating substrates.

5. Conclusion

$Si_{80}Ge_{20}$ thin films of 500 nm thickness were prepared via sputter deposition of Al/$Si_{80}Ge_{20}$ multilayers onto thermally oxidized Si substrates and subsequent annealing. Utilizing the effect of MIC by adjusting the Al interlayer thickness led to lowered crystallization temperature and control over crystallite size of the SiGe. The multilayer structure was destroyed by diffusion during MIC leaving a nanograined, dense SiGe thin film behind. Semiconductor-like behavior in electrical resistance was determined for all crystallized samples. A steep drop in resistance for temperatures above 500 K could be allocated to intrinsic conduction via the Si substrate also being confirmed by changes of the Seebeck coefficient and a change in sign of the charge carrier concentration. This can be explained by the reduction of SiO_2 by Al and thus creating conduction channels along the 200 nm thick isolation layer. Thus for further investigations, it is suggested to switch to electrically isolating substrates.

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