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# Impedance spectroscopy for pentacene field-effect transistor –channel formation process in transistor operation–

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## ABSTRACT

The carrier behavior in pentacene based organic field-effect transistors (OFETs) was investigated by impedance spectroscopy measurements (IS). We clearly observed the carrier injection from the electrode and accumulation at the pentacene/insulator interface. We propose a method for IS in transistor operation by using a battery source for applying the drain voltage. In these measurements, an additional structure is observed where the capacitance gradually increases between injection and accumulation processes. From the comparison of this result and the analyzed curve, which reflects the injection properties from the electrode, we conclude that this additional structure originates from the charge sheet spreading into the channel region. This technique enables us to observe the carrier injection into the channel region and to investigate the charge sheet formation from off-state to on-state and vice versa of OFETs.

**Keywords:** impedance spectroscopy, pentacene, channel formation, carrier injection, field-effect transistor, charge transport, displacement current measurement, organic electronics

## 1. INTRODUCTION

Organic field-effect transistors (OFETs) have attracted attention for decades because OFETs have the advantage of flexibility, light weight and low cost fabrication<sup>1-3</sup>. As the results of ardent research, the mobility of OFETs has increased exponentially<sup>4</sup>. Among the organic materials used for active layer in OFETs, pentacene (Pn) is one of the key materials mainly because Pn based OFETs have high mobility ( $\approx 1 \text{ cm}^2/\text{Vs}$ )<sup>3-5</sup>. However, the growth rate of mobility tends to saturate recently, partly due to the lack of the understanding of the operation mechanism. From the view point of the device stability, for example, many OFETs have been found to exhibit undesirable threshold-voltage shifts, hysteresis, or mobility degradation as a result of prolonged bias-temperature stress<sup>6</sup>. The origin of these processes should be understood for device application.

In order to clarify the operation mechanism of OFETs in detail, carrier injection properties have been the main focus, because the conducting channel is formed by the carriers injected from the electrodes. S. Ogawa *et al.*, evaluated carrier injection and accumulation properties of OFETs by displacement current measurement (DCM)<sup>7-11</sup>. Recently, drain-to-source current and displacement current have been evaluated using the simultaneous measurements of source and drain currents during the application of a constant drain voltage and a triangular-wave voltage<sup>12-14</sup>. Second harmonic generation technique allows for the direct probing of dynamic carrier motion<sup>15-17</sup>. In addition, impedance spectroscopy (IS) has been used to investigate depletion and accumulation behavior in OFETs<sup>18-20</sup>. Many electrical methods, however, are two-terminal measurements, that is, the voltage is applied to one electrode and the other one is connected to the ground. On the other hand, OFETs have three electrodes; source, drain and gate electrodes. Therefore it is not necessarily appropriate to conclude that the observed carrier behavior in these methods correspond to that *in transistor operation*.

In this paper, we have proposed the measurement setup for IS on OFETs, which allows for the observation of carrier behavior in transistor operation by using a battery source for applying the drain voltage ( $V_{\text{DS}}$ ). In capacitance-voltage ( $C$ - $V$ ) relationship, we observe carrier injection and accumulation processes without  $V_{\text{DS}}$ . Capacitance-frequency ( $C$ - $f$ ) curves show that the injection process is much faster than the accumulation process. When  $V_{\text{DS}}$  is applied, an additional structure is observed, where the capacitance gradually increases between carrier injection and accumulation processes.

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Comparing this result with the curve obtained from the result of  $V_{DS} = 0$  V, which mainly reflects the injection properties, we conclude that the additional structure originates from the charge sheet spreading into the channel region. This method enables us to observe the charges, which are injected to the channel region, and to investigate the operation mechanism of OFETs in more detail.

## 2. METHOD

The principle of IS is simple; a combined DC and AC voltage is applied to the sample and the current response is measured. From the impedance, the capacitance can be estimated. For simplicity, we briefly explain the principle of IS applying to metal-insulator-semiconductor (MIS) device<sup>21, 22</sup>.

As mentioned above, AC voltage ( $V_{AC}$ ), which is given by

$$V_{AC}(t) = |V_{AC}| \exp(i \cdot 2\pi f t) \quad (1)$$

is applied to the sample. Here,  $f$  is the frequency of the applied voltage. Then, the current in MIS device is expressed by

$$I_{AC}(t) = |I_{AC}| \exp(i \cdot 2\pi f t + \varphi), \quad (2)$$

where  $\varphi$  denotes the general phase shift. Since the complex impedance ( $Z$ ) is the ratio of  $V_{AC}$  and  $I_{AC}$ ,  $Z$  can be expressed as

$$Z(t) = \frac{V_{AC}(t)}{I_{AC}(t)} = \text{Re}(Z) + i \cdot \text{Im}(Z). \quad (3)$$

Finally, the capacitance ( $C$ ) is calculated as

$$C(f) = -\frac{1}{2\pi f} \cdot \frac{\text{Im}(Z)}{\text{Re}(Z)^2 + \text{Im}(Z)^2}. \quad (4)$$

The DC voltage ( $V_{DC}$ ) is only used to change the carrier accumulation condition of the MIS device in static state, for example, depletion or accumulation.

## 3. EXPERIMENT

Figure 1 (a) shows the top contact type FET structure being studied. A p-type Si wafer (resistance  $< 0.02 \Omega \cdot \text{cm}$ ) was used as the substrate of OFETs. The thickness of the oxide layer was 300 nm. A 30 nm thick tetratetracontane (TTC;  $\text{C}_{44}\text{H}_{90}$ ) layer was deposited on the  $\text{SiO}_2/\text{p-Si}$  substrate as the insulator layer and annealed at 350 K for 10 min in a glove box (GB) filled with nitrogen. Then, a 100 nm thick Pn layer was evaporated, and finally gold was deposited as source and drain electrodes through a shadow mask. The device was transferred to the GB for electrical measurements. The channel length and width were 100  $\mu\text{m}$  and 4 mm, respectively. The area of source and drain electrodes was both 16  $\text{mm}^2$ , and the electrode pads (5  $\text{mm}^2$ ) were connected to the each electrode. The area of Pn was the same as the sum of the area of the electrodes and channel region.

IS measurements were performed using a frequency response analyzer (Solartron SI 1260 Impedance/Gain-Phase Analyzer) combined with a dielectric interface (Solartron 1296) at University of Augsburg. In IS measurement,  $V_{AC}$  was applied to the heavily doped p-Si substrate with respect to the source electrode at an amplitude of 0.1 V and frequency was swept from 100 kHz to 0.1 Hz for  $C$ - $f$  curves.  $V_{DC}$  was swept from 20 to -40 V for  $C$ - $V$  curves. To investigate the carrier behavior in OFET under transistor operation, an isolated battery source was used for  $V_{DS}$  [dashed line in Fig. 1]. Since the circuit with the current flow of  $I_{DS}$  is isolated electrically from the gate electrode,  $I_{AC}$  can be directly measured under transistor operation.

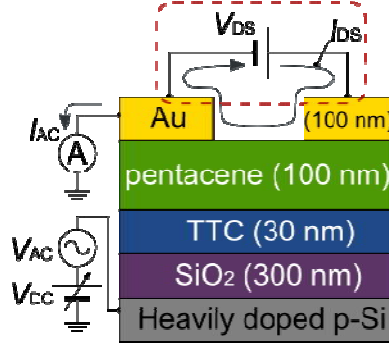


Figure 1. Schematic illustration of device structure and experimental setup.

## 4. RESULTS AND DISCUSSION

### 4.1 Transistor characteristics

The  $I_{DS}$ - $V_{DS}$  curves for the p-channel and n-channel Pn-FET are shown in Fig. 2(a) and (b), and  $I_{DS}$ - $V_{GS}$  curves for the p-channel and n-channel Pn-FET are shown in Fig. 2(c) and (d), respectively. This device showed good ambipolar property and the field-effect mobility of holes ( $\mu_h$ ) and electrons ( $\mu_e$ ) were estimated as  $\mu_h = 0.23 \text{ cm}^2/\text{V} \cdot \text{s}$  and  $\mu_e = 0.019 \text{ cm}^2/\text{V} \cdot \text{s}$ , respectively. Since the ambipolar characteristic was not observed in Pn-FET without TTC layer (not shown), this result indicates that the TTC layer effectively restrains the electron traps on the  $\text{SiO}_2$  surface as previously reported.

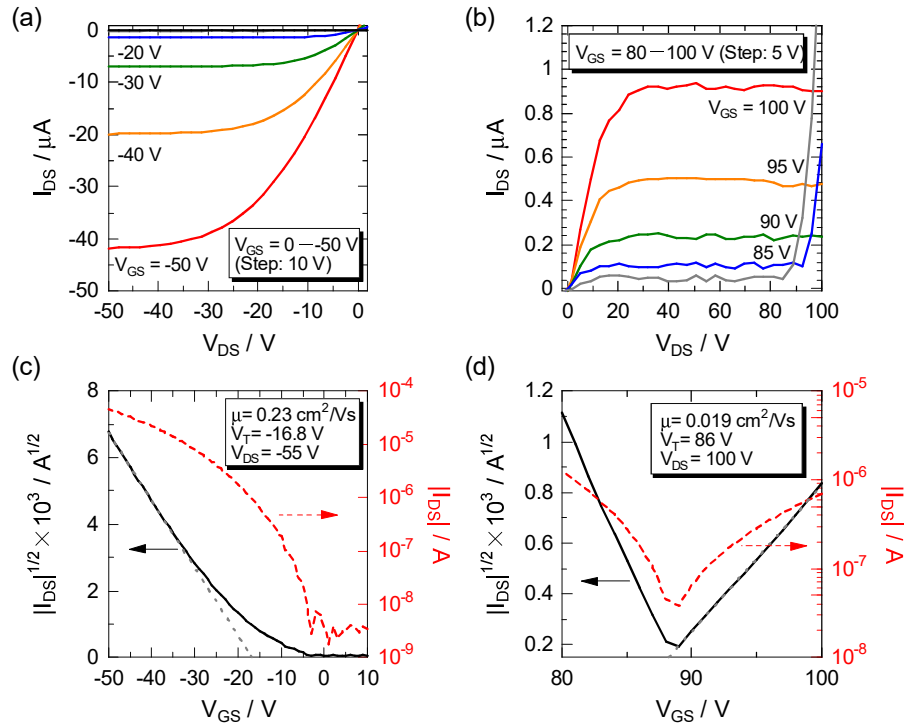


Figure 2. (a)  $I_{DS}$ - $V_{DS}$  curves of the p-channel Pn-FET. (b)  $I_{DS}$ - $V_{DS}$  curves of the n-channel Pn-FET. (c)  $I_{DS}$ - $V_{GS}$  curves of the p-channel Pn-FET. (d)  $I_{DS}$ - $V_{GS}$  curves of the n-channel Pn-FET.

## 4.2 Carrier injection properties from the source electrode

Figure 3 (a) shows the typical  $C$ - $V$  curves with various frequencies of the applied voltage (from 2 Hz to 10 kHz) and (b) indicates the  $C$ - $f$  curves with various  $V_{DC}$  (from -40 V to 40 V). In these measurements,  $V_{AC}$  and  $V_{DC}$  were applied to the Si substrate and only the source electrode was connected to the ground, that is, the drain electrode was electrically floating. Figures 3 (c)-(e) show the schematic illustrations of carrier distributions in various static states.

In Fig. 3 (a), the device is completely depleted for higher positive voltages than 10 V, because holes cannot be injected from the electrode [Fig. 3 (c)]. With sweeping the voltage to the negative side, the capacitance gradually increases below 10 V, except for the curve at 10 kHz. This result suggests hole injection from the source electrode. The capacitance starts to increase again when the negative voltage is applied. Finally, the capacitance of the device becomes constant at higher negative voltage than -25 V in the case that the frequency is 2 Hz. This result clearly indicates that the injected holes spread along the Pn/TTC interface and accumulate over that interface as shown in Fig. 3 (e).

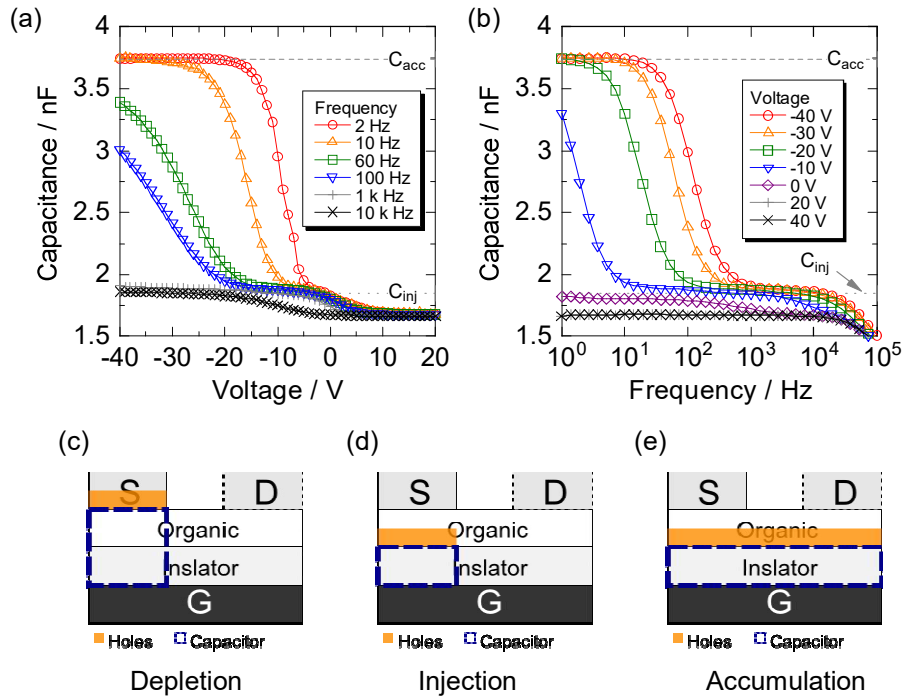


Figure 3. (a) Capacitance-voltage curves with various frequency of applied voltage. The frequencies were changed from 2 Hz to 10 kHz.  $C_{acc} = 3.41$  nF (reading value; dashed line) and  $C_{inj} = 1.85$  nF (estimation from the device structure; dotted line). (b) Capacitance-frequency curves with various  $V_{DC}$ .  $V_{DC}$  was changed from -40 V to 40 V. Schematic illustrations of carrier distribution in: (c) depletion, (d) injection (accumulation just under the source electrode) and (e) accumulation over the organic/insulator interface.

When only the insulator layer works as capacitor dielectric, the value of the accumulation capacitance ( $C_{acc}$ ) reaches 3.74 nF [dashed line in Fig. 3 (a)]. Judging from the area ratio of carrier distribution in Fig. 3 (d) and (e), the value of the injection capacitance ( $C_{inj}$ ) is estimated to 1.85 nF [dotted line in Fig. 3 (a)]. This value corresponds well with the step structure, which appears between depletion and accumulation condition, suggesting that this feature originates from carrier accumulation just under the source electrode as shown in Fig. 3 (d). This result indicates that the injected holes do not spread instantaneously along the Pn/TTC interface due to the difference of the electric potential just under and far from the source electrode<sup>21</sup>.

The difference of speed between carrier injection and spreading is clearly observed by  $C$ - $f$  relationship in Fig. 3 (b). The carrier injection from the source electrode occurs at frequencies higher than  $10^4$  Hz. From  $10^3$  to  $10^4$  Hz, the constant capacitance is observed in the results of  $V_{DS} = -40, -30$  and  $-20$  V. Since this capacitance agrees well with the value of  $C_{inj}$ , this result suggests that carriers, which accumulate under the source electrode, can follow the frequency of the applied voltage. For frequencies lower than  $10^3$  Hz, accumulated carriers farther away from the source electrode start to respond to the applied voltage. Here, the frequency at the inflection point is called the relaxation frequency ( $f_{rel}$ ). Since  $f_{rel}$  of the carrier injection is (at least) 2 decades higher than the frequency of carrier spreading, the carrier accumulation just under the electrode is clearly observed.

### 4.3 Capacitance-voltage relationship in transistor operation

Using the measurement circuit for IS with a battery source for  $V_{DS}$  (Fig. 1),  $C$ - $V$  curves under transistor operation were measured as shown by circles in Fig. 4 (a). The frequency was set to 2 Hz and  $V_{DC}$  (corresponding to  $V_{GS}$ ) was changed from 10 to  $-40$  V. Figure 4 (b) shows the  $I_{DS}$ - $V_{GS}$  curves. The upper triangles shows the results of  $V_{DS} = 0$  V, that is, source and drain electrodes are connected to the ground.

In  $V_{DS} = 0$  V, the carrier injection from both source and drain electrodes occurs almost simultaneously in region (I) [Fig. 4 (a)]. This reason is described as follows. The circles and squares in Fig. 4 (c) show the injection properties from the source electrode (drain electrode is floating in this measurement) and drain electrode (source electrode is floating), respectively. Since the onset voltages of carrier injection and spreading are almost the same (independent of source or drain electrodes), the injection properties observed in region (I) [upper triangles in Fig. 4(a)] are a superposition of injection from source and drain electrode. With negatively increasing  $V_{GS}$ , the capacitance becomes constant due to the carrier accumulation over the Pn/TTC interface. During the  $V_{GS}$  scan, no drain current ( $I_{DS}$ ) is flowing as shown in Fig. 4 (b), because  $V_{DS} = 0$  is applied.

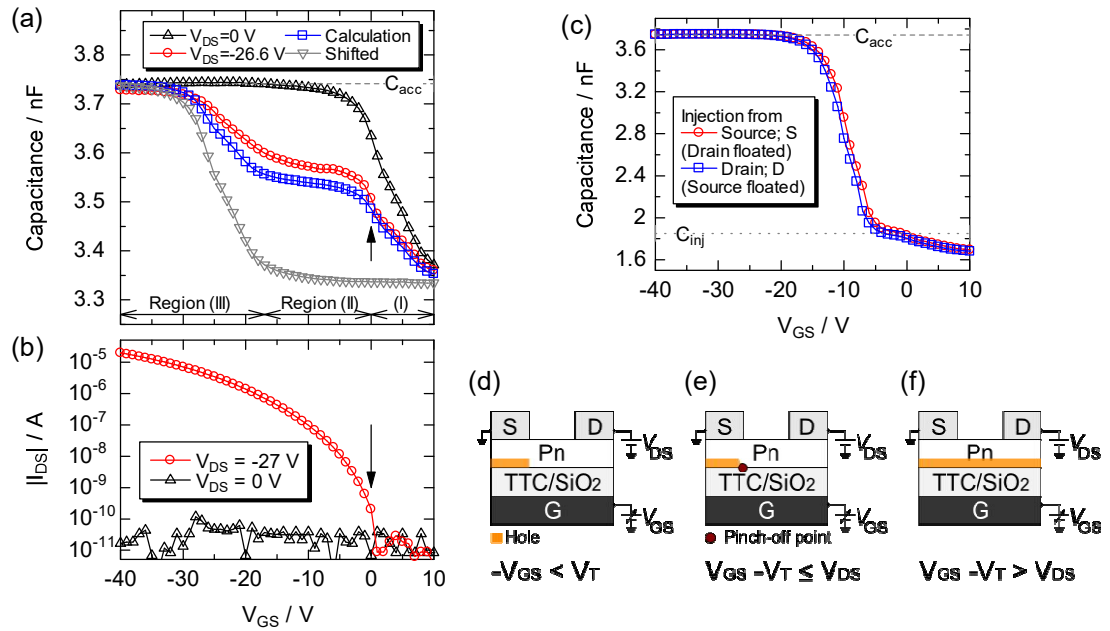


Figure 4. (a)  $C$ - $V$  curves in transistor operation at frequency of 2 Hz [upper triangles:  $V_{DS} = 0$  V, circles:  $V_{DS} = -26.6$  V, squares: (hypothetical) injection properties, lower triangles: shifted curve of the results in  $V_{DS} = 0$ ]. (b)  $I_{DS}$ - $V_{GS}$  curves. (c)  $C$ - $V$  relationships in one electrode (source or drain) floated. Schematic illustrations of carrier distribution in; (d) injection from the source electrode, (e) pinch-off point existing at the source edge and (f) accumulation over Pn/TTC interface.

The circles in Fig. 4 (a) indicate the results at  $V_{DS} = -26.6$  V using a battery source. In region (I), the slope of the variation of capacitance due to carrier injection from the top electrode is different from that at  $V_{DS} = 0$ , because holes are injected now only from the source electrode [Fig. 4 (d)]. In this region,  $I_{DS}$  is not observed as shown in Fig. 4 (b), suggesting that a conducting channel is not yet formed. With scanning  $V_{GS}$  to the negative voltage side, an additional structure, where the capacitance gradually increases, is observed in region (II). In addition,  $I_{DS}$  starts to flow at the beginning of region (II) [arrow in Fig. 4 (b)]. This result indicates that the channel is formed and the OFET changes from the off-state to on-state. Since the capacitance at  $V_{DS} = -26.6$  V is smaller than that at  $V_{DS} = 0$  V, we conclude that a pinch-off point exists at the source electrode edge [Fig. 4 (e)] and  $I_{DS}$  belongs to the saturation region at the beginning of region (II). After that, the capacitance increases again with scanning  $V_{GS}$  towards more negative values and finally becomes constant. Since the injected holes now accumulate over the total interface area [Fig. 4 (f)],  $I_{DS}$  is a property of the linear region.

To observe the channel formation process more clearly, we introduce “hypothetical” injection properties in transistor operation mode by analyzing the results at  $V_{DS} = 0$  V. As mentioned above, the injection properties at  $V_{DS} = 0$  V in region (I) include information about the injection from both source and drain electrodes. Therefore this curve weighted by a factor of 0.5 corresponds to the injection from one electrode. Taking account of p-type OFET operation, the potential of the drain is higher than that of the source by  $V_{DS}$ , which prevents holes from being injected from the drain electrode. Thus, hypothetical injection properties from the drain electrode can be expressed by shifting the results of  $V_{DS} = 0$  V to the negative voltage side by  $|V_{DS}|$  [lower triangles in Fig. 4 (a)]. That is, this curve again multiplied by 0.5 shows the injection properties from the drain electrode in transistor operation. Finally, the addition of the both curves (with the weighting factor 0.5), containing the information about injection properties from source electrode [upper triangles in Fig. 4 (a)] and from drain electrode [lower triangles in Fig. 4 (a)], yields the hypothetical injection properties from both electrodes in transistor operation [squares in Fig. 4 (a)].

In Fig. 4 (a), the measured capacitance in transistor operation (circles) and the one from the proposed injection behavior (squares) almost correspond to each other, because both curves show the correct injection property from the source electrode. At the beginning of region (II), the curve in transistor operation becomes slightly larger than that from injection properties and  $I_{DS}$  starts to flow [arrows in Fig. 4 (a) and (b)]. This result implies that the charge sheet at Pn/TTC interface starts to spread laterally into the channel region. We conclude that the difference between both curves originates from the charge sheet in the channel region. Actually, the capacitance of the channel region is estimated at 35.3 pF from the device structure. This value roughly agrees with the difference from -5 to -12 V (average: 34.1 pF).

This method can become a useful tool to investigate bias stress instabilities of OFETs. As mentioned in the introduction, T. Richards and H. Sirringhaus discussed undesirable threshold voltage shifts, hysteresis, or mobility degradation of FETs<sup>6</sup>. Especially, the application of a negative gate bias causes a negative shift in the threshold voltage<sup>24-27</sup>. To evaluate the origin of these instabilities, it is essential to be able to separate the effects of any contact degradation from that of degradation along the active channel itself<sup>6</sup>. The commonly used techniques for the extraction of contact resistance are the transfer line method, but this technique is complicated by many practical issues mainly due to the morphological characteristics, such as grains and grain boundaries<sup>28</sup>. Since the proposed method in this paper can simultaneously investigate the carrier injection from the electrode and spreading along the channel region in transistor operation, the mobile charges which are the possible cause of the instabilities can be evaluated in detail.

## 5. CONCLUSION

IS was used to investigate the carrier behavior in pentacene based OFET. Carrier injection from the top electrode, accumulation just under the source electrode and along the Pn/TTC interface were clearly observed in  $C$ - $V$  and  $C$ - $f$  curves. We proposed a method for IS in transistor operation by using a battery source for  $V_{DS}$ . An additional structure, where the capacitance gradually increased, was observed between carrier injection and accumulation process. Comparing this result with the analyzed curve, reflecting the carrier injection property from the electrodes, we conclude that the conducting channel was formed in this region, that is, the charge sheet spreads into the channel region. This method enables us to evaluate the carrier injection into the channel region, which is needed for current flow in the OFET, and could be a tool to obtain information about the origin of instabilities in OFETs.

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