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### Angaben zur Veröffentlichung / Publication details:

Pollner, Zsigmond, Tímea Nóra Török, László Pósa, Miklós Csontos, Sebastian Werner Schmid, Zoltán Balogh, András Bükkfejes, et al. 2026. "VO2 oscillator circuits optimized for ultrafast, 100 MHz-range operation." *Advanced Electronic Materials* 12 (1): e00433. <https://doi.org/10.1002/aelm.202500433>.

# VO<sub>2</sub> Oscillator Circuits Optimized for Ultrafast, 100 MHz-Range Operation

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Oscillating neural networks are promising candidates for a new computational paradigm, where complex optimization problems are solved by physics itself through the synchronization of coupled oscillating circuits. VO<sub>2</sub> Mott memristors are particularly promising building blocks for such oscillating neural networks. Until now, however, not only the maximum frequency of VO<sub>2</sub> oscillating neural networks, but also the maximum frequency of individual VO<sub>2</sub> oscillators is severely limited, which has restricted their efficient and energy-saving use. In this study, it is showed how to increase the oscillating frequency by more than an order of magnitude into the 100 MHz range utilizing ultrasmall, ≈30 nm wide active volume VO<sub>2</sub> devices and optimizing the circuit layout for high frequency operation. In addition, the physical limiting factors of the oscillation frequencies are studied by investigating the complex switching dynamics of our nanoscale VO<sub>2</sub> devices. These dynamical studies, together with simulations, provide a clear conclusion on the maximum achievable operating frequencies and the optimal operating parameters under which these can be reached.

the computational or optimization problem into the couplings between oscillators, and then the solution is provided by physics itself through the synchronization of the oscillators into different phase shifts.<sup>[7–9]</sup> This scheme can be implemented with conventional semiconductor circuits such as ring oscillators,<sup>[10]</sup> while relaxation oscillators made from novel memristive nano-devices enable even more compact and energy-efficient oscillator networks.<sup>[11]</sup> The most promising memristive oscillators rely on the nanoscale voltage-induced insulator-to-metal transition in Mott-type NbO<sub>2</sub> or VO<sub>2</sub> memristors.<sup>[12–17]</sup> The latter material system, which is the main focus of the present paper as well, has been successfully used to assemble oscillating neural networks (ONNs), which could solve problems like map coloring

## 1. Introduction

The possibility of performing computational operations by the synchronization of coupled oscillators was originally raised by John von Neumann,<sup>[1,2]</sup> and has since been demonstrated in various physical systems.<sup>[3–6]</sup> This elegant idea is based on encoding

and maximum cut,<sup>[18–20]</sup> gesture recognition,<sup>[21,22]</sup> or feature extraction in convolutional neural networks.<sup>[23,24]</sup>

The building blocks of VO<sub>2</sub> ONNs are simple oscillator circuits, like the scheme illustrated in **Figure 1a**. The oscillation is granted by the hysteretic switching of the VO<sub>2</sub> memristor (blue square) and the resistor in series ( $R_S$ ), while the oscillation

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DOI: 10.1002/aelm.202500433

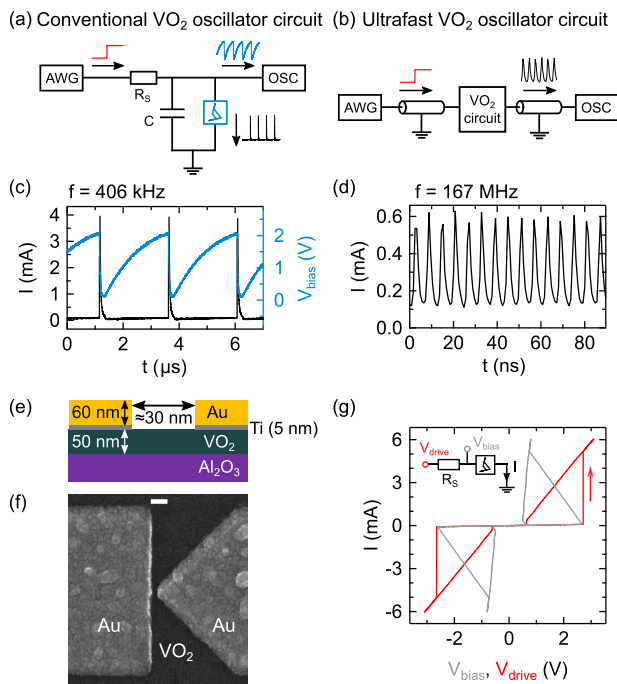
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**Figure 1.** Basics of our low-frequency and high-frequency  $\text{VO}_2$  oscillators. a) Conventional low frequency oscillator circuit with a  $\text{VO}_2$  memristor (blue box), and a series resistor and parallel capacitor. An arbitrary waveform generator (AWG) is used to switch the driving voltage from zero to the desired DC value (red step function), which yields an oscillating current (black) and voltage (blue) signal. The latter is measured by an oscilloscope (OSC). b) Scheme of the high-frequency transmission line oscillator arrangement. c) Low-frequency oscillating waveforms produced by a conventional oscillator circuit (a). The measured oscillating current and voltage signals on the memristor are respectively shown by the black and blue lines. d) Demonstration of the current signal of our highest frequency oscillation ( $f = 167$  MHz). e) Schematic of the memristor device highlighting the small device size and the layer structure (see the Experimental Section for more details). f) Scanning electron micrograph of a representative  $\text{VO}_2$  memristor, scale bar: 100 nm. The V-shaped sample layout focuses the switching to an ultrasmall spot. g) Low-frequency  $I(V)$  graph of a  $\text{VO}_2$  device as a function of driving voltage (red) and the bias voltage (grey) measured on the memristor,  $R_S = 380 \Omega$ . The standard circuit schematic of our low-frequency  $I(V)$  measurements is shown in the inset.

frequency is tunable by the parallel capacitor  $C$ . This circuit produces the typical oscillating voltage (blue) or current (black) signal demonstrated in Figure 1c, once the input signal is switched from zero to a DC level (see red input signal in Figure 1a).

The performance of ONNs is directly influenced by the frequency of the oscillations; higher oscillation frequencies enable faster and more energy-efficient computations, thereby reducing the overall computing time and energy consumption.<sup>[18,25]</sup> According to the state of the art, the oscillation frequency of single  $\text{VO}_2$  oscillators have not yet exceeded the maximum of 9 – 11 MHz,<sup>[15,26]</sup> while  $\text{VO}_2$  oscillating neural networks were usually operated at even lower frequencies, such as 2 kHz<sup>[18]</sup> or 3 MHz<sup>[27]</sup>. In  $\text{TaO}_x$  oscillators a record frequency of 250 MHz was achieved,<sup>[28]</sup> however, in that case the frequency was boosted by an active transistor in the circuit (see the Supporting Information

for a more complete comparison of the oscillation frequencies in various architectures).

In this paper, we investigate the possibility of increasing the operating frequency in circuits that contain only the passive series resistor and parallel capacitance in addition to the Mott memristor. In particular, we demonstrate significantly faster oscillations in  $\text{VO}_2$  devices compared to the previous studies,<sup>[15,26]</sup> as demonstrated by our record 167 MHz oscillation frequency in Figure 1d. This achievement relies on three optimization aspects. (i) For the oscillators we use  $\text{VO}_2$  devices, in which the operation is focused to an ultrasmall, few tens of nanometers wide active region,<sup>[25,29]</sup> while the stray capacitance is minimized. This allows us to exceed theoretical frequency limits established for so-called crossbar  $\text{VO}_2$  devices.<sup>[30]</sup> Similar, strongly confined operation region devices were applied in our previous study to demonstrate the fastest electrically induced  $\text{VO}_2$  switching so far.<sup>[31]</sup> (ii) The oscillator circuit layout is optimized for high-frequency, transmission-line geometry (see illustration in Figure 1b). (iii) The physical limitations of frequency boosting are demonstrated through examining the internal physical relaxation time of the  $\text{VO}_2$  memristor.

These steps are presented as follows. First, the fabrication and characterization of the optimized  $\text{VO}_2$  devices is summarized. Afterwards, the geometric frequency limitations and the optimized circuit layout are motivated by transmission-line geometry LT-spice simulations. Next, we summarize our experimental results on the ultrafast oscillating circuits. Finally, the physical limitations of the oscillation frequency are analyzed through pulsed relaxation-time experiments.

## 2. Results and Discussion

### 2.1. Sample Characterisation and Low-Frequency Measurements

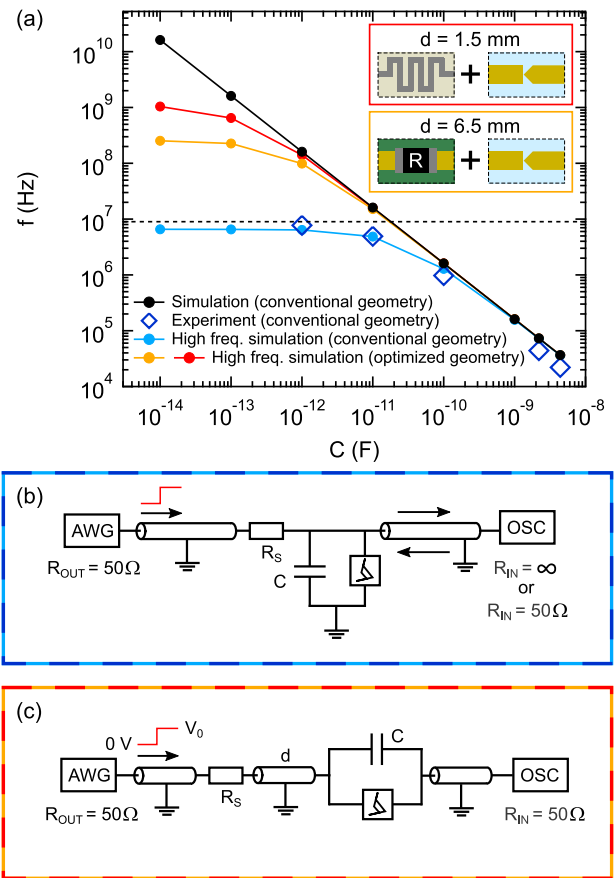
The schematic vertical cross-section of our planar,  $\approx 30$  nm gap size devices is shown in Figure 1e. For the high-frequency experiments, the use of a doped Si substrate would be disadvantageous due to the high stray capacitance toward the substrate, so a well insulating  $\text{Al}_2\text{O}_3$  substrate was applied. The gold top electrodes were patterned on the epitaxial  $\text{VO}_2$  layer by standard electron beam lithography (see the Experimental Section for fabrication and characterization details). A key feature of the structure is the asymmetric lateral geometry (Figure 1f): a rectangular electrode on one side faces a V-shaped electrode on the other side. This geometry enables the production of ultrasmall ( $\approx 30$  nm) gap sizes and the confinement of the active region in an ultranarrow, nanoscale spot<sup>[29]</sup> (note the 100 nm wide scale bar in Figure 1f, while the complete sample layout with a smaller magnification is available in the Experimental Section). This confined geometry is considered crucial for the ultrafast operation, as well as for achieving sufficiently low switching threshold voltages and low switching energies at room temperature.<sup>[31]</sup>

The electrical switching is represented by the  $I(V)$  curves of our devices in Figure 1g where the red trace shows the measured  $I$  current as a function of the drive voltage ( $V_{\text{drive}}$ ) applied to the  $\text{VO}_2$  memristor and the  $R_S = 380 \Omega$  resistor in series, whereas the grey graph is the function of the  $V_{\text{bias}} = V_{\text{drive}} - I \cdot R_S$  voltage drop on the memristor. The inset in Figure 1g illustrates the driving scheme of the  $I(V)$  measurement. This  $I(V)$  curve shows

hysteretic resistance switching. Initially, at zero bias, the device exhibits a high resistance state (HRS), but at the appropriate threshold voltage, an insulator-metal transition (IMT), i.e., a switching to a low resistance state (LRS) is observed. When the voltage drops back to zero, the switchback, i.e., the metal-insulator transition (MIT), occurs at a lower threshold voltage. Hereinafter, the insulator-metal and metal-insulator transitions are referred to as the set and reset transitions, respectively. The corresponding threshold voltages are denoted by  $V_{set}$  and  $V_{reset}$ . We note that no dedicated electroforming process is required for the observation of such  $I(V)$  curves, the as-prepared samples already exhibit switching at the same threshold values as the further measurements.

Applying an even larger resistance in series ( $R_S > 4500 \Omega$ ) a self-oscillation of the  $VO_2$  memristor can be induced by a constant  $V_{drive} = V_0$  driving voltage. In this case the  $I = (V_0 - V_{bias})/R_S$  load line does not cross the  $I(V_{bias})$  curve at stable states, i.e., the set transition occurs prior to the establishment of the stable voltage in the HRS, but then the bias voltage is released due to the voltage division by the series resistor and the system switches back to the HRS before reaching the stable voltage in the LRS. This process yields the self-oscillating behavior, for which the frequency can be tuned by a parallel capacitor  $C$ . In practice, this is realized in the circuit scheme of Figure 1a: applying a step function from an arbitrary waveform generator (AWG) on this circuit (red line in Figure 1a), i.e., increasing the drive voltage from zero to a sufficient DC value, yields an oscillating operation at the output (blue illustration Figure 1a), which can be measured by an oscilloscope (OSC). The measured periodic oscillation of the voltage (blue) and current (black) signal is exemplified in Figure 1c.

In such a conventional  $VO_2$  oscillator circuit (Figure 1a) the oscillation frequency is expected to be an inverse function of the  $C$  parallel capacitance, as shown by the results of simple circuit simulations (Figure 2a black curve). In these simulations the  $VO_2$  memristor is treated as a simple hysteretic switch with  $V_{set}$  and  $V_{reset}$  set and reset voltages and  $R_{M,HRS}$  and  $R_{M,LRS}$  resistances in the insulator HRS and the metallic LRS of the memristor (see the Experimental Section for details of the simulations). In practice, the parallel capacitance is limited by the stray capacitance of the device, which can be reduced to the level of a few femtofarads by careful sample design.<sup>[31]</sup> According to our simple simulations, a correspondingly chosen  $\approx 10^{-14}$  F minimal parallel capacitance would yield  $\approx 10$  GHz oscillation frequencies, while a conventionally achievable  $\approx 10^{-12}$  F parallel capacitance would result in  $\approx 100$  MHz oscillations (see black line in Figure 2a). These oscillation frequencies would highly exceed the current world record of 9 – 11 MHz (horizontal dashed line in Figure 2a) demonstrated in the fastest  $VO_2$  oscillator circuits so far.<sup>[15,26]</sup> Our experiments with the oscillator circuit of Figure 1a result in the dark blue rectangles in Figure 2a, which also show a significantly slower experimental oscillation in the low capacitance range than expected (i.e. compared to the black curve). This deviation is understood through high-frequency simulations in the next Section. Afterwards, using a circuit layout



**Figure 2.** Simulation of the oscillation frequencies using various circuit arrangements. a) Oscillation frequencies as the function of the parallel  $C$  capacitance in comparison to the highest 9 MHz oscillation frequency achieved so far (black dashed line).<sup>[26]</sup> The black curve illustrates the simulated oscillation frequencies for a conventional  $VO_2$  oscillator circuit (see Figure 1a) such that the finite signal propagation speed in the cables is not taken into account at all. The same circuit arrangement yields the light blue curve once the cable between the circuit and the high-impedance OSC is treated as a transmission line (see panel (b)) with 0.25 m length and  $v = 2 \cdot 10^8$  m/s propagation speed.<sup>[32]</sup> Note the low-pass filter nature of the oscilloscope-cable pair. These simulated frequency values are consistent with our experimental results (dark blue squares) measured in the arrangement of panel (b). The orange and red curves correspond to the in-line oscillator arrangement of panel (c). This arrangement is optimized for high-frequency operation such that only the finite memristor-to-resistor distance  $d$  is the limiting factor for the maximum achievable frequencies. This distance is respectively set to  $d = 6.5$  mm and  $d = 1.5$  mm for the orange and red curves. In the simulations experimentally reasonable circuit parameters of  $R_S = 22$  k $\Omega$ ,  $R_{M,HRS} = 28$  k $\Omega$ ,  $R_{M,LRS} = 180 \Omega$ ,  $V_0 = 5$  V,  $V_{set} = 2.4$  V and  $V_{reset} = 0.45$  V are applied. The orange- and red-framed insets illustrate possible experimental realizations of different distances:  $d = 6.5$  mm is easily realized on a printed circuit board with a surface-mounted resistor, while  $d = 1.5$  mm, or even smaller, sub-mm distances already prefer an integrated on-chip resistor, like a meander-shaped platinum wire. b) Conventional oscillator circuit, but the cables to the AWG and OSC are considered as transmission lines. c) In-line oscillator circuit arrangement optimized for high-frequency operation, where every cable is modeled as a transmission line.

optimized with the help of the simulations in Section 2.2, we experimentally demonstrate the realization of ultrafast oscillations (Section 2.3).

## 2.2. Oscillator Circuit Layout Optimized for High-Frequency Operation

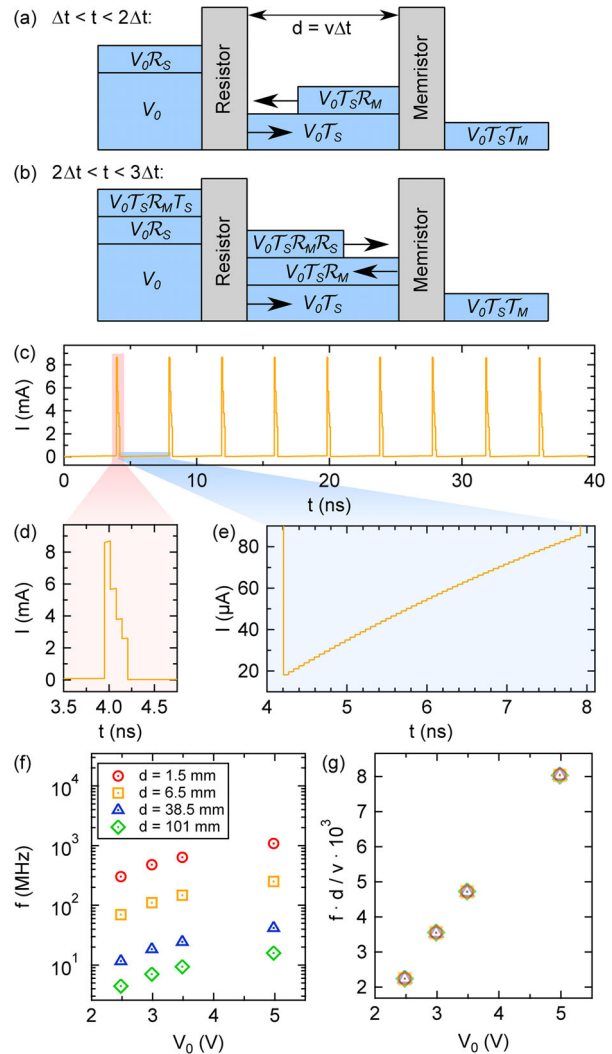
In order to achieve our main goal, a significant increase in oscillation frequency, it is essential to understand the effects of finite signal propagation speed on the operation of the oscillator circuit and to optimize our circuit accordingly. We do this using high-frequency LTspice simulations. In these, we keep considering the VO<sub>2</sub> device as a simple hysteretic switch with  $R_{M, HRS}$  and  $R_{M, LRS}$  resistances and  $V_{set}$  and  $V_{reset}$  threshold voltages, but we treat the cables connecting the circuit elements as 50 Ω transmission lines, in which the signal propagates with  $v \approx 2 \cdot 10^8$  m/s speed (see the Supporting Information for the details of the transmission line geometry LTspice simulations).

First, we simulate the conventional oscillating circuit in Figure 1a, but the cables connecting the oscillator circuit to the arbitrary waveform generator (AWG) and the oscilloscope (OSC) are treated as transmission lines (Figure 2b). The light blue curve Figure 2a demonstrates the simulated oscillation frequencies as a function of the parallel capacitance  $C$ . Already a 0.25 m long cable between the high-impedance input oscilloscope and the oscillator circuit yields a severe frequency limitation (see the deviation of the light blue and black curves in Figure 2a) due to the delayed return of the signal being reflected at the oscilloscope. On the other hand, an impedance-matched 50 Ω input of the oscilloscope would result in shunting of the oscillator circuit, which would completely disable the oscillating operation.

To avoid the above difficulties in the high frequency regime, further on we apply the modified, in-line oscillator scheme of Figure 2c, where the impedance-matched oscilloscope with 50 Ω input impedance measures the current signal transmitted through the oscillator circuit ( $I = V_{OSC}/50\Omega$ ). At the other side, an AWG with 50 Ω output impedance drives the circuit. This impedance matching is essential to avoid signal reflections at the AWG and OSC. In this case the lengths of the transmission lines between the oscillator circuit and the AWG or OSC are not relevant for the frequency of the oscillation. As a price, we cannot measure the voltage drop on the VO<sub>2</sub> element, just a signal proportional to the current is detected. On the other hand, the finite distance  $d$  between the series resistor and the VO<sub>2</sub> sample becomes a crucial factor. This part of the circuit is also modeled as a transmission line.

In this optimized circuit arrangement the simulated capacitance-dependent oscillation frequencies readily reach values above 100 MHz for  $d = 6.5$  mm distance, which can be easily realized with a memristor chip and an SMD resistor on a printed circuit board (see the orange trace in Figure 2a and the the orange-framed inset). Even higher, 1 GHz oscillation frequencies are predicted once the memristor-resistor distance is reduced to the  $d = 1.5$  mm range, which arrangement, however, already prefers an integrated on-chip resistor (see the red trace in Figure 2a and the red-framed inset).

Obviously, the highest oscillation frequencies occur at the lowest capacitance values. For this reason, in the following para-



**Figure 3.** Simulated oscillating time-traces in the high-frequency domain, and the scaling of the oscillation frequencies with the memristor-to-resistor distance. a,b) Illustration of the voltage-build-up in the circuit. At time  $t = 0$  a step-function excitation  $0 \rightarrow V_0$  arrives to the resistor in series. Panel (a) illustrates the  $\Delta t < t < 2\Delta t$  time interval, when the signal transmitted through the resistor has already arrived at the memristor and has been partially reflected by it, but has not yet returned to the resistor. Panel (b) similarly illustrates the  $2\Delta t < t < 3\Delta t$  time interval. c) Example simulated oscillating current signal with 251 MHz oscillation frequency. d,e) Magnified segments of panel (c) illustrating the step-wise current evolution along the reset (d) and set (e) transition. f) Simulated oscillation frequencies as a function of the  $V_0$  oscillator drive voltage with different markers displaying different memristor-to-resistor distances (see legends). g) Once the oscillation frequencies are normalized to the  $1/\Delta t = v/d$  inverse signal propagation time, the frequency values demonstrated in panel (f) collapse to a single curve. The same simulation parameters are used as in Figure 2.

graphs we analyze the operation of the predicted circuit in the absence of a parallel capacitor  $C$ , by considering only the frequency limitation caused by the finite memristor-to-resistor distance. The results of these simulations are shown in Figure 3f, with the different colors showing the simulated oscillation frequencies at different distances  $d$  (see legends), while the horizontal

axis shows the variation of the oscillation frequencies with the constant oscillator drive voltage  $V_0$ . Note that here  $V_0$  is the amplitude of the  $0\text{V} \rightarrow V_0$  voltage step (see the red illustration in Figure 2c) that the AWG outputs to the coaxial line with  $50\ \Omega$  wave impedance, which practically results in a  $2V_0$  DC voltage in the coaxial line due to the large reflection from the series resistor. These simulations show that an oscillator with a  $d = 6.5\text{ mm}$  of memristor-to-resistor spacing can produce frequencies in the range of our highest experimentally observed oscillations (see the  $167\text{ MHz}$  oscillation in Figure 1d) when operated with a sufficiently high drive voltage  $V_0$ . As  $d$  is increased or  $V_0$  is decreased, the oscillation frequencies gradually decrease. However, if  $d$  is further reduced, the predicted oscillation frequencies become even higher, but as will be shown later, this regime is subject to further experimental limitations.

Note that the above  $100\text{ MHz}$ -range frequencies at  $d = 6.5\text{ mm}$  memristor-to-resistor distance (orange squares in Figure 3f) correspond to a  $\Delta t = d/v \approx 32\text{ ps}$  signal propagation time from the resistor to the memristor, where  $v \approx 2 \cdot 10^8\text{ m/s}$  is the signal propagation speed in the transmission lines. This short propagation time seemingly contradicts the two orders of magnitude larger period time of the oscillation at  $\approx 100\text{ MHz}$  frequency. This apparent discrepancy is resolved by a detailed calculation of the voltage build-up on the memristive element. We assume that at time  $t = 0$  the voltage changes from zero to a constant  $V_0$  value on the AWG and analyze how this signal propagates through the circuit (see Figure 3a,b). This step-function first arrives to the resistor in series ( $R_S$ ), where it is partially transmitted (reflected) with a transmission coefficient  $\mathcal{T}_S$  (reflection coefficient  $\mathcal{R}_S$ ). The reflected signal is fed back to the AWG where it is absorbed by the  $50\ \Omega$  output impedance. The transmission and reflection coefficients are calculated from the solution of the telegrapher's equations as,

$$\mathcal{T}_S = 1 - \mathcal{R}_S = 2Z_0 / (R_S + 2Z_0) \quad (1)$$

where  $Z_0 = 50\ \Omega$  is the wave impedance of the transmission lines.<sup>[33]</sup> The transmitted signal is then propagated to the memristor, where the signal is partially transmitted (reflected) with a transmission coefficient  $\mathcal{T}_M$  (reflection coefficient  $\mathcal{R}_M$ ). These coefficients are obtained from the actual  $Z_M$  memristor impedance as,

$$\mathcal{T}_M = 1 - \mathcal{R}_M = 2Z_0 / (Z_M + 2Z_0) \quad (2)$$

where  $Z_M$  can be replaced by the  $R_M$  memristor resistance due to the negligible capacitive impedance compared to the resistance over the frequency range of the measurement. This is underpinned by the measured  $C = 2\text{ fF}$  stray capacitance of our devices,<sup>[31]</sup> which is significantly smaller than the  $\approx 55\text{ fF}$  capacitance, at which we would start to expect signal distortion at our typical devices resistances and our  $1\text{ GHz}$  measurement bandwidth (see Section S1 of the Supporting Information for the more detailed analysis of the stray capacitance). The partial signal wave transmitted through the memristor is eventually propagated to the OSC, where it is absorbed by the  $50\ \Omega$  input impedance. Due to the large series resistance  $R_S$ , only a very small fraction of the voltage  $V_0$  reaches the memristor in the first turn, i.e., a large

number of back and forth bounces are required to reach the  $V_{\text{set}}$  voltage drop on the memristor where the set transition occurs. This voltage build-up time can be calculated analytically as follows:

$$\tau_{0 \rightarrow V_{\text{set}}} = \frac{d}{v} \left[ \frac{\ln \left( 1 - V_{\text{set}} \cdot \frac{1 - \mathcal{R}_M \mathcal{R}_S}{2V_0 \mathcal{T}_S \mathcal{R}_M} \right)}{\ln (\mathcal{R}_M \mathcal{R}_S)} - 1 \right] \quad (3)$$

(see Section S2 of the Supporting Information for the derivation of Equation 3). Applying experimentally reasonable values of  $d = 6.5\text{ mm}$ ,  $R_S = 22\text{ k}\Omega$ ,  $R_{M, \text{HRS}} = 28\text{ k}\Omega$ ,  $V_0 = 5\text{ V}$  and  $V_{\text{set}} = 2.4\text{ V}$ , a voltage build-up time of  $2.2\text{ ns}$  is obtained, which corresponds to a signal bouncing back and forth 68 times between the resistor and the memristor. The above analytical formula describes the voltage build-up from zero to  $V_{\text{set}}$ , but similar voltage build-up times are also delivered by the LTSpice simulations of a periodic oscillation (see Figure 3c). The magnified figures of the reset (Figure 3d) and set (Figure 3e) transitions clearly demonstrate the step-wise voltage build-up, where the number of discrete steps correspond to the number of bounces between the resistor and the memristor. Figure 3d shows a rather fast reset process after the set transition. This is related to the low memristor resistance, which allows a fast release of the voltage across the memristor. However, after the reset process, the next set transition requires a large number ( $\approx 57$ ) of back and forth bounces, as shown in Figure 3e. This explains why the oscillation frequency is eventually much lower than the  $1/\Delta t \approx 31.25\text{ GHz}$  inverse propagation time.

Finally, it is important to recognize another crucial property of the oscillations from these simple model calculations. By increasing the distance  $d$  and the corresponding propagation time  $\Delta t = d/v$ , we slow down the oscillation curves linearly along the time axis only. This means that a normalized, unitless  $t \cdot v/d$  time axis, or the equivalent normalized  $f \cdot d/v$  frequency axis, result in the collapse of the data of different distances  $d$  into a single curve. This is shown in Figure 3g, where the such normalized frequency values indeed collapse on the same curve showing the same dependence on  $V_0$ . This property can be clearly seen from Equation 3 as well, where the voltage build-up time scales linearly with  $\Delta t = d/v$ , and the rest of the equation does not depend on  $d$ .

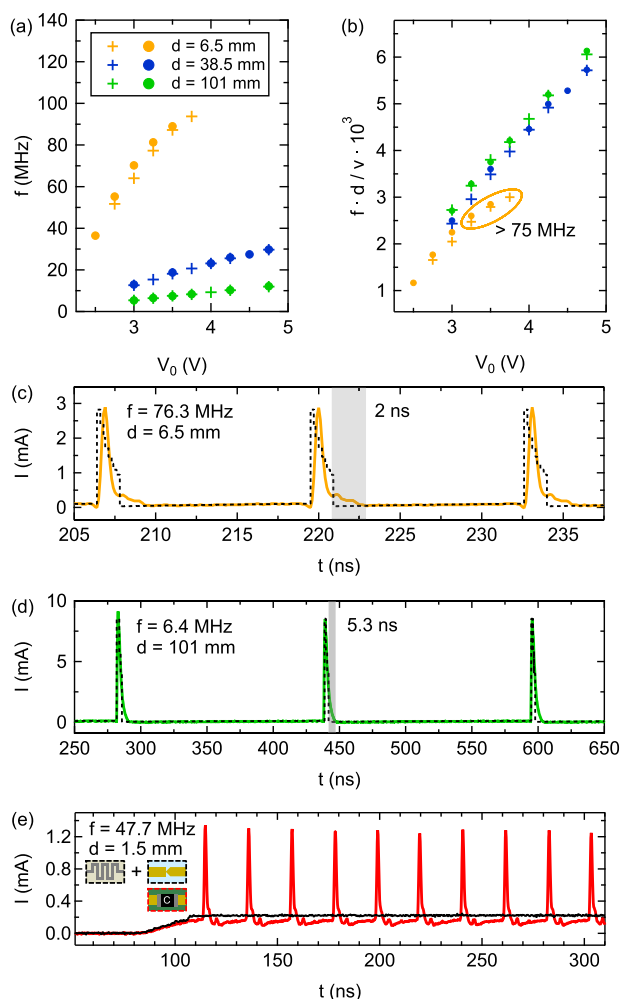
Concluding our simulations in this Section, we have proposed an optimized in-line circuit layout for high frequency oscillations (Figure 2c) instead of the conventional low-frequency oscillator circuit layout (Figure 1a). Using this layout, the simulations indeed predict ultrafast oscillations with asymmetric current traces, i.e., short current pulses prior to the reset transition, and much longer low current segments prior to the set transition (Figure 3c). The latter are almost two orders of magnitude longer than the  $\Delta t$  resistor-to-memristor signal propagation time due to the large number of back-and-forth signal bounces prior to the build-up of the set voltage. The latter phenomenon introduces a fundamental frequency limitation at finite resistor-to-memristor distances. Finally, we have highlighted a universal scaling of the simulated frequency versus driving voltage dependencies (Figure 3g).

### 2.3. Experimental Demonstration of Ultrafast Oscillations

Equipped with the above finite signal propagation speed simulations, we explore the experimental possibility of ultrafast oscillations. We have built oscillator circuits using our nanosized VO<sub>2</sub> samples and the optimized circuit layout of Figure 2c. The circuit is established using an  $R_S = 22 \text{ k}\Omega$  SMD series resistor assembled along a transmission line on a printed circuit board (see the details of the experimental setup in the Experimental Section). The series resistors were placed at distances  $d = 6.5, 38.5, 101 \text{ mm}$  from the memristor, and the respective time-traces (solid lines in Figure 4c,d) and the related oscillation frequencies (Figure 4a,b) were measured. These experimental data show great similarity to our simulations discussed above, but also show some fundamental differences. This comparison allows us to separate the phenomena resulting from the finite signal propagation speed considered in the simulations from additional features resulting from the complex switching dynamics of real VO<sub>2</sub> devices.

First, the time-traces (Figure 4c,d) show a similar asymmetric pattern, where the system stays shortly in the LRS, but after the reset process, the next set transition requires a long time compared to the width of the sharp peaks, where the system stays in the LRS. Second, the dependence of the oscillation frequencies on  $d$  and  $V_0$  (Figure 4a,b) show similar trends as the simulated oscillations (Figure 3f,g). In particular, after normalizing the frequencies ( $f \cdot d/v$ ), the measurements at different distances mostly fall on the same curve (Figure 4b). However, at the highest frequencies this scaling fails (see the deviation of the orange datapoints from the rest of the data at higher  $V_0$  values, i.e., the orange encircled measurements). Note that all these significantly deviating datapoints correspond to  $>75 \text{ MHz}$  oscillation frequencies. This implies that for the fastest oscillations the frequency is not limited by the memristor-resistor distance, rather some other time-scale, like the internal relaxation time of the memristor becomes important. The same tendency is also seen in Figure 4c,d, where the measured time-traces (solid lines) are compared to black simulated traces with similar operation characters. This comparison highlights a clear difference at the falling edges after the current peaks: whereas the simulations always show a sharp reset, in the experiment the falling edges exhibit extended tails, which we also attribute to an internal relaxation time of the memristor. These tails extend over the time-scale of a few nanoseconds, as illustrated by the light gray shaded areas. This phenomenon becomes important if the oscillation period is comparable to the duration of this tail region.

The previous observations indicate the interplay of geometry-induced voltage build-up times and internal physical relaxation times in determining the fastest possible oscillation frequencies. From this point of view it is interesting to explore devices, where the memristor-to-resistor distance is even smaller. To this end, we have fabricated memristor devices with integrated meander-shaped resistor in series yielding  $d \approx 1.5 \text{ mm}$  (see the Experimental Section for more details). For such short distance the simulations in Figure 2a predict  $>1 \text{ GHz}$  oscillation frequencies. As a sharp contrast, for such spatially confined devices we



**Figure 4.** Experimentally observed ultrafast oscillations. a) Measured oscillation frequencies at various memristor-to-resistor distances ( $d$ , indicated by the legend) and drive voltages ( $V_0$ ) are displayed. We plotted two measurement cycles, marked with cross and circle symbols, to demonstrate reproducibility. In one cycle, the voltage is increased at a given distance; then, the distance is increased to the next value. After measuring at all distances in the first cycle (marked with crosses), the whole procedure was repeated (marked with circles). b) Once the oscillation frequencies are normalized to the  $1/\Delta t = v/d$  inverse signal propagation time, the frequency values demonstrated in panel (a) collapse to a single curve similarly to the simulations (Figures 3f,g). This scaling only fails at the highest frequencies above 75 MHz (see orange encircled measurements). c,d) Measured oscillating time-traces (solid lines) in comparison to simulated time-traces with similar characters (black dashed lines). The experimental traces exhibit an extended tail region during the reset process, as illustrated by the gray shaded areas with the indicated widths. The distances  $d$  and the oscillation frequencies  $f$  are indicated in the panels. e) Investigation of oscillator circuits with an integrated, meander-shaped resistor with  $R_S = 30 \text{ k}\Omega$  in series. The meander's center is at  $190 \mu\text{m}$  distance from the device active region, while the path length from the meander's center to the device active region is  $1.5 \text{ mm}$ . The black curve illustrates the measurement without a parallel capacitor: in this configuration, integrated samples with ultra-small  $d$  systematically fail to oscillate (see black curve). With the insertion of a  $C = 1 \text{ pF}$  parallel capacitor the oscillatory behavior is recaptured (red curve).

have systematically not observed oscillatory behavior, rather the system reaches a steady state when the  $V_0$  voltage is applied (black line in Figure 4e). If, however, the device operation is artificially slowed down by a  $C = 1$  pF parallel capacitor, the oscillating operation can be recovered (red line in Figure 4e). We explain this as follows. During oscillation, when the  $V_{\text{set}}$  value is reached, the resistance decreases and thus the voltage also drops below  $V_{\text{set}}$ , while when the  $V_{\text{reset}}$  value is reached, the resistance increases and thus the voltage rises above  $V_{\text{reset}}$ . However, a rapid distancing from the switching voltage can lead to incomplete set and reset transitions, and the system would stick to some stable state instead of an oscillation. However, a properly chosen parallel capacitor, or a properly distant resistor in series helps to slow down the voltage variation in the circuit, such that after reaching the set (reset voltage) these voltage levels are kept for a while to ensure a complete set (reset) transition for the oscillation. To support the above explanation, we constructed Matlab Simulink simulations where the set and reset switching timescales of the memristors are modeled through equations for the time derivative of the device resistance. These simulations reproduce the experimentally reached 167 MHz frequency maximum (see Section S3, Supporting Information), and also illustrate the role of delayed voltage build-up in stabilizing the oscillation. The latter is demonstrated in Sections S4 and S5 (Supporting Information) conclusively reproducing the phenomenon seen in Figure 4e. According to the above arguments, the fastest oscillation is achieved when the internal relaxation time of the memristor matches the time-scale at which the finite  $d$  distance or the  $C$  parallel capacitor keeps the voltage close to the set or reset voltage value once these are reached along the oscillation.

Following these considerations, we investigate the realistic internal relaxation time-scales of our devices, which play a fundamental role in determining the maximum possible oscillation frequency.

#### 2.4. Investigation of the Internal Relaxation Time-Scales

Using  $\text{VO}_2$  memristors with the same geometry as the one tested here, we have demonstrated set times below 15 ps and reset times below 600 ps,<sup>[31]</sup> which would allow oscillation frequencies up to above GHz. However, these shortest switching time values were achieved under optimized conditions. The 15 ps set time was demonstrated with an ultrashort, 20 ps FWHM switching pulse of amplitude significantly exceeding the set threshold voltage, while the 600 ps reset time was achieved with the least invasive measurement, i.e., the set transition was performed with the lowest possible meaningful set pulse, after which the voltage was immediately taken off the sample and the time it takes for the system to relax to the HRS was scanned with ultra-short (20 ps) readout pulses.

In what follows, we argue that significantly longer set/reset times than these can be experienced under less optimized conditions, which are unavoidable during oscillating operation. Most importantly, in  $\text{VO}_2$  oscillator circuits, the maximum and minimum voltages available are mainly determined by the set voltage and the reset voltage, as explained below. As soon as the set voltage is reached on the  $\text{VO}_2$  device, the resistance starts to decrease

(set transition), so the device voltage also starts to decrease due to the voltage division with the series resistor. Likewise, as the voltage decreases to the reset voltage, the resistance of the sample starts to increase (reset transition), so the voltage across the sample also starts to increase. Although minor overshoots or undershoots are possible due to the finite voltage build-up time, in principle, no voltages significantly higher (lower) than  $V_{\text{set}}$  (and  $V_{\text{reset}}$ ) can be obtained on the  $\text{VO}_2$  sample during oscillation.

In an oscillator circuit, however, the driving conditions are constantly changing, making it difficult to directly study the switching times and their dependence on the driving parameters. To overcome this difficulty, we prefer to investigate the switching times by pulsed measurements, where the driving conditions are well controlled, while the pulsed current variation still somewhat resembles the oscillating time-traces. Specifically, oscillatory operation is mimicked by using a series of pulses whose amplitude is close to the set transition, while the constant voltage between the pulses represents a level close to the reset transition.

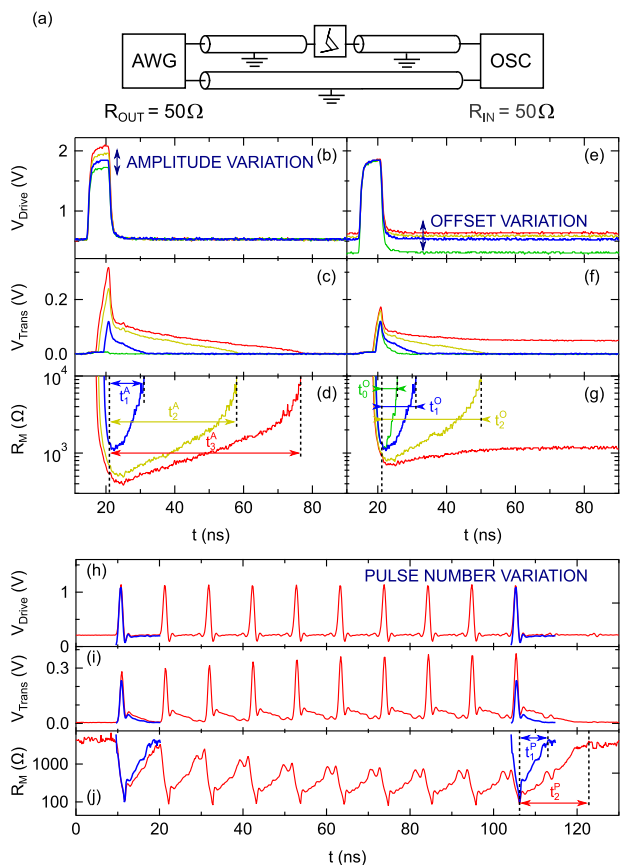
The scheme of our measurement is sketched in Figure 5a. In these experiments the AWG outputs ultrashort voltage pulses ( $V_{\text{Drive}}(t)$ ) instead of a step function, which are measured directly by one channel of the oscilloscope. The same pulses are driving the memristor sample from the other output channel of the AWG, and the pulses transmitted through the sample ( $V_{\text{Trans}}(t)$ ) are measured at another channel of the OSC (see further details of the experimental setup in the Experimental Section). In this scheme, no resistor in series is applied, but the switching dynamics of the memristor sample alone is tested.

Note that the transmission coefficient in Equation 2 would yield a frequency-dependent transmission for a capacitive or inductive  $Z_M$  memristor impedance, but for a dominantly resistive  $Z_M = R_M$ , which is the case in our measurements (see discussion after Equation 2), the transmission coefficient is frequency independent. This property ensures that an incoming wave-package, such as a pulse, preserves its shape along the transmission, only its amplitude is modified, as long as  $R_M$  is constant in time. Or, inversely, the temporal variation of the memristor resistance can be directly traced from the ratio of the transmitted and incoming (driving) signals:<sup>[31]</sup>

$$R_M(t) = 2Z_0 \cdot \left( \frac{V_{\text{Drive}}(t)}{V_{\text{Trans}}(t)} - 1 \right) \quad (4)$$

Note, that the transmitted voltage signal is directly proportional to the memristor current as  $V_{\text{Trans}}(t) = I(t) \cdot Z_0$ . Figure 5b–d, Figure 5e–g, and Figure 5h–j respectively demonstrate the  $V_{\text{Drive}}(t)$  driving waveforms output from the AWG (top panels), the  $V_{\text{Trans}}(t)$  transmitted waveforms (middle panels) measured at the OSC and the  $R_M(t)$  temporal variation of the memristor resistance calculated from Equation 4 (bottom panels) for various driving signals. The bottom panels are cut at  $10^4 \Omega$ , a resistance slightly below our resolution limit due to the finite 8 bit resolution of our OSC.

In Figure 5b–d and Figure 5e–g, we investigate the response of the memristive sample to single driving pulses with variable pulse amplitudes and offset voltages between the pulses. Our primary focus is on the blue curve (the same in the right and left panels), where the pulse amplitude and offset are adjusted close to the set and reset voltage. The green curves in Figure 5b,c shows



**Figure 5.** Investigation of the physical relaxation times by pulsed experiments. a) The scheme of the measurement setup. b) Driving pulses for our experiments with variable pulse amplitude and fixed voltage offset, with pulse amplitudes of 1.7 V (green curve), 1.85 V (blue curve), 1.95 V (yellow curve), 2.1 V (red curve). c) Transmitted voltage through the VO<sub>2</sub> sample as measured by the oscilloscope. The time axis of panels (b) and (c) are aligned to eliminate the finite propagation times in the coaxial lines connecting to the AWG and OSC. d) The memristor resistance  $R_M(t)$  evaluated according to Equation 4. e–g) Driving pulses for our experiments with fixed pulse amplitude and variable voltage offsets of 0.31 V (green curve), 0.53 V (blue curve), 0.59 V (yellow curve), 0.64 V (red curve), (e) together with the corresponding transmitted voltage pulses (f), and the calculated  $R_M(t)$  traces (g). h–j) Experiments with single driving pulses (blue) and ten times repeated driving pulses (red) (h) together with the corresponding transmitted voltage pulses (i), and the calculated  $R_M(t)$  traces (j). For comparison, the single pulse measurements (blue) are also replotted at the time of the tenth repetitive pulse (red).

that a slightly smaller pulse amplitude no longer turns the sample to the LRS, while the red curves in Figure 5e–g demonstrate that by applying a slightly higher offset voltage, the system is already stuck in the LRS without switching to the HRS.

To define a comparable measure for the duration of the set and reset transitions at the different driving conditions, we measure the set time as the time between the middle of the rising edge of the drive pulse and reaching <2 kΩ resistance, while the reset time is the time between the middle of the falling edge of the drive pulse and reaching >10 kΩ resistance. The latter relaxation times are denoted by the correspondingly colored arrows in the

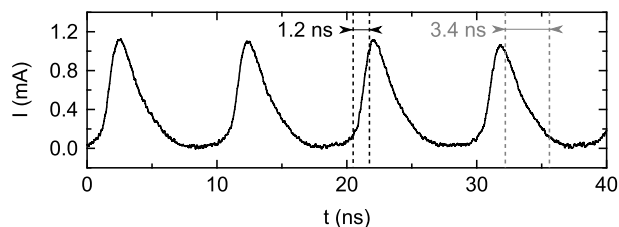
figure. For the blue reference measurement the above definitions yield a set time of 5.4 ns and a reset time of  $t_1^A = t_1^O = 9.6$  ns.

Next, we investigate how these times vary by changing the pulse amplitude and the offset voltage. Once the pulse amplitude is increased compared to the blue curve (see the yellow and red curves in Figure 5b–d) the set time respectively decreases to 3.7 ns and 2.8 ns, while the reset time significantly increases to  $t_2^A = 36.4$  ns and  $t_3^A = 54.4$  ns, respectively. On the other hand, the minor increase of the offset voltage (yellow and red curves in Figure 5e–g) yields minor variation of the set time, while the reset time shows a significant increase ( $t_2^O = 28.8$  ns for the yellow curve, and  $\gg 100$  ns for the red curve). We also tested a significantly lower offset voltage than the blue curve (green curve), which reduces the reset time to  $t_0^O = 4.4$  ns. The latter value is still much longer than the fastest 600 ps relaxation at zero offset voltage,<sup>[31]</sup> while the offset voltage corresponding to the green curve is already unrealistically small for an oscillator operation. This means that the above  $t_0^O = 4.4$  ns reset time is a lower estimate of the relaxation time achievable under oscillator conditions in this particular case.

The above experimentally determined set and reset time values can be compared with our finite element simulations of the electrothermal dynamics (see the Section S10, Supporting Information). These simulations follow a similar protocol to our previous work,<sup>[29]</sup> but the actual thermal parameters are adjusted to the characteristics of the device with high-frequency operation whose  $I(V)$  curve is presented in Figure 1g. These simulations show set times consistent with the experiments, demonstrating that 10 ps-scale set times are expected for large driving pulse amplitudes of  $V_{\text{Drive, max}} \approx 3 \cdot V_{\text{set}}$ , while the set time increases to several nanoseconds as the pulse amplitude approaches the set voltage (see Figure S10b, Supporting Information, and its description). The simulations also clearly show that larger devices or substrates with poorer thermal conductivity slow down the set transition. On the other hand, the simulation of the reset transition is more challenging, and simple simulations provide significantly shorter reset times compared to the experiments. This discrepancy suggests that additional mechanisms contribute during reset, such as elastic energy stored in grains, which can stabilize metallic regions for a period even when the temperature is below the phase-transition threshold.<sup>[34]</sup>

So far, in Figure 5b–g the response to single driving pulses was tested. Next, we demonstrate that the relaxation time is also very sensitive to the number of applied driving pulses (Figure 5h–j). In these experiments, a relaxation time of  $t_1^P = 6.8$  ns is measured after a single  $\approx 1.1$  ns long driving pulse (blue curves), while the 10 times repetition of the same driving pulse with 10.6 ns period time (red curves) yields a relaxation time of  $t_2^P = 16.6$  ns after the last pulse. Here, the single blue pulse is replotted at the time of the 10<sup>th</sup> pulse for comparison. Here, the elongation of the relaxation time is attributed to the incomplete cooling of the active volume and the incomplete MIT prior to the arrival of the subsequent pulses.

Finally, we gain a better insight into the time scale of the set transitions during oscillator operation by testing the oscillator circuits with our 100 GHz bandwidth measurement setup, which we also used for the ultra-short switching time experiments (see the experimental details in the Experimental Section and in Ref. [31].) The such-measured oscillating signal in



**Figure 6.** Ultrafast oscillations measured by our 100 GHz bandwidth setup. The measurements are performed by the experimental setup used in Ref. [31] and an  $R_s = 16 \text{ k}\Omega$  resistor.

**Figure 6** yields similar 103 MHz oscillation frequency, respectively exhibiting a 10–90% rise-time of 1.2 ns and fall-time of 3.4 ns for the set and reset transition. This confirms that the reset transition is the dominating limiting factor. On the other hand, the observed 1.2 ns rise time is significantly longer than the 15 ps set time measured in our previous work.<sup>[31]</sup> This 100 GHz bandwidth measurement clearly demonstrates that the 1.2 ns rise time is not an instrumental bandwidth limitation, but the set time is really elongated. This is attributed to the fact that in an oscillator the voltage is limited by the set voltage, while the 15 ps set time was observed at pulsed driving with significantly higher pulse amplitudes. We also note, that the 1.2 ns rise time is shorter than the several nanosecond long set times observed in Figure 5b–d for pulses adjusted close to the set transition. This apparent difference is attributed to the fact that for single pulses the switching starts from a room temperature, fully developed HRS. However, during oscillator operation the active region heats up slightly, the reset transition is incomplete, and thus a faster set transition is achieved than for single pulse driving.

The above illustrative experiments on the switching dynamics of  $\text{VO}_2$ , as well as previous sub-threshold firing experiments and further  $\text{VO}_2$  dynamics studies<sup>[35,36]</sup> show that  $\text{VO}_2$  devices cannot be treated as simple hysteresis switches with well-defined switching voltages and switching times. On the contrary, the switching parameters depend sensitively on the drive parameters and the history of the device, with switching time variations of up to an order of magnitude. A comprehensive analysis of the full relaxation dynamics and the device-to-device variation of the transition times is clearly beyond the scope of this paper. Nevertheless, our above switching-time experiments and our similar experiments on other devices already point to the following conclusions: (i) Under the conditions of an oscillator circuit, i.e., for repetitive voltage oscillations not significantly exceeding the set voltage and not going below the reset voltage, the set and reset times are expected to be order(s) of magnitude larger than the minimum set time of 15 ps and relaxation time of 600 ps. (ii) The reset transition is always significantly longer than the set transition, i.e., the relaxation time is the key restricting factor for the oscillation frequency. (iii) The observed relaxation times make it clear that an oscillation significantly faster than the fastest 167 MHz oscillation achieved is not realistic. Our experience with these ultrafast oscillator circuits shows that oscillations up to  $\approx 100$  MHz regime are routinely established, while even larger frequencies, like the 167 MHz oscillation in Figure 1d, specifically rely on the fine interplay of the device parameters.

Based on the analysis of >50 independent devices, we found that the low-frequency switching characteristics ( $V_{\text{set}}$ ,  $V_{\text{reset}}$ ,  $R_{\text{M, HRS}}$ , and  $R_{\text{M, LRS}}$ ) show significant device-to-device variations. These differences are summarized in Figure S6 (Supporting Information) and are attributed to the small active volume, where the effects of material imperfections or grain boundaries are magnified compared to larger devices. These differences also affect high-frequency characteristics: in our experience, selected devices with a set voltage of  $V_{\text{set}} < 2.5 \text{ V}$  (approximately 35% of all devices) are advantageous for ultra-high-frequency operation. Of this subgroup of devices,  $\approx 50\%$  and  $\approx 20\%$  exhibit >50 MHz and >100 MHz oscillation frequencies, respectively.

In terms of cycle-to-cycle stability, we can say that our devices remain operational for  $>2 \cdot 10^{13}$  cycles (i.e., several days, see Figure S7, Supporting Information). However, some frequency drift can be observed during operation, as illustrated in Figure S8 (Supporting Information), which shows a frequency variation of less than 3% over  $\approx 10^7$  oscillation cycles, and Figure S7 (Supporting Information), which shows a frequency change of 13% between the start and end of a total of  $>2 \cdot 10^{13}$  cycles.

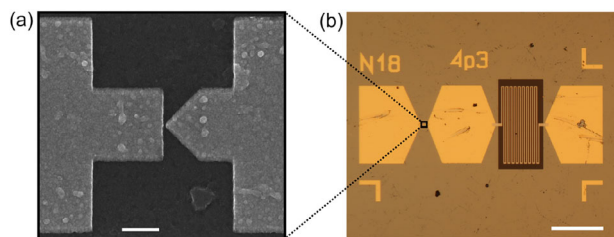
The temperature dependence of the oscillations was also investigated (see Figure S5, Supporting Information), which showed that a slightly increasing trend of the oscillation frequencies is observed by the elevation of the temperature, but this is accompanied by a rapid degradation of the oscillation stability.

These results indicate that ONNs built from our ultrafast oscillator circuits may achieve orders of magnitude faster time-to-solution with significantly reduced energy consumption. In addition, due to the small size of the active area, thermal crosstalk<sup>[27]</sup> from neighboring devices is also reduced to a range of  $1 \mu\text{m}$  (see the simulations of Figure S9, Supporting Information). At the same time, the device-to-device variability described above poses a significant challenge in synchronizing multiple oscillators, so device-to-device variability must be reduced through further material and manufacturing optimization.

### 3. Conclusion

In conclusion, we have demonstrated  $\text{VO}_2$  oscillator circuits optimized for high-frequency, 100 MHz-range operation. To this end, we have applied an optimized sample layout, where the stray capacitance is minimized, and the switching is focused to an ultra-small,  $\approx 30 \text{ nm}$  wide active region. Furthermore, the circuit layout is also optimized for high-frequency operation by applying a transmission line geometry, where the oscillation frequency is tunable both by the  $d$  memristor-to-resistor distance and the  $C$  parallel capacitance. According to circuit simulations of the same transmission-line geometry, reasonably achievable, pF-range parallel capacitances and a few mm memristor-to-resistor distances readily yield 100 MHz-range oscillation frequencies, similarly to our experimentally demonstrated oscillations up to 167 MHz frequency.

Circuit simulations would allow even higher > GHz oscillation frequencies with even shorter  $d$  and lower  $C$ . At the same time the fastest pulsed switching experiments demonstrate subnanosecond relaxation times,<sup>[31]</sup> which could also be compatible with GHz oscillator operation. However, we have demonstrated that the speed limitation is fundamentally different for an oscillator circuit than for optimized resistive switching experiments with



**Figure 7.** Images of the on-chip integrated VO<sub>2</sub> memristor-meander resistor samples. a) SEM image showing the planar memristor design, the arrangement of a flat and a V-shaped Au electrode pair encompassing a 30 nm VO<sub>2</sub> active region in between. Scale bar: 500 nm. b) Optical microscope image of a memristor-resistor sample, showing the layout for a thin film Pt meander resistor with  $N = 18$  turns. Scale bar: 100  $\mu\text{m}$ .

single pulses. Most importantly, the finite  $\gtrsim V_{\text{reset}}$  voltage level on the memristive element and the rapidly repeated switching events lead to a slowdown of the relaxation time, which explains the 100 MHz-range frequency limit achieved. Together with these constraints, the above results have enabled oscillation frequencies more than an order of magnitude higher than the fastest VO<sub>2</sub> oscillators presented so far,<sup>[26]</sup> paving the way toward the realization of ultra-fast and energy-efficient VO<sub>2</sub>-based oscillating neural networks.

## 4. Experimental Section

**Sample Fabrication and Characterization:** The VO<sub>2</sub> layers used for creating the memristors were formed on Al<sub>2</sub>O<sub>3</sub> substrates by pulsed laser deposition method according to Refs. [37,38]. The VO<sub>2</sub> films were optimized for pure stoichiometric VO<sub>2</sub> by adjusting oxygen background pressures during deposition.<sup>[39]</sup> X-ray diffraction (XRD) and scanning transmission electron microscopy – electron energy loss spectroscopy (STEM EELS) methods were used to confirm the phase and stoichiometry of the VO<sub>2</sub> films, as described in Refs. [37–40].

The vertical layer structure of the VO<sub>2</sub> devices is shown in Figure 1e including the Al<sub>2</sub>O<sub>3</sub> substrate, the 50 nm thick epitaxial VO<sub>2</sub> layer, a 5 nm Ti adhesive layer and the 60 nm thick gold top electrodes. The electrodes were patterned by standard electron beam lithography and deposited by electron-beam evaporation at 10<sup>-7</sup> mbar base pressure at rates of 0.1 nm/s (Ti) and 0.4 nm/s (Au), followed by lift-off. Figure 7a shows the surrounding region of a typical VO<sub>2</sub> nanogap memristor formed by this method.

Small,  $\approx 1.5$  mm memristor-to-resistor distances were achieved by samples, where a meander-shaped series resistor was integrated on the memristor chip (see the optical microscope image in Figure 7.b and the illustrative inset in Figure 2a). The line width of the meanders was 2  $\mu\text{m}$  with 2  $\mu\text{m}$  spacing, 150  $\mu\text{m}$  length (for a single line) and  $N = 5, 9, 13, 18$  turns. The beginning of the meanders were located at 150  $\mu\text{m}$  distance from the memristors. For the calculation of an effective memristor-resistor distance, the total length of the meander lines has to be considered, which can be estimated as  $150 \mu\text{m} \cdot 18/2 + 150 \mu\text{m} = 1.5$  mm for the longest meander with  $N = 18$  turns (shown in Figure 7.b).

The VO<sub>2</sub> layer beneath the meanders was etched away in a reactive ion etching process. The etching mask was created in a standard electron beam lithography process, leaving rectangular areas free for etching at locations where the meanders will be formed (see Figure 7b, rectangular area around the meander). This etching step prior to the deposition of meander resistors was implemented to exclude the possibility of conduction through the VO<sub>2</sub> layer between Pt lines.

The etching process was performed by a Diener low-pressure plasma system. First, the vacuum chamber was pumped to reach 0.16 mbar base

pressure, then pure CH<sub>4</sub> gas was supplied with 42 sccm flow rate to set the 0.64 mbar process pressure. The plasma power was set to 240 W and the duration of the etching to 30 s. Afterwards, the meander resistors were patterned by electron beam lithography, and 15 nm Pt was deposited by electron beam evaporation using 0.3 nm/s rate, followed by lift-off.

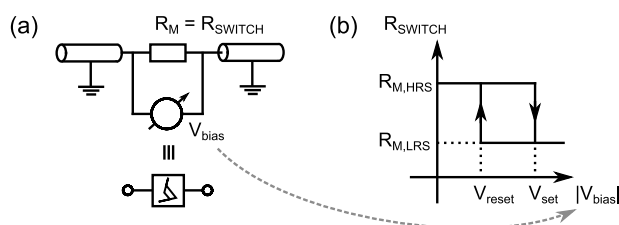
**Measurement Scheme:** The oscillating traces of the VO<sub>2</sub> circuits were investigated with a Rohde & Schwarz RTO1024 oscilloscope with 1 GHz bandwidth and 10 GS/s sampling, or by a Picoscope 6404A oscilloscope with 0.5 GHz bandwidth and 5 GS/s sampling (Figures 4e and Figure 5h,i,j). In the latter case small reflections were observed at the 50  $\Omega$  input of the oscilloscope, which cause minor echo peaks after the main peaks in the oscillating signals. The drive voltage was supplied by an Agilent 33210A arbitrary waveform generator. In order to avoid sample degradation due to too many oscillation periods, the constant drive voltage was applied to the oscillator circuit for a finite time, typically achieving  $\approx 50$  periods of oscillations per measurement.

Most of the measurements were performed on 3.0 cm  $\times$  2.4 cm printed circuit boards with SMA connectors on both sides, and 50  $\Omega$  wave impedance transmission lines connecting the SMA connector to the surface mounted series resistor, the resistor to the bonding wires of the sample, and the sample to the other SMA connector.

For the pulsed measurements in Figure 5 either a Zurich Instruments HDAWG or an AT1120 AWG module mounted on a National Instruments PXIe-7976 board together with a Mini-Circuit ZHL-72A+ amplifier were applied.

The  $\approx 100$  GHz bandwidth measurements in Figure 6 were performed with the same setup as the measurements in Ref. [31]. The principle of these measurements also followed the principle depicted in Figure 2c lacking the parallel capacitive element C, the difference lies solely in the much greater bandwidth of the driving, probing and measuring units. The samples were contacted by two 67 GHz bandwidth Picoprobe triple probes in a probe station. A Micram DAC10004 100 GSa/s DAC unit together with a Centellax UA0L65VM broadband amplifier served as the driving unit. The transmitted voltage was recorded by a Keysight UXR1104A digital storage oscilloscope at 256 GSa/s sampling rate and 113 GHz analog bandwidth. The input terminals of the oscilloscope were protected by RF attenuators.

**Simulation:** The oscillating circuits were simulated by LTspice and Matlab Simulink. In order to place our memristor in a circuit with a waveguide geometry (Figure 8a), it was important that it acted as a variable resistor, instead of low-frequency simulations of VO<sub>2</sub> devices,<sup>[41]</sup> where the memristor model contained a current generator element in the circuit. In Figures 2, 3 as well as in the comparative analysis of Figure 4c,d (dotted lines) we have used a minimal model, where the memristor is simply a hysteretic resistance switch in LTspice, and no internal relaxation time is considered (see Figure 8b.) These simulations can track the key consequences of the finite memristor-to-resistor distance or the finite parallel capacitance. More refined Matlab Simulink simulations are presented in



**Figure 8.** LTspice simulations of the VO<sub>2</sub> oscillator circuits. In most of our investigation the VO<sub>2</sub> memristor is placed in a waveguide geometry circuit, like Figure 2c. These arrangements are simulated by (i) measuring the  $V_{\text{bias}}$  voltage drop on the memristor, which acts as a variable resistor,  $R_M$  (panel (a)); and (ii) updating the memristor resistance according to the variation of  $V_{\text{bias}}$  and the hysteretic resistance switch model in panel (b). The memristor in the HRS (LRS) executes a set (reset) transition once the voltage goes above (goes below)  $V_{\text{set}}$  ( $V_{\text{reset}}$ ).

Sections S3–S5 (Supporting Information), where finite and different physical relaxation times are used for the set and reset transitions.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

This research was supported by the Ministry of Culture and Innovation and the National Research, Development and Innovation Office within the Quantum Information National Laboratory of Hungary (Grant No. 2022-2.1.1-NL-2022-00004), and the NKFI K143169, K143282 and TKP2021-NVA-03 grants. L.P. and T.N.T. acknowledge the support of the János Bolyai Research Scholarship of the Hungarian Academy of Sciences. L.P. and Z.P. acknowledge the support of the Ministry of Culture and Innovation and the National Research, Development and Innovation Office within the University Research Scholarship Programme. J.L. and M.C. acknowledge the financial support of the Werner Siemens Stiftung.

## Conflict of Interest

The authors declare no conflict of interest.

## Author Contributions

Z.P. and T.N.T. contributed equally to this work. The LTspice simulation and experiment involving VO<sub>2</sub>-based memristors and oscillator circuits were developed and performed by Z.P. under the daily guidance of T.N.T. The Matlab Simulink simulations were developed by T.N.T. The experiment carried out with the 100 GHz bandwidth setup was performed by S.W.S. and M.C. in the group of J.L. Technical support for the measurements was provided by Z.B. (low frequency characterization, printed circuit board development and the high frequency probe station development) and by A.B. (fast pulsed measurements). The VO<sub>2</sub> memristors were developed and fabricated by T.N.T. and L.P., and the integrated meander resistor-memristor samples were designed by T.N.T. in the group of J.V. The VO<sub>2</sub> thin layers were manufactured and optimized by H.K. and A.P. The project was conceived and supervised by A.H. The manuscript was written by Z.P., T.N.T. and A.H. All authors contributed to the discussion of the results and the preparation of the manuscript.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

oscillator, resistive switching, memristor, vanadium oxide

Received: July 5, 2025

Revised: October 6, 2025

Published online: October 24, 2025

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