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Angaben zur Veröffentlichung / Publication details:

Tanaka, Yuya, Yutaka Noguchi, Michael Kraus, Wolfgang Brütting, and Hisao Ishii. 2013. "Three-terminal capacitance-voltage measurements of pentacene field-effect transistors during operation." *Organic Electronics* 14 (10): 2491–96. https://doi.org/10.1016/j.orgel.2013.06.013.

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Organic Electronics, 14 (2013) 2491-2496
https://doi.org/10.1016/j.orgel.2013.06.013

Three-Terminal Capacitance–Voltage Measurements of a Pentacene Field-Effect Transistor during Operation

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Abstract

We propose a modified measurement technique of capacitance for three-terminal devices and apply this method for the evaluation of the channel formation in pentacene field-effect transistors. An additional structure in the capacitance–voltage curves clearly shows the channel formation from the saturation to the linear region in an operating transistor which has not been directly observed in conventional methods. Based on the amount of accumulated charge in the channel region, the validity of the gradual channel approximation model and the usability of a buffer layer are discussed. This method enables the detailed investigation of carrier behaviors in organic transistors through appropriate evaluation of the channel formation process during operation.

Keywords: Displacement current measurement, Impedance spectroscopy,

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https://doi.org/10.1016/j.orgel.2013.06.013

Pentacene, Organic field-effect transistor, Channel formation, Organic electronics

1. Introduction

Organic field-effect transistors (OFETs) are promising devices because of their favorable features such as flexibility and low cost fabrication [1, 2]. Much effort has been devoted to increase in performance through insertion of buffer layer at organic/gate dielectric interface and optimization of electrodes and insulator layer [3]. In addition, the bias-induced instability has attracted attention as the issue to be overcome [4]. To advance these efforts toward practical use, it is important to understand the carrier behaviors in OFETs. Generally, the carrier behaviors in OFETs are described as follows: (i) carriers are injected from the source electrode by applied gate voltage (V_{GS}) and accumulated immediately under the source electrode; (ii) the accumulated carriers spread laterally and forms the conduction channel along the organic/gate dielectric interface; (iii) the charge carrier travels from the source to the drain electrode due to the applied drain voltage (V_{DS}). Because all of these processes induce the variation of the carrier distribution in the device, monitoring the capacitance is a good measure to evaluate the carrier dynamics in the device.

Capacitance–voltage (C–V) relationships obtained by capacitance measurements, such as impedance spectroscopy (IS) and displacement current measurement (DCM), have been measured in organic metal-insulator-semiconductor (MIS) diodes and OFETs [5, 6, 7, 8, 9]. The MIS structure is a model device for transistor and suitable to evaluate the injection and accumulation prop-

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erties corresponding to (i) in the previous paragraph. However, the channel formation process is unavailable to be evaluated in MIS structure. Even in FET structures, conventional C–V techniques have been performed with connecting the source and drain electrodes to the ground during C–V measurements [6, 7, 8]. Because of lacking V_{DS}, it is impossible to examine the V_{DS} dependence of the behaviors of accumulated charges. This difficulty is attributed to the fact that C–V techniques are two-terminal measurement methods while OFETs have three electrodes. Thus the C–V methods with application of V_{DS} are required to elucidate the channel formation process during transistor operation.

In a recent study, Majima *et al.* successfully obtained C–V relationship by DCM during transistor operation by using simultaneous measurements of the source and drain currents [10, 11, 12]. Basically, in DCM, the triangular wave voltage is applied to the gate electrode and current response is measured. In the case of DCM proposed by Majima *et al.*, a high frequency of the triangular gate voltage is necessary due to the limitation of dynamic range. This is because the intensity of the displacement current, which is proportional to the frequency of the triangular voltage, should be comparable to the drain-to-source current; this restricts the range of the available measurement frequencies. In order to understand the channel formation process in detail, the limitation of frequency should be removed. Furthermore, their approach is specific to DCM and cannot be applied to IS, which is a more common method as capacitance measurement.

In this study, we proposed a three-terminal C–V method where an isolated battery source is used to apply V_{DS}. This method allows us to directly

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and easily obtain the C–V relationships with high signal-to-noise ratio during transistor operation at any frequencies. In a pentacene (Pn)-based OFET with a tetratetracontane (TTC; $C_{44}H_{90}$) surface treatment on the SiO_2 substrate, Pn/TTC-FET, an additional structure in the C–V curves that reflects the variation of the capacitance from the saturation to linear region was clearly observed which has not appeared in conventional C–V measurements. From the analysis of the results of three-terminal C–V measurement, the validity of the gradual channel approximation (GCA) model and effect of buffer layer are discussed. Because these evaluations cannot be conducted in conventional C–V setups, the three-terminal C–V method allows for the detailed investigation of the operating mechanism and performance assessment of OFETs.

2. Experimental

In C–V measurements, the scanning bias, for example, a combined AC and DC voltages in IS and triangular wave voltages in DCM, are applied to the gate electrode in order to evaluate the carrier accumulation process in organic/dielectric interface. We expand the function of these conventional C–V measurements by inserting the drain voltage source into its measurement circuit. Figure 1(a) shows the proposed measurement setup for capacitance which includes an isolated battery source to apply V_{DS}, named as three-terminal C–V method. As the battery circuit is electrically isolated from the gate electrode, AC current in IS and displacement current in DCM can be measured precisely during transistor operation.

In three-terminal C–V method, V_{GS} is changed under a constant V_{DS}.

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Therefore, the observed C–V characteristics corresponds to the variation of the capacitance in I_{DS}–V_{GS} (transfer) curve. By changing the V_{DS}, the charge injection and channel formation processes are investigated in more detail by comparing with transfer curve.

Figure 1(a) shows the FET structure with top contact geometry. A heavily doped p^+-type Si wafer (resistivity $< 0.02\ \Omega \cdot \mathrm{cm}$) was used as the FET substrate (gate electrode). The thickness of the oxide layer was 300 nm. A 30-nm-thick TTC layer [Fig. 1(b)] was deposited on the SiO_2/p^+-Si substrate as the insulating layer and annealed at 350 K for 10 min in a glove box filled with pure nitrogen. Figure 1(c) shows the AFM image of the TTC (30 nm) on the SiO_2/p^+-Si substrate (top) and the cross-section view of the TTC surface along the solid line in the AFM image (bottom). The step height (≈ 5.9 nm) nearly corresponds to the molecular length of TTC, suggesting that the TTC molecules stand up with full coverage of the SiO_2 substrate. On this smooth TTC surface, a 100-nm-thick pentacene (Pn) layer [Fig. 1(b)] was evaporated, and finally, gold was deposited as the source and drain electrodes. The device was transferred to the glove box for electrical measurements without exposure to air. The channel length (L) and width (W) were 120 μm and 3 mm, respectively. The areas of the source and drain electrodes were both 9 mm^2. The area of the Pn layer was the same as the total area of the electrodes plus channel region.

The three-terminal C–V method was applied to two types of OFETs, Pn/TTC-FET which has TTC buffer layer on SiO_2 and Pn-FET without TTC layer. The amplitude of the AC bias was set to be 0.1 V and the DC bias was varied from 10 V to -40 V at a frequency of 2 Hz for Pn/TTC-

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FET and 5 Hz for Pn-FET. V_{DS} was changed from 0 V to −46.1 V by ca. 9 V steps. Capacitance–frequency (C–f) curves were also obtained by the proposed method at various f ranging from 1 Hz to 10^5 Hz (not shown). In this study, we focus on the variation of capacitance in static state by setting the frequencies of 2 Hz or 5 Hz.

3. Results and discussion

3.1. Three-terminal C–V measurement of operating OFET

Figure 2(a) shows the C–V curves in the operating Pn/TTC-FET and Fig. 2(b) presents the I_{DS}–V_{GS} (transfer) curves. The circles in Figs. 2(a) and 2(b) indicate the results for $V_{DS} = 0$. That is, the C–V measurement was performed using the conventional setup: V_{GS} was applied to the gate electrode and both the source and drain electrodes were connected to the ground. In Fig. 2(a), the device was completely depleted near $V_{GS} = 10$ V because the capacitance was constant at the smallest value (C_{dep}). With a decrease in V_{GS}, the capacitance began to increase due to hole injection from the source and drain electrodes to the Pn layer. Finally, because the injected holes accumulated at the whole Pn/TTC interface, the measured capacitance remained constant in the negative V_{GS} region at the largest value (C_{acc}). During the scanning of V_{GS}, I_{DS} did not flow as shown in Fig. 2(b).

The inverted triangles in Fig. 2(a) indicate the results for $V_{DS} = -28.0$ V by using the three-terminal C–V setup in Fig. 1(a). The spectrum is divided into three parts: region (I), (II) and (III). In region (I), the capacitance nearly corresponds to C_{dep} from $V_{GS} = 1$–3 V, indicating the device in the depletion region. In this region, I_{DS} does not flow because there are no free carriers in

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the device [Fig. 2(b)]. The variations of capacitance and I_{DS} at the voltages higher than 3 V are originated from electron injection as discussed later. With scanning V_{GS} to the negative voltage side, the capacitance increases and reaches C_{inj} [Fig. 2(a)], which is the estimated capacitance when the holes accumulate immediately under the source electrode [Fig. 2(d)]. In this region, the holes are injected only from the source electrode because of V_{DS}. Upon further scanning of V_{GS} to the negative side, results show gradual increase in the capacitance in region (II) [Fig. 2(a)] and I_{DS} starts to flow at the beginning of this region, suggesting the formation of a conduction channel. The capacitance is roughly saturated at C_{chn}, which is the calculated capacitance when the injected holes accumulate under the source electrode and channel region [Fig. 2(e)]. These results clearly indicate that the pinch-off occurs in this region; i.e. I_{DS} in region (II) [Fig. 2(b)] belongs to the saturation region. Thus, the variation of the capacitance from C_{inj} to C_{chn} can be explained as the move of the pinch-off point from the edge of the source electrode to that of the drain electrode. With a further decrease in V_{GS}, the capacitance begins to increase again in region (III), suggesting hole accumulation under the drain electrode. Finally, the capacitance becomes constant at C_{acc}. This situation corresponds to the linear region because a charge sheet is completely formed at the whole Pn/TTC interface. In this way, our proposed technique reveals the processes in Pn/TTC-FET while the injected carrier forms the conduction channel which has not been directly observed in conventional setup.

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3.2. Charge accumulation process in channel region

As described in previous section, the variation of capacitance observed by three-terminal C–V method reflects the channel formation process during the transistor operation. Here, we would like to focus on the analysis of the amount of the charge (Q) in channel region. Figure 3(a) shows the $V_{\rm DS}$ dependence of C–V curves at various $V_{\rm DS}$ (ranging from 0 V to −37.6 V). Figure 3(b) indicates the transfer curves for corresponding $V_{\rm DS}$. This result implies that charge accumulation process strongly depends on the applied $V_{\rm DS}$.

When $V_{\rm DS}$ was set to be −9.6 V, only a weak shoulder structure is observed at $V_{\rm GS} = 0$ during the transition of capacitance from $C_{\rm inj}$ to $C_{\rm chn}$. This is because the holes rapidly accumulate under the drain electrode. With decreasing $V_{\rm DS}$, the region of the gradual increase from $C_{\rm inj}$ to $C_{\rm chn}$ becomes wider and $V_{\rm GS}$ at which the capacitance reaches $C_{\rm acc}$ shifts to the negative $V_{\rm GS}$ side since the negative $V_{\rm DS}$ prevents from the hole injection from the drain electrode. These results imply that pinch-off voltage ($V_{\rm PO}$) is changed by the applied $V_{\rm DS}$ and $V_{\rm GS}$.

The amount of injected holes (Q) is easily calculated from the C–V curves by integrating the capacitance with respect to $V_{\rm GS}$ and is one of the best indicators of $V_{\rm PO}$ because the distribution of Q determines whether the FET operates in the linear or saturation regions. Q is given by

$$Q = -\int_{V_{\rm GS}^{\rm A}}^{V_{\rm GS}} (C - C_{\rm inj}) dV, \tag{1}$$

where $V_{\rm GS}^{\rm A}$ is the voltage when capacitance reaches the $C_{\rm inj}$, that is, the injected holes accumulate under the source electrode [see Fig. 2(d)]. $V_{\rm GS}^{\rm A}$

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was set to be −4 V for Pn/TTC-FET and −1.5 V for Pn-FET. In order to focus on the hole accumulation property in channel region, an integrated capacitance was estimated by subtracting C_{inj} from observed capacitance.

Figure 4(a) shows the plots of Q as a function of V_{GS} estimated by Eq. (1). In the case of $V_{\mathrm{DS}} = 0$ V, Q linearly increases and the slope (≈ 2.97 nC/V) corresponds to $C_{\mathrm{acc}} - C_{\mathrm{inj}} = 2.96$ nF, simply indicating the charging of the capacitor. In addition to this charging process, an another slope (≈ 0.046 nC/V) appears with decreasing V_{DS}. Because this slope nearly agrees with $C_{\mathrm{chn}} - C_{\mathrm{inj}} = 0.036$ nF, this result indicates that the amount of injected charge to the channel region is estimated from the C–V curves without assumptions. With a further decrease in V_{GS} to the negative side, the slope of the Q–V_{GS} curves increases and corresponds with that where $V_{\mathrm{DS}} = 0$ V. This change occurs because the holes accumulate under the drain electrode and the whole insulator layer works as a capacitor. Therefore, by analyzing the variation of Q for fixed V_{DS}, the channel formation can be discussed in detail. For example, when $V_{\mathrm{GS}} = -20$ V, Q decreases with V_{DS} and finally saturates at $V_{\mathrm{DS}} < -18.5$ V. This variation of Q as a function of V_{DS} implies a change in the operating regime from linear to saturation.

In order to understand the details of the hole accumulation process during transistor operation, Q was replotted as a function of V_{DS} in Fig. 4(b). The value of Q was calculated when V_{GS} was set to −10 V (circles), −20 V (squares), −30 V (triangles) and −40 V (inverted triangles), and normalised by Q at $V_{\mathrm{DS}} = 0$ V (Q_0) in order to facilitate visualization. The solid lines indicate the I_{DS}–V_{DS} (output) curves for the corresponding V_{GS}. When $V_{\mathrm{GS}} = -20$ V, Q decreases linearly for $V_{\mathrm{DS}} > -20$ V, suggesting the discharge

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of holes to the drain electrode due to the decrease in $V_{\rm DS}$. This behavior of the accumulated holes corresponds well with that in the linear region. For $V_{\rm DS} < -20$ V, Q becomes constant. Here this constant value in Fig. 4(b) is referred to as $Q_{\rm sat}$ (dashed line). This result suggests that the pinch-off occurs in this region and the amount of the accumulated charge in the channel region is saturated. From the intersection (marked by the vertical bar) of the linear approximation functions in the linear and saturation regimes, $V_{\rm PO}$ was directly estimated for various $V_{\rm GS}$. The crosses on the output curves in Fig. 4(b) indicate the drain current at $V_{\rm DS} = V_{\rm PO}$ ($I_{\rm DS}^{\rm PO}$) when $V_{\rm GS}$ was set to be -10 V, -20 V and -30 V. According to GCA model, the $V_{\rm PO}$ and $I_{\rm DS}^{\rm PO}$ can be expressed by

$$V_{\rm PO} = V_{\rm GS} - V_{\rm T}, \tag{2}$$

$$I_{\rm DS}^{\rm PO} = \frac{WC_{\rm ins}\mu}{2L}(V_{\rm GS} - V_{\rm T})^2, \tag{3}$$

where $V_{\rm T}$, $C_{\rm ins}$ and μ show the threshold voltage, insulator capacitance per unit area and field-effect mobility, respectively [13, 14, 15]. Figure 4(b) clearly indicates that, with decreasing $V_{\rm GS}$, $V_{\rm PO}$ linearly shifts to the negative $V_{\rm DS}$ side and $I_{\rm DS}^{\rm PO}$ nearly increases quadratically. These results strongly suggest that the GCA model constructed for inorganic FETs can be properly applied to analyze the operation mechanism of the Pn/TTC-FET.

3.3. Impact of insertion of TTC buffer layer on SiO_2

For discussing the effect of the surface treatment of SiO_2 by TTC, Pn-FET without TTC layer is also evaluated by three-terminal IS. Figures 5(a) and 5(b) show the three-terminal C–V and transfer curves at various $V_{\rm DS}$, respectively. Compared with the three-terminal C–V curves of Pn/TTC-FET,

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the variation in the capacitance during the hole accumulation process under the source electrode is stretched out. An increase in the sub-threshold swing (SS) due to the decrease in the charge inside the device is expected. In actual, the SS increases from 0.75 V/decade in Pn/TTC-FET to 2.5 V/decade in Pn-FET, suggesting a high contact resistance in Pn-FET or an increase in the trap states in the channel region supported by capacitance-frequency measurement (not shown). While the capacitance is changed from C_{inj} to C_{chn}, only a shoulder structure is observed in Fig. 5(a) even if V_{DS} decreases, implying that the saturation condition is not entirely fulfilled. In the Q–V_{GS} curve in Fig. 5(c) estimated from Fig. 5(a) by using Eq. (1), when V_{DS} is changed from 0 V to −37.6 V, the saturation of Q at a certain V_{GS} is not clearly observed. The value of Q as a function of V_{DS} and the output curves are plotted in Fig. 5(d) and show that Q at $V_{\mathrm{GS}} = -20$ V, −30 V and −40 V does not become constant. This result clearly suggests that complete saturation did not occur in the Pn-FET. Therefore, analysis based on the GCA model should be carefully applied to OFETs.

In addition to the effect of the TTC on the hole accumulation characteristics, another impact on the FET properties is also apparent. As can be seen in Fig. 3(a), when $V_{\mathrm{DS}} = -9.6$ V, the capacitance for positive values of V_{GS} (> 5 V) agrees well with that for $V_{\mathrm{DS}} = 0$ V, indicating the depletion condition as shown in Fig. 2(c). At values higher than or equal to $V_{\mathrm{DS}} = -18.5$ V, the capacitance and I_{DS} for the positive V_{GS} region increase. On the other hand, any increases in the capacitance and I_{DS} in the positive V_{GS} region are not observed in Figs. 5(a) and 5(b). These results suggest that the TTC layer passivates the electron traps on the SiO_2 surface and

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enhances the electron injection and n-channel formation, as shown in the inset [Fig. 3(a)] [16, 17, 18]. Because the simultaneous accumulation of hole and electron is not achieved without V_{DS}, our method is expected to be a powerful technique to investigate the carrier behaviors in ambipolar FETs and light-emitting transistors.

4. Conclusion

We proposed three-terminal C–V measurements of a pentacene-based FETs during transistor operation by using a battery circuit for V_{DS}. In addition to the hole injection and accumulation properties, a gradual increase in the capacitance was observed in Pn/TTC-FET, suggesting the pinch-off condition of the transistor. Amount of injected charges in the channel region from C–V curves was estimated and the validity of GCA model was discussed. The battery-circuit is also useful to expand DCM for the three-terminal method, which can be used to evaluate the channel formation and annihilation processes separately during transistor operation [19]. The proposed method can be used as a tool for clarifying the operating mechanism of OFETs, including ambipolar and light-emitting transistors.

ACKNOWLEDGMENTS

We thank Prof. Masakazu Nakamura and Dr. Satoshi Ogawa for his helpful suggestions. This work was supported by the Global-COE program at Chiba University (Advanced School for Organic Electronics, G-03, MEXT), KAKENHI (Grants No. 21245042, 22750167), and the Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST).

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YT gratefully acknowledges JSPS Research Fellowships for Young Scientists (Grants No. 22·7042).

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https://doi.org/10.1016/j.orgel.2013.06.013

Figure captions:

Figure 1: (a) Schematic illustration of the device structure and experimental setup. I_{AC} between the isolated battery circuit and gate electrode is measured under a bias of V_{GS} and the V_{DS} is supplied by the battery circuit. This setup enables impedance spectroscopy and displacement current measurement for three-terminal devices such as an operating transistor. (b) Chemical structures of pentacene (Pn) and $C_{44}H_{90}$; tetratetracontane (TTC). (c) AFM image of the TTC (30 nm) on the SiO_2/p^+-Si substrate. The bottom figure shows the cross-section view of the TTC surface along the solid line in the AFM image.

Figure 2: (a) Three-terminal IS curves of Pn/TTC-FET in $V_{\mathrm{DS}} = 0$ V (circles) and $V_{\mathrm{DS}} = -28.0$ V (inverted triangles). (b) $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curves in $V_{\mathrm{DS}} = 0$ V (circles) and $V_{\mathrm{DS}} = -28.0$ V (inverted triangles). (c-f) Schematic view of the carrier distribution during the measurement in (c) depletion, (d) hole accumulation immediately under the source electrode, (e) hole accumulation under the source electrode and channel region and (f) hole accumulation over the pentacene/insulator interface. C_{dep}, C_{inj}, C_{chn} and C_{acc} show the capacitance value in various carrier accumulation conditions as shown in (c), (d), (e) and (f), respectively.

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Figure 3: (a) Three-terminal IS curves of Pn/TTC-FET in $V_{\rm DS}$ = 0 V (circles), −9.6 V (triangles), −18.5 V (squares), −28.0 V (inverted triangles) and −37.6 V (diamonds). (b) $I_{\rm DS} - V_{\rm GS}$ curves for corresponding $V_{\rm DS}$. Insets show the carrier distribution in hole injection from source electrode in negative $V_{\rm GS}$ and electron injection from the drain electrode in positive $V_{\rm GS}$.

Figure 4: (a) The amount of injected holes as a function of $V_{\rm GS}$. (b) Plots of the amount of injected holes normalized by that in $V_{\rm DS}$ = 0 V and $I_{\rm DS}$ as a function of $V_{\rm DS}$. $V_{\rm GS}$ was set to be −10 V (filled circles), −20 V (filled triangles), −30 V (filled squares) and −40 V (filled inverted triangles). Solid lines show the $I_{\rm DS}$. Filled triangles indicate the pinch-off voltages for corresponding $V_{\rm GS}$. Dashed line shows the amount of injected charge normalized by that in $V_{\rm DS}$ = 0 in channel region. Vertical bars and crosses indicate the intersection of linear approximation functions in linear and saturation regimes and the drain current at $V_{\rm DS} = V_{\rm PO}$, respectively.

Figure 5: (a) Three-terminal IS curves of Pn-FET without TTC layer in $V_{\rm DS}$ = 0 V (circles), −9.6 V (triangles), −18.5 V (squares), −28.0 V (inverted triangles) and −37.6 V (diamonds). (b) $I_{\rm DS} - V_{\rm GS}$ curves for corresponding $V_{\rm DS}$. (c) Amount of injected holes in Pn-FET without TTC layer as a function of $V_{\rm GS}$. (d) Plots of amount of injected holes of Pn-FET without TTC layer normalized by that in $V_{\rm DS}$ = 0 V and $I_{\rm DS}$ as a function of $V_{\rm DS}$. $V_{\rm GS}$ was set to be −10 V (filled circles), −20 V (filled triangles), −30 V (filled squares) and −40 V (filled inverted triangles). Solid lines show the $I_{\rm DS}$.

Figure1

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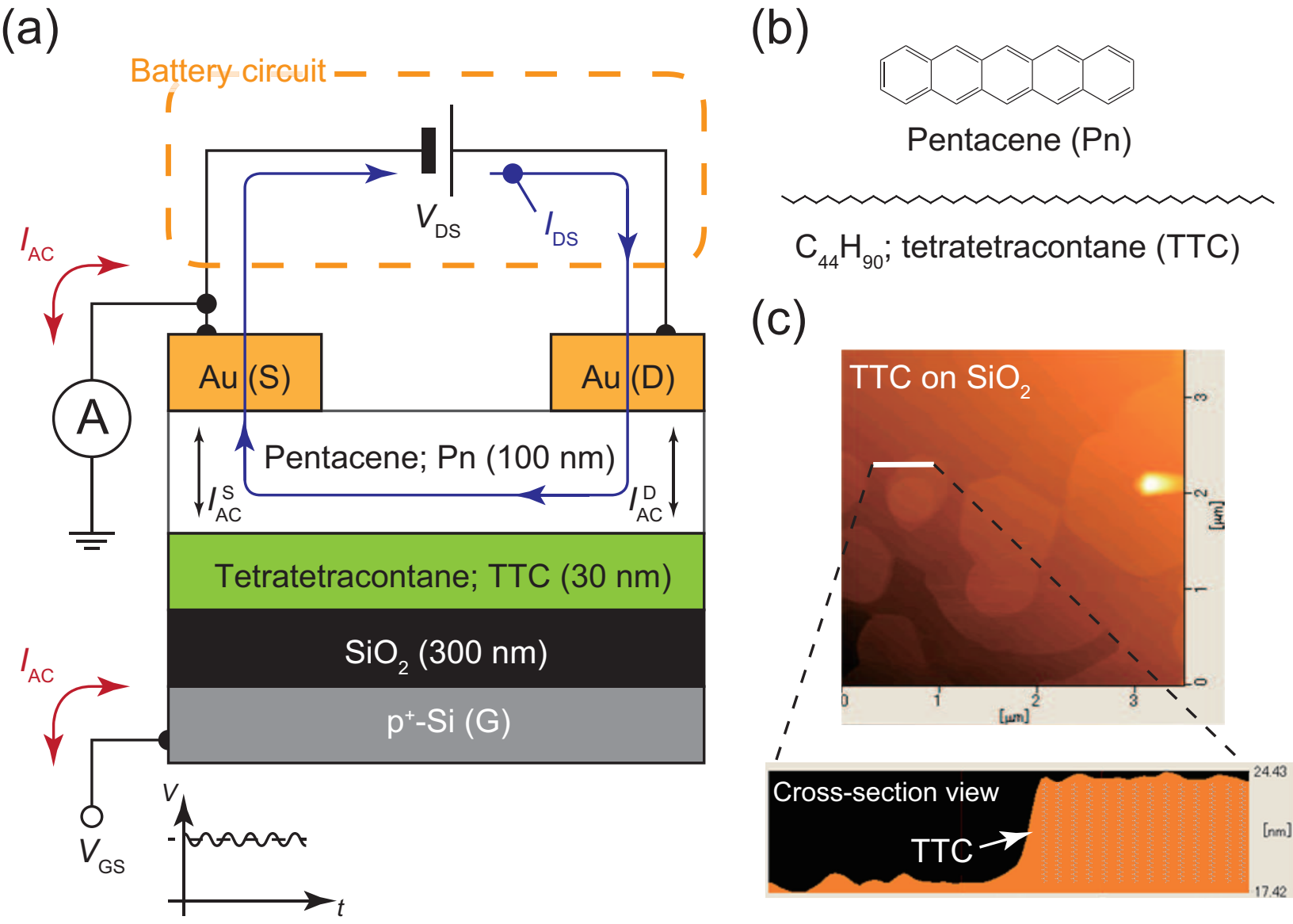

Figure2

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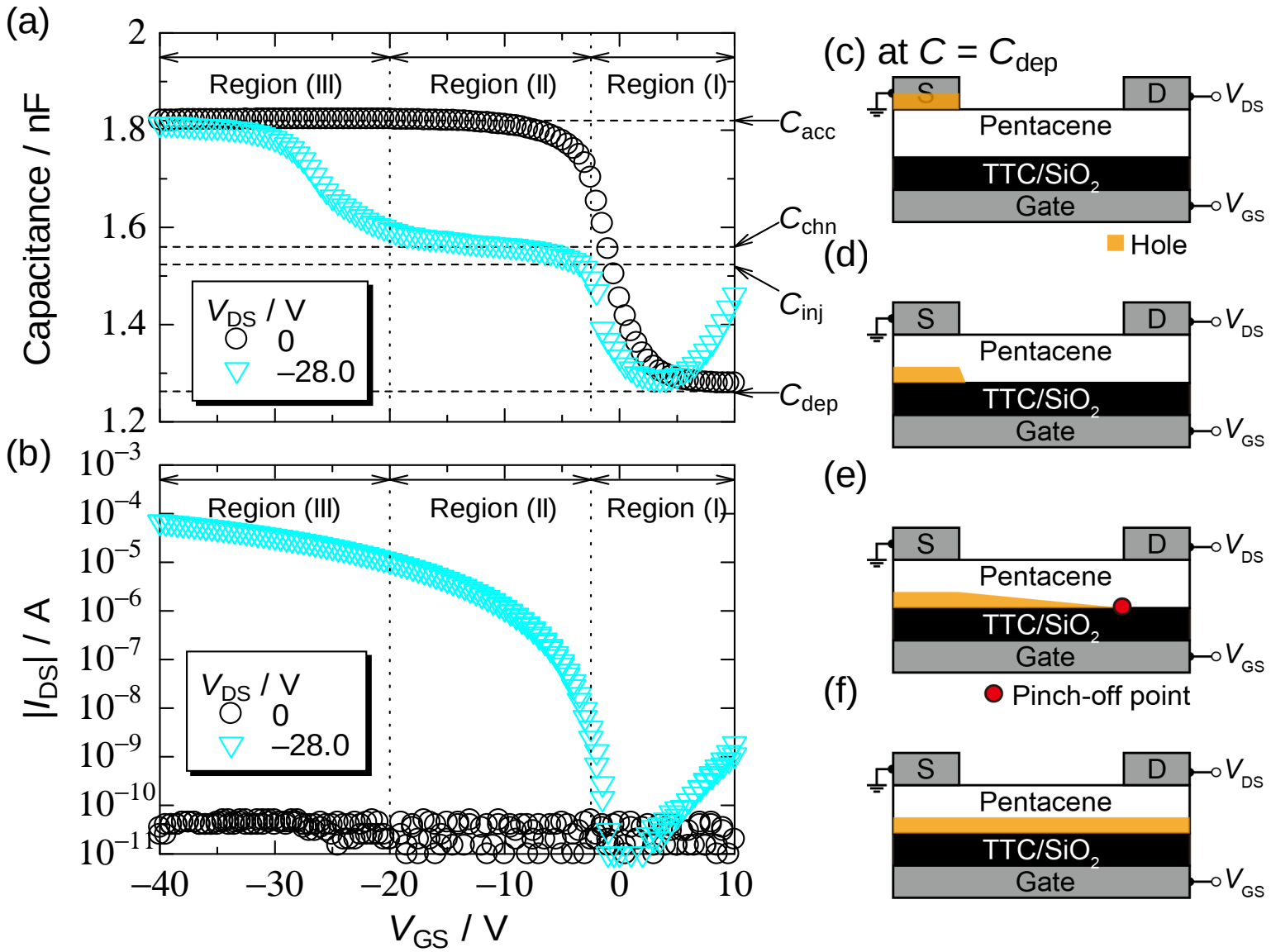

Figure3

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https://doi.org/10.1016/j.orgel.2013.06.013

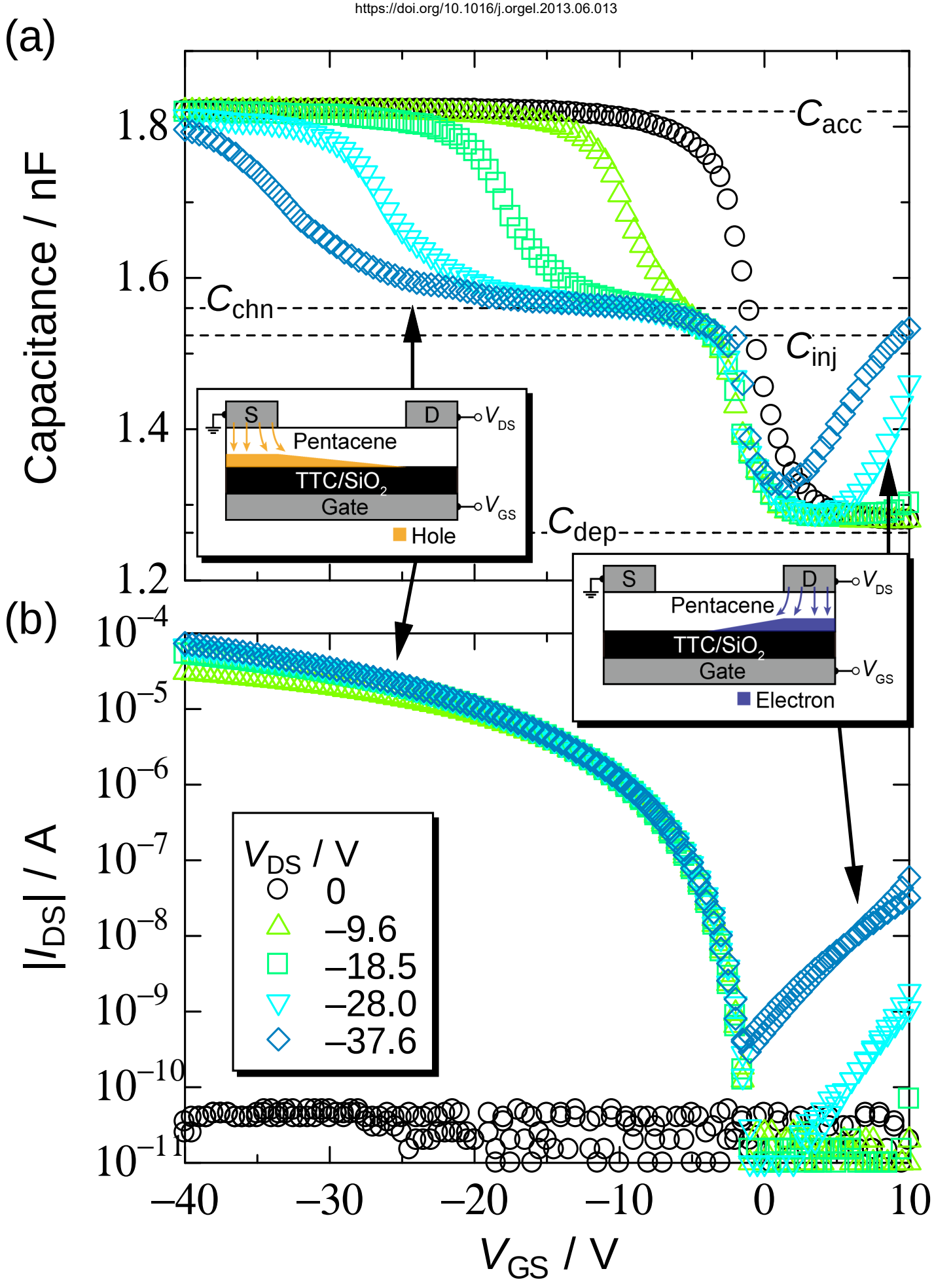

Figure4

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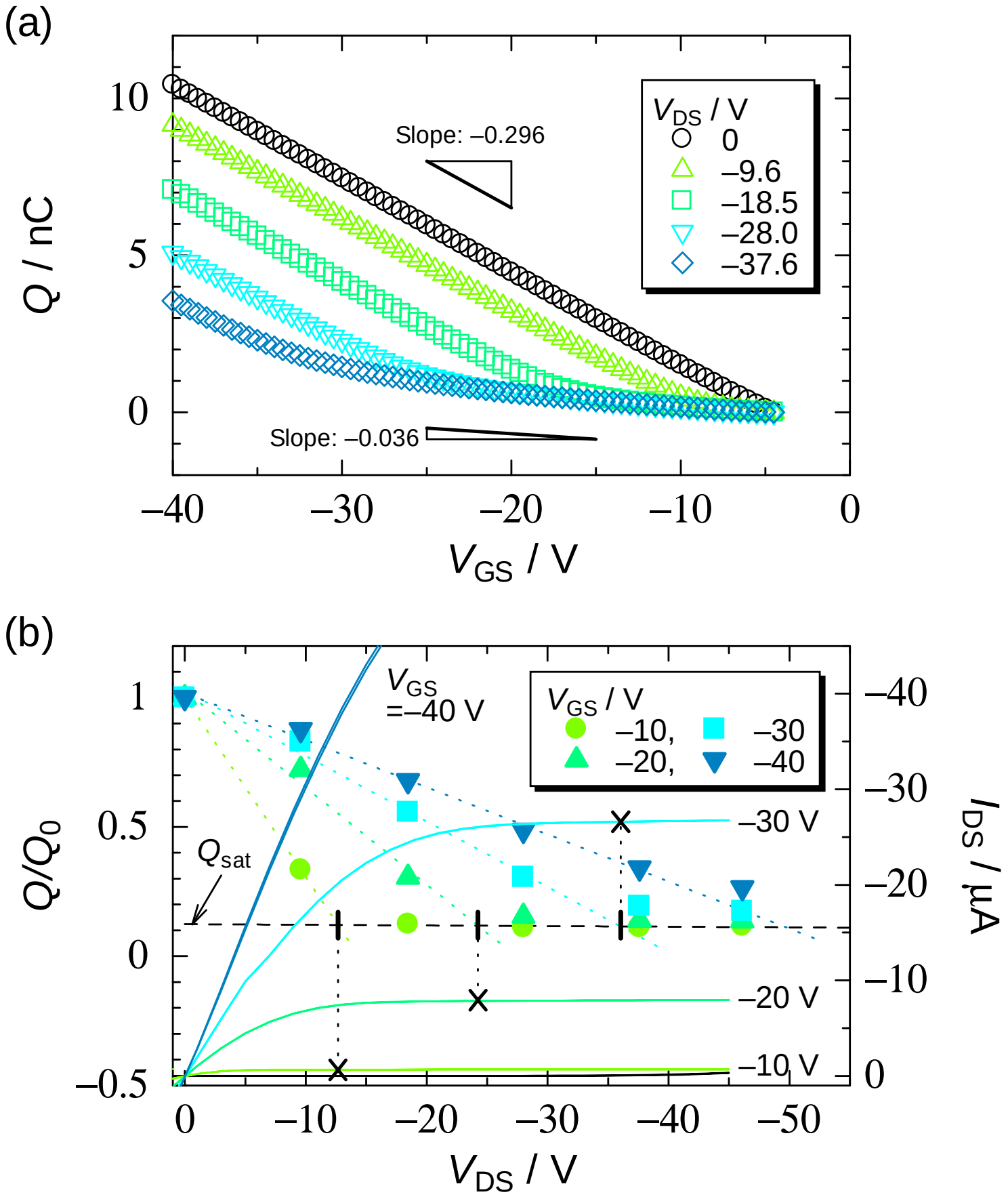
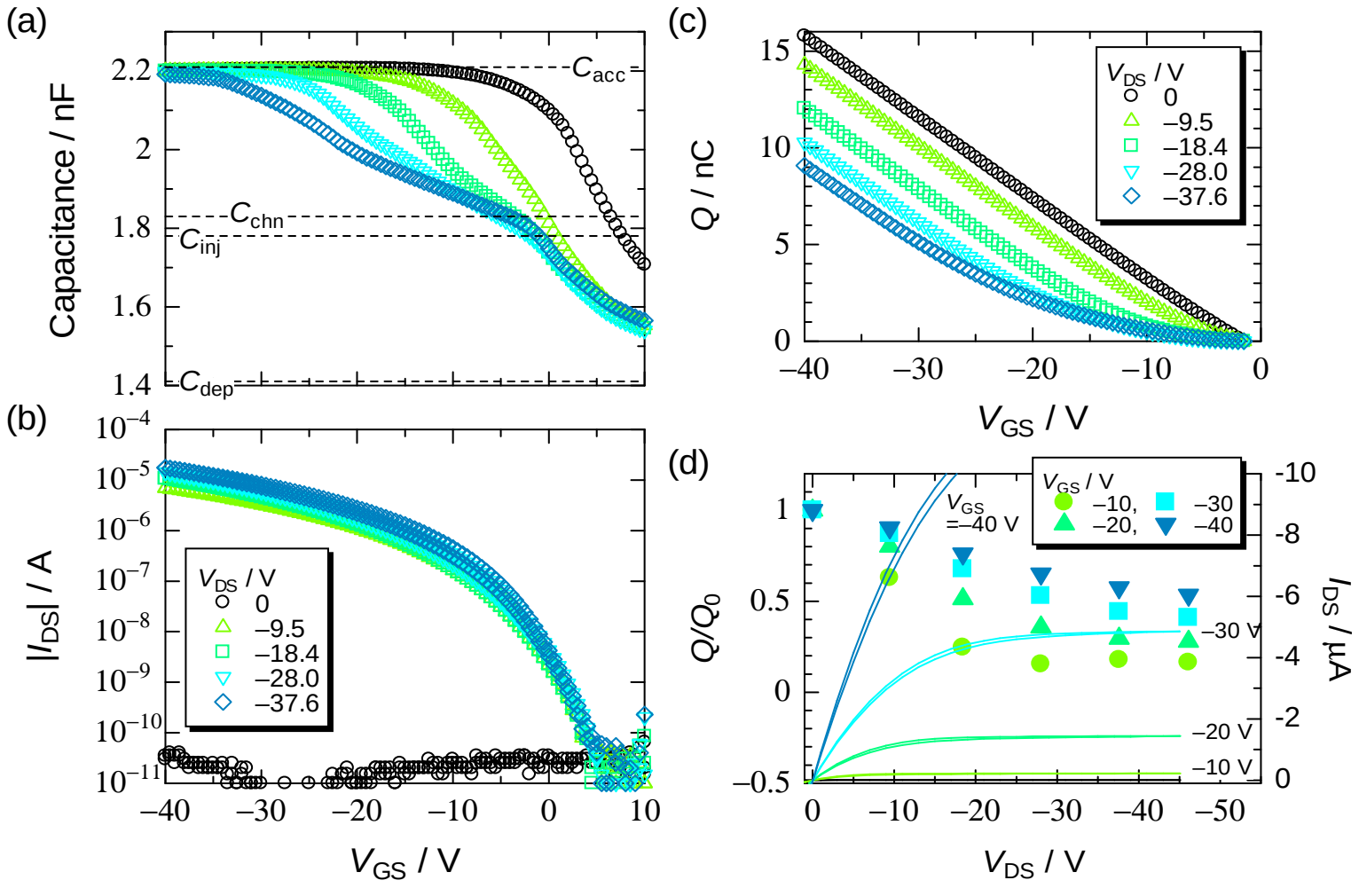


Figure5

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